TOSHIBA

32-bit TX System RISC
TX19 Family
TMP19A61C10XBG
TMP19A61CDXBG

Rev1.0

2008-12-05

32-Bit RISC Microprocessor TX19 Family

TMP19A61C10XBG, TMP19A61CDXBG

1. Overview and features

TMP19A61 is equipped with the TX19A processor core that forms a high-performance 32-bit RISC processor series. The core was developed based on the MIPS32ISA that contains a 32-bit instruction set and the MIPS16eISA that contains an instruction set of high code efficiency. TOSHIBA uniquely integrated these two and the MIPS16e-TX ™ASE (Application Specific Extension), which includes an extended instruction set of high code efficiency.

TMP19A61 is a 32-bit RISC microprocessor with a TX19A processor core and various peripheral functions integrated into one package. It can operate at low voltage with low power consumption.

Features of TMP19A61 are as follows:

(1) TX19A processor core

1) Improved code efficiency and operating performance have been realized through the use of two ISA (Instruction Set Architecture) modes - 16- and 32-bit ISA modes.

- The 16-bit ISA mode instructions are compatible with the MIPS16™ASE instructions of superior code efficiency at the object level.
- The 32-bit ISA mode instructions are compatible with the TX39 instructions of superior operating performance at the object level.

2) Both high performance and low power consumption have been achieved.

•High performance

- Almost all instructions can be executed with one clock.
- High performance is possible via a three-operand operation instruction.
- 5-stage pipeline
- Built-in high-speed memory
- DSP function: A 32-bit multiplication and accumulation operation can be executed with one clock.

•Low power consumption

- Optimized design using a low power consumption library
- Standby function that stops the operation of the processor core

3) High-speed interrupt response suitable for real-time control

- Independency of the entry address
- Automatic generation of factor-specific vector addresses
- Automatic update of interrupt mask levels

(2) Internal program memory and data memory

Product name	Built-in ROM	Built-in RAM
TMP19A61C10XBG	1Mbyte	48Kbyte
TMP19A61CDXBG	512Kbyte	40Kbyte
TMP19A61F10XBG	1Mbyte(Flash)	48Kbyte

- ROM correction function: 8word×12 block

(3) External memory expansion

- Expandable to 16 megabytes (for both programs and data)
- External data bus:

  Separate bus/multiplexed bus : Coexistence of 8- and 16-bit widths is possible.
  Chip select/wait controller : 4 channels
  Added CS recovery function (wait is inserted within RD (WR)↑−CS↑)
  (For 1 clock)
  External wait X+2N-capable（X=2 to 15）
  Changed ALE width (1-4 clocks)

(4) DMA controller : 8 channels

- Activated by an interrupt or software
- Data to be transferred to internal memory, internal I/O, external memory, and external I/O

(5)16-bit timer : 36 channels

- 16-bit interval timer mode
- 16-bit event counter mode
- 16-bit PPG output
- Input capture function
- 2-phase pulse input counter function (2 channels assigned to perform this function):

(6)32-bit timer

- 32-bit input capture register: 4 channels
- 32-bit compare register: 4 channels
- 32-bit time base timer: 2 channels

(7) General-purpose serial interface: 9 channels

- Selectable between the UART mode and the synchronization mode

(8) Serial bus interface: 2 channels

- Selectable between I^2C bus mode/ the clock synchronization mode

(9) High-speed serial bus interface: 2 channels

- Selectable between UART mode/ the high-speed synchronization mode (max.: 10Mbps fsys=40MHz).

(10) 10-bit A/D converter (with S/H): 32 channels
- An optional trigger by the internal timer
- Fixed channel/scan mode
- Single/repeat mode
- Top-priority conversion mode
- Timer monitor function

  1.7usec@27MHz (at 54MHz) 1.15usec@40MHz (at 40MHz)
  (Consists of 2 units. Capable of simultaneous conversion. No definition for error between units)

(11) Watchdog timer: 1 channel
(12) Chip select/ wait controller: 6 channels
(13) Interrupt function
- CPU: 2 factors …software interrupt instruction
- Internal 83 factors…The order of precedence can be set over 7 levels
  (except the watchdog timer interrupt)
  39- independent-interrupt factors are included.
- External: 16 factors…The order of precedence can be set over 7 levels.
  (Except for NMI interrupt)
  4 factors, which are KWUP, are united as an interrupt factor.

(14) Input and output ports: 212 pins
(15) Standby function
- Two stand-by modes (IDLE, STOP)

(16) Clock generator
- Built-in PLL (multiplication by 4)
- Clock gear function: The high-speed clock can be divided into 1/1, 1/2，1/4, 1/8.

(17) Endian: Bi-endian (big-endian/little-endian)
Big endian

Upper address

31 24	23 16	15 8	7 0	Word address
8	9	10	11	8
4	5	6	7	4
0	1	2	3	0

Lower address

- The most significant byte is 0 (bit 31-24).
- The address of the most significant byte specifies the word address.

Little endian

Upper address

31 24	23 16	15 8	7 0	Word address
11	10	9	8	8
7	6	5	4	4
3	2	1	0	0

Lower address

- The least significant byte is 0 (bit 7-0).
- The address of the least significant byte specifies the word address.

(18) Operating frequency
- 54MHz (DVCC15 = 1.35V-1.65V)

(19) Operating voltage range
- Core: 1.35 - 1.65V
- I/O: 1.65 - 3.3 V
- ADC: 2.7 - 3.3 V

(20) Temperature range
- -20°C-85°C

(21) Package
- P-TFBGA289 (11mm×11mm, 0.5mm pitch)

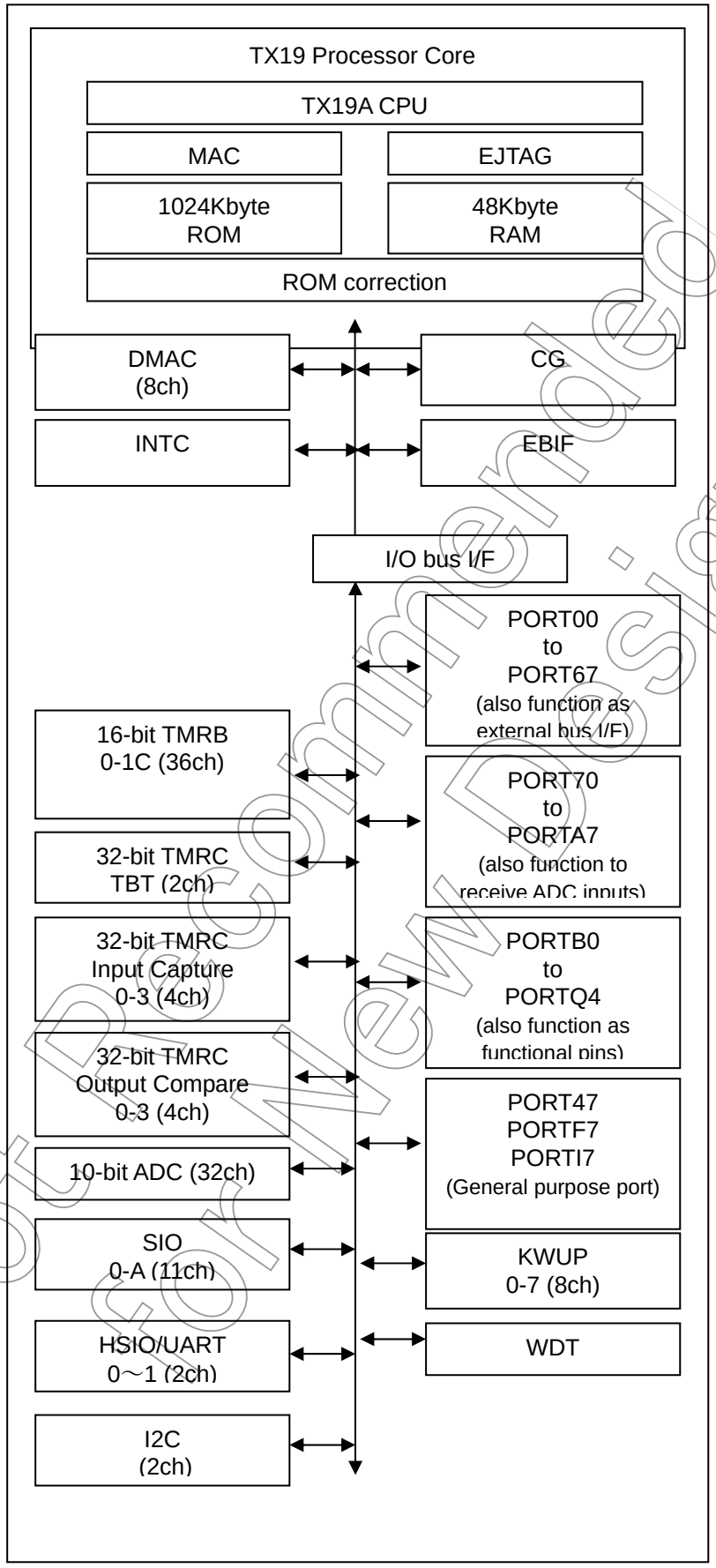


Fig. 1.1 TMP19A61C10/ CDXBG Block Diagram

2. Pin Layout and Pin Functions

This section shows the pin layout of TMP19A61C10/CD and describes the names and functions of input and output pins.

2.1 Pin Layout (Top view)

Fig. 2.1.1 shows the pin layout of TMP19A61C10/CD.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20
C1	C2																	C19	C20
D1	D2		D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17		D19	D20
E1	E2		E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16	E17		E19	E20
F1	F2		F4	F5											F16	F17		F19	F20
G1	G2		G4	G5		G7	G8	G9	G10	G11	G12	G13	G14		G16	G17		G19	G20
H1	H2		H4	H5		H7	H8	H9	H10	H11	H12	H13	H14		H16	H17		H19	H20
J1	J2		J4	J5		J7	J8	J9				J13	J14		J16	J17		J19	J20
K1	K2		K4	K5		K7	K8					K13	K14		K16	K17		K19	K20
L1	L2		L4	L5		L7	L8					L13	L14		L16	L17		L19	L20
M1	M2		M4	M5		M7	M8					M13	M14		M16	M17		M19	M20
N1	N2		N4	N5		N7	N8	N9	N10	N11	N12	N13	N14		N16	N17		N19	N20
P1	P2		P4	P5		P7	P8	P9	P10	P11	P12	P13	P14		P16	P17		P19	P20
R1	R2		R4	R5											R16	R17		R19	R20
T1	T2		T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17		T19	T20
U1	U2		U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17		U19	U20
V1	V2																	V19	V20
W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	W17	W18	W19	W20
Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17	Y18	Y19	Y20

Fig. 2.1.1 Pin Layout Diagram (P-FBGA289)

2.2 Pin numbers and pin names

Table 2.2 show the pin numbers and pin names of TMP19A61C10/CD.

PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name
A1	N.C(GND)	B1	N.C(GND)	C1	PL0/TC4IN	D1	PL2
A2	N.C(GND)	B2	N.C(GND)	C2	PL1/TC5IN	D2	PL3/TCOUTB0
A3	RESET	B3	PCST0				
A4	PCST1	B4	PCST2			D4	DVSS
A5	PCST3	B5	PCST4			D5	PQ0/DREQ2
A6	DCLK	B6	TOVR			D6	TCK
A7	TDO	B7	TDI			D7	DINT
A8	PP6/TPC6/TPD6	B8	PP7/TPC7/TPD7			D8	PO6/*HSCLK1/HCTS1
A9	PP4/TPC4/TPD4	B9	PP5/TPC5/TPD5			D9	PO4/HTXD1
A10	PP2/TPC2/TPD2	B10	PP3/TPC3/TPD3			D10	PO2/KEY2
A11	PP0/TPC0/TPD0	B11	PP1/TPC1/TPD1			D11	PO0/KEY0
A12	PJ4/	B12	PJ5/			D12	PJ6/
A13	PJ2/	B13	PJ3/			D13	PM6/TCOUTA0
A14	PJ0/	B14	PJ1/			D14	PM4/INT4
A15	PF6/SCLK1/CTS1	B15	PF7			D15	PM2/INT2
A16	PF4/TXD1	B16	PF5/RXD1			D16	PM0/INT0
A17	PF2/SCLK0/CTS0	B17	PF3			D17	PG5/
A18	PF0/TXD0	B18	PF1/RXD0				
A19	N.C(GND)	B19	N.C(GND)	C19	PG7/TBTIN2	D19	PG4/
A20	N.C(GND)	B20	N.C(GND)	C20	PG6/	D20	PG3/TBTIN1

Table 2.2 Pin Numbers and Pin Names (1/3)

PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name
E1	PL4/HTXD0	F1	PL6/HSCLK0/HCTS0	G1	P00/D0/AD0	H1	P02/D2/AD2
E2	PL5/HRXD0	F2	PL7/TCOUTB1	G2	P01/D1/AD1	H2	P03/D3/AD3
E4	PQ1/DACK2	F4	PQ2/DREQ3	G4	PK0/TXD8	H4	PK2/*SCLK8/CTS8
E5	DVSS	F5	PQ3/DACK3	G5	PK1/RXD8	H5	PK3/TC0IN
E6	TRST						
E7	TMS			G7	DVSSC	H7	PK4/TC1IN
E8	PO7/			G8	EJE	H8	DVSSD
E9	PO5/HRXD1			G9	DVCC33	H9	NC(FVCC30)
E10	PO3/KEY3			G10	DVCC34	H10	NC(FVCC31)
E11	PO1/KEY1			G11	DVCC34	H11	DVCC15(FVCC15)
E12	PJ7/			G12	DVCC34	H12	DVCC15
E13	PM7/TCOUTA1			G13	DVCC32	H13	AVSS1
E14	PM5/INT5			G14	AVSS0	H14	P85/ANA13
E15	PM3/INT3						
E16	PM1/INT1	F16	P77/ANA7	G16	P87/ANA15	H16	P84/ANA12
E17	PG2/SCLK2/CTS2	F17	P76/ANA6	G17	P86/ANA14	H17	P83/ANA11
E19	PG1/RXD2	F19	P75/ANA5	G19	P73/ANA3	H19	P71/ANA1
E20	PG0/TXD2	F20	P74/ANA4	G20	P72/ANA2	H20	P70/ANA0
J1	P04/D4/AD4	K1	P06/D6/AD6	L1	P10/D8/AD8/A8	M1	P12/D10/AD10/A10
J2	P05/D5/AD5	K2	P07/D7/AD7	L2	P11/D9/AD9/A9	M2	P13/D11/AD11/A11
J4	P50/A0	K4	P52/A2	L4	P54/A4	M4	P56/A6
J5	P51/A1	K5	P53/A3	L5	P55/A5	M5	P57/A7
J7	PK5/SO1/SDA1	K7	PK6/SI1/SCL1	L7	PK7/SCK1	M7	BW0
J8	DVCC30	K8	DVCC30	L8	DVCC30	M8	DVCC15
J9	DVSS						
J13	AVCC30	K13	AVREFH0	L13	AVREFH1	M13	AVCC31
J14	P82/ANA10	K14	PA7/ANB15	L14	PA4/ANB12	M14	DVCC15
J16	P81/ANA9	K16	PA6/ANB14	L16	PA3/ANB11	M16	PA1/ANB9
J17	P80/ANA8	K17	PA5/ANB13	L17	PA2/ANB10	M17	PA0/ANB8
J19	P97/ANB7	K19	P95/ANB5	L19	P93/ANB3	M19	P91/ANB1
J20	P96/ANB6	K20	P94/ANB4	L20	P92/ANB2	M20	P90/ANB0
N1	P14/D12/AD12/A12	P1	P16/D14/AD14/A14	R1	P40/*CS0	T1	P42/*CS2
N2	P15/D13/AD13/A13	P2	P17/D15/AD15/A15	R2	P41/*CS1	T2	P43/*CS3
N4	P30/*RD	P4	P32/*HWR	R4	P34/*BUSRQ	T4	P36/R/*W
N5	P31/*WR	P5	P33/*WAIT/*RDY	R5	P35/*BUSAK	T5	P61/A9
						T6	P63/A11
N7	BW1	P7	TEST2			T7	P65/A13
N8	TEST1	P8	TEST3			T8	PN1/INT7
N9	BUSMD	P9	ENDIAN			T9	PN3/ADTRG-A
N10	DVCC15(FVCC15)	P10	*NMI			T10	PN5/
N11	DVCC15	P11	DVCC31			T11	PN7/ADTRG-B
N12	PLLSEL	P12	DVCC31			T12	PH1/RXD4
N13	DVSSF	P13	CVSS			T13	PH3/INT9
N14	CVCC15	P14	DVSS			T14	PH5/RXD5
						T15	PH7/INTA
N16	PC7/TBFIN0	P16	PC5/RXD3	R16	PC3/TBEIN0	T16	DVSSG
N17	PC6/SCLK3/CTS3	P17	PC4/TXD3	R17	PC2/TBDIN0	T17	PC1/TBCIN1
N19	PB7/TBBIN1	P19	PB5/TBAIN1	R19	PB3/TB9IN1	T19	PB1/TB8IN1
N20	PB6/TBBIN0	P20	PB4/TBAIN0	R20	PB2/TB9IN0	T20	PB0/TB8IN0

Table 2.2 Pin Numbers and Pin Names (2/3)

PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name
U1	P44/*CS4	V1	P46/SCOUT	W1	N.C(GND)	Y1	N.C(GND)
U2	P45/*CS5	V2	P47	W2	N.C(GND)	Y2	N.C(GND)
				W3	P21/A17/A1/A17	Y3	P20/A16/A0/A16
U4	P37/ALE			W4	P23/A19/A3/A19	Y4	P22/A18/A2/A18
U5	P60/A8			W5	P25/A21/A5/A21	Y5	P24/A20/A4/A20
U6	P62/A10			W6	P27/A23/A7/A23	Y6	P26/A22/A6/A22
U7	P64/A12			W7	P67/A15	Y7	P66/A14
U8	PN0/INT6			W8	PI1/RXD6	Y8	PI0/TXD6
U9	PN2/INT8			W9	PI3/INTB	Y9	PI2/SCLK6/CLS6
U10	PN4/			W10	PI5/RXD7	Y10	PI4/TXD7
U11	PN6/			W11	PI7	Y11	PI6/SCLK7/CTS7
U12	PH0/TXD4			W12	PE1/TB17OUT	Y12	PE0/TB16OUT
U13	PH2/SCLK4/CTS4			W13	PE3/TB19OUT	Y13	PE2/TB18OUT
U14	PH4/TXD5			W14	PE5/SO0/SDA0	Y14	PE4/TB1AOUT
U15	PH6/SCLK5/CTS5			W15	PE7/SCK0	Y15	PE6/SI0/SCL0
U16	PD2/TB11IN0			W16	PD1/TB10IN1	Y16	PD0/TB10IN0
U17	DVSSH			W17	PD4/TB12IN0	Y17	PD3/TB11IN1
				W18	PD6/TB14OUT	Y18	PD5/TB12IN1
U19	PC0/TBCIN0	V19	PD7/TB15OUT	W19	N.C(GND)	Y19	N.C(GND)
U20	X2	V20	X1	W20	N.C(GND)	Y20	N.C(GND)

* Parenthetic pin names are for TMP19A61F10XBG incorporating FLASH memory (excluding GND).

Table 2.2 Pin Numbers and Pin Names (3/3)

2.3 Pin Names and Functions

Tables 2.3 show the names and functions of input and output pins.

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
P00~P07 D0~D7 AD0~D7	8	I/O I/O I/O	Port 0: I/O port that allows input/output to be set in units of bits Data (lower): Data bus 0~7 (separate bus mode) Address data (lower): Address data bus 0~7 (multiplexed bus mode)				DVCC30
P10~P17 D8~D15 AD8~AD15 A8~A15	8	I/O I/O I/O O	Port 1: I/O port that allows input/output to be set in units of bits Data (upper): Data bus 8~15: (separate bus mode) Address data (upper): Address data bus 8~15 (multiplexed bus mode) Address: Address bus 8~15 (multiplexed bus mode)				DVCC30
P20~P27 A16~A23 A0~A7 A16~A23	8	I/O O O O	Port 2: I/O port that allows input/output to be set in units of bits Address: Address bus 16~23 (separate bus mode) Address: Address bus 0~7 (multiplexed bus mode) Address: Address bus 16~23 (multiplexed bus mode)				DVCC30
P30 *RD	1	I/O O	Port 30:I/O port Read: Strobe signal for reading external memory	PU			DVCC30
P31 *WR	1	I/O O	Port 31:I/O port Write: Strobe signal for writing data of D0 to D7 pins	PU			
P32 *HWR	1	I/O O	Port 32:Input/output port Write upper-pin data: Strobe signal for writing data of D8 to D15 pins	PU			
P33 *WAIT *RDY	1	I/O I I	Port 33:I/O port Wait: Pin for requesting CPU to put a bus in a wait state Ready: Pin for notifying CPU that a bus is ready	PU			
P34 *BUSRQ	1	I/O I	Port 34:I/O port Bus request: Signal requesting CPU to allow an external master to take the bus control authority	PU			
P35 *BUSAK	1	I/O O	Port 35:I/O port Bus acknowledge: Signal notifying that CPU has released the bus control authority in response to *BUSREQ	PU			
P36 R/*W	1	I/O O	Port 36:I/O port Read/write: "1" shows a read cycle or a dummy cycle. "0" shows a write cycle.	PU			
P37 ALE	1	I/O O	Port 37:: I/O port Address latch enable (address latch is enabled only if access to external memory is taking place, that is multiplex bus mode)				
P40 *CS0	1	I/O O	Port 40:I/O port Chip select 0:"0" is output if the address is in a designated address area.	PU			DVCC30
P41 *CS1	1	I/O O	Port 41:I/O port Chip select 1:"0" is output if the address is in a designated address area.	PU			
P42 *CS2	1	I/O O	Port 42:I/O port Chip select 2:"0" is output if the address is in a designated address area.	PU			
P43 *CS3	1	I/O O	Port 43:I/O port Chip select 3:"0" is output if the address is in a designated address area.	PU			
P44 *CS4	1	I/O O	Port 44:I/O port Chip select 4:"0" is output if the address is in a designated address area.	PU			
P45 *CS5	1	I/O O	Port 45:I/O port Chip select 5:"0" is output if the address is in a designated address area.	PU			
P46 SCOUT	1	I/O O	Port 46: I/O port System clock output: Selectable between high- and low-speed clock outputs, as in the case of CPU				
P47	1	I/O	Port 47: I/O port				

PU: Programmable pull-up

Table 2.3 Pin Names and Functions (1/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
P50~P57 A0~A7	8	I/O O	Port 5: I/O port that allows input/output to be set in units of bits Address: Address bus 0~7 (separate bus mode)				DVCC 30
P60~P67 A8~A15	8	I/O O	Port 6 :I/O port Address: Address bus 8~15 (separate bus mode)				DVCC 30
P70~P77 ANA0~ANA7	8	I	Port 7:Port used exclusively for input Analog input: Input from A/D converter				AVCC 30
P80~P87 ANA8~ANA15	8	I	Port 8:Port used exclusively for input Analog input: Input from A/D converter				AVCC 30
P90~P97 ANB0~ANB7	8	I	Port 9:Port used exclusively for input Analog input: Input from A/D converter				AVCC 31
PA0~PA7 ANB8~ANB15	8	I	Port A: Port used exclusively for input Analog input: Input from A/D converter				AVCC 31
PB0 TB8IN0	1	I/O I	Port B0:I/O port 16-bit timer 8 input 0:For inputting the capture trigger of a 16-bit timer 8		○		DVCC31
PB1 TB8IN1	1	I/O I	Port B1:I/O port 16-bit timer 8 input 1:For inputting the capture trigger of a 16-bit timer 8		○		
PB2 TB9IN0	1	I/O I	Port B2:I/O port 16-bit timer 9 input 0:For inputting the capture trigger of a 16-bit timer 9		○		
PB3 TB9IN1	1	I/O I	Port B3:I/O port 16-bit timer 9 input 1:For inputting the capture trigger of a 16-bit timer 9		○		
PB4 TBAIN0	1	I/O I	Port B4:I/O port 16-bit timer A input 0:For inputting the capture trigger of a 16-bit timer A		○		
PB5 TBAIN1	1	I/O I	Port B5:I/O port 16-bit timer A input 1:For inputting the capture trigger of a 16-bit timer A		○		
PB6 TBBIN0	1	I/O I	Port B6:I/O port 16-bit timer B input 0:For inputting the capture trigger of a 16-bit timer B		○		
PB7 TBBIN1	1	I/O I	Port B7:I/O port 16-bit timer B input 1:For inputting the capture trigger of a 16-bit timer B		○		
PC0 TBCIN0	1	I/O I	Port C0:I/O port 16-bit timer C input 0:For inputting the capture trigger of a 16-bit timer C/Two-phase counter input pin		○		DVCC31
PC1 TBCIN1	1	I/O I	Port C1:I/O port 16-bit timer C input 1:For inputting the capture trigger of a 16-bit timer C/Two-phase counter input pin		○		
PC2 TBDIN0	1	I/O I	Port C2:I/O port 16-bit timer D input 0:For inputting the capture trigger of a 16-bit timer D		○		
PC3 TBEIN0	1	I/O I	Port C3:I/O port 16-bit timer D input 1:For inputting the capture trigger of a 16-bit timer D		○		

Table 2.3 Pin Names and Functions (2/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
PC4 TXD3	1	I/O O	Port C4:I/O port Sending serial data 3: Open drain output pin			○	DVCC31
PC5 RXD3	1	I/O I	Port C5:I/O port Receiving serial data 3				
PC6 *SCLK3 CTS3	1	I/O I/O I	Port C6:I/O port Serial clock I/O 3 : Open drain output pin Handshake input pin			○	
PC7 TBFIN0	1	I/O I	Port C7:I/O port 16-bit timer F input 0:For inputting the capture trigger of a 16-bit timer F		○		
PD0 TB10IN0	1	I/O I	Port D0:I/O port 16-bit timer 10 input 0:For inputting the capture trigger of a 16-bit timer 10		○		DVCC31
PD1 TB10IN1	1	I/O I	Port D1:I/O port 16-bit timer 10 input 1:For inputting the capture trigger of a 16-bit timer 10		○		
PD2 TB11IN0	1	I/O I	Port D2:I/O port 16-bit timer 11 input 0:For inputting the capture trigger of a 16-bit timer 11		○		
PD3 TB11IN1	1	I/O I	Port D3:I/O port 16-bit timer 11 input 1:For inputting the capture trigger of a 16-bit timer 11		○		
PD4 TB12IN0	1	I/O I	Port D4:I/O port 16-bit timer 12 input 0:For inputting the capture trigger of a 16-bit timer 12 /Two-phase counter input pin		○		
PD5 TB12IN1	1	I/O I	Port D5:I/O port 16-bit timer 12 input 1:For inputting the capture trigger of a 16-bit timer 12 /Two-phase counter input pin		○		
PD6 TB14OUT	1	I/O O	Port D6:I/O port 16-bit timer 14 output :16bit timer 14 variable PPG output				
PD7 TB15OUT	1	I/O O	Port D7:I/O port 16-bit timer 15 output :16bit timer 15 variable PPG output				
PE0 TB16OUT	1	I/O O	Port E0:I/O port 16-bit timer 16 output :16bit timer 16 variable PPG output				DVCC31
PE1 TB17OUT	1	I/O O	Port E1:I/O port 16-bit timer 17 output :16bit timer 17 variable PPG output				
PE2 TB18OUT	1	I/O O	Port E2:I/O port 16-bit timer 18 output :16bit timer 18 variable PPG output				
PE3 TB19OUT	1	I/O O	Port E3:I/O port 16-bit timer 19 output :16bit timer 19 variable PPG output				
PE4 TB1AOUT	1	I/O O	Port E4:I/O port 16-bit timer 1A output :16bit timer 1A variable PPG output				
PE5 SO0 SDA0	1	I/O O I/O	Port E5:I/O port Pin for sending data if the serial bus interface operates in the SIO mode Pin for sending and receiving data if the serial bus interface operates in the I2C mode **Open drain output pin**		○	○	
PE6 SI0 SCL0	1	I/O O I/O	Port E6:I/O port Pin for receiving data if the serial bus interface operates in the SIO mode Pin for inputting and outputting a clock if the serial bus interface operates in the I2C mode **Open drain output pin**		○	○	
PE7 SCK0	1	I/O I/O	Port E7:I/O port Pin for inputting and outputting a clock if the serial bus interface operates in the I2C mode				

OpenDrain: Programmable open-drain

Table 2.3 Pin Names and Functions (3/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
PF0 TXD0	1	I/O O	Port F0:Input/output port Sending serial data 0: Open drain output pin			○	DVCC32
PF1 RXD0	1	I/O I	Port F1 Input/output port Receiving serial data 0				
PF2 *SCLK0 CTS0	1	I/O I/O I	Port F2:Input/output port Serial clock input/output 0 : Open drain output pin Handshake input pin			○	
PF3	1	I/O	Port F3:Input/output port				
PF4 TXD1	1	I/O O	Port F4:Input/output port Sending serial data 1: Open drain output pin			○	
PF5 RXD1	1	I/O I	Port F5 Input/output port Receiving serial data 1				
PF6 *SCLK1 CTS1	1	I/O I/O I	Port F6:Input/output port Serial clock input/output 1 : Open drain output pin Handshake input pin			○	
PF7	1	I/O	Port F7:Input/output port				
PG0 TXD2	1	I/O O	Port G0:Input/output port Sending serial data 2: Open drain output pin			○	DVCC32
PG1 RXD2	1	I/O I	Port G1 Input/output port Receiving serial data 2				
PG2 *SCLK2 CTS2	1	I/O I/O I	Port G2:Input/output port serial clock input/output 2 : Open drain output pin Handshake input pin			○	
PG3 TBTIN1	1	I/O I	Port G3:Input/output port 32-bit time base timer input 1:For inputting a 32-bit time base timer		○		
PG4	1	I/O	Port G4:Input/output port				
PG5	1	I/O	Port G5 Input/output port				
PG6	1	I/O	Port G6:Input/output port				
PG7 TBTIN2	1	I/O I	Port G7:Input/output port 32-bit time base timer input 2:For inputting a 32-bit time base timer		○		
PH0 TXD4	1	I/O O	Port H0:Input/output port Sending serial data 4: Open drain output pin			○	DVCC31
PH1 RXD4	1	I/O I	Port H1 Input/output port Receiving serial data 4				
PH2 *SCLK4 CTS4	1	I/O I/O I	Port H2:Input/output port Serial clock input/output 4 : Open drain output pin Handshake input pin			○	
PH3 INT9	1	I/O I	Port H3 Input/output port Interrupt request pin 9: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		

OpenDrain: Programmable open drain

Table 2.3 Pin Names and Functions (4/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
PH4 TXD5	1	I/O O	Port H4:I/O port Sending serial data 5: Open drain output pin			○	DVCC31
PH5 RXD5	1	I/O I	Port H5 I/O port Receiving serial data 5				
PH6 *SCLK5 CTS5	1	I/O I/O I	Port H6:I/O port Serial clock I/O 5 : Open drain output pin Handshake input pin			○	
PH7 INTA	1	I/O I	Port H7 I/O port Interrupt request pin A: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		
PI0 TXD6	1	I/O O	Port I0:I/O port Sending serial data 6: Open drain output pin			○	DVCC31
PI1 RXD6	1	I/O I	Port I1 I/O port Receiving serial data 6				
PI2 *SCLK6 CTS6	1	I/O I/O I	Port I2:I/O port Serial clock I/O 6 : Open drain output pin Handshake input pin			○	
PI3 INTB	1	I/O I	Port I3 I/O port Interrupt request pin B: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		
PI4 TXD7	1	I/O O	Port I4:I/O port Sending serial data 7: Open drain output pin			○	
PI5 RXD7	1	I/O I	Port I5 I/O port Receiving serial data				
PI6 *SCLK7 CTS7	1	I/O I/O I	Port I6:I/O port Serial clock I/O 7 : Open drain output pin Handshake input pin			○	
PI7	1	I/O	Port I7:I/O port				
PJ0	1	I/O	Port J0:I/O port				DVCC32
PJ1	1	I/O	Port J1 I/O port				
PJ2	1	I/O	Port J2:I/O port				
PJ3	1	I/O	Port J3 I/O port				
PJ4	1	I/O	Port J4 I/O port				
PJ5	1	I/O	Port J5:I/O port				
PJ6	1	I/O	Port J6:I/O port				
PJ7	1	I/O	Port J7:I/O port				

OpenDrain: Programmable open drain

Table 2.3 Pin Names and Functions (5/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
PK0 TXD8	1	I/O O	Port K0:Input/output port Sending serial data 8: Open drain output pin			○	DVCC33
PK1 RXD8	1	I/O I	Port K1:Input/output port Receiving serial data 8				
PK2 ＊SCLK8 CTS8	1	I/O I/O I	Port K2:Input/output port Serial clock input/output 8 : Open drain output pin Handshake input pin			○	
PK3 TC0IN	1	I/O I	Port K3:Input/output port For inputting the capture trigger for 32-bit timer		○		
PK4 TC1IN	1	I/O I	Port K4:Input/output port For inputting the capture trigger for 32-bit timer		○		
PK5 SO1 SDA1	1	I/O O I/O	Port K5:Input/output port Pin for sending data if the serial bus interface operates in the SIO mode. Pin for sending and receiving data if the serial bus interface operates in the I2C mode. **Open drain output pin**		○	○	
PK6 SI1 SCL1	1	I/O I I/O	Port K6:Input/output port Pin for receiving data if the serial bus interface operates in the SIO mode Pin for inputting and outputting a clock if the serial bus interface operates in the I2C mode. **Open drain output pin**		○	○	
PK7 SCK1	1	I/O I/O	Port K7:Input/output port Pin for inputting and outputting a clock if the serial bus interface 1 operates in the SIO mode				
PL0 TC4IN	1	I/O I	Port L0:Input/output port For inputting the capture trigger for 32-bit timer		○		DVCC33
PL1 TC5IN	1	I/O I	Port L1:Input/output port For inputting the capture trigger for 32-bit timer		○		
PL2	1	I/O	Port L2:Input/output port				
PL3 TCOUTB0	1	I/O O	Port L3:Input/output port Outputting 32-bit timer if the result of a comparison is a match				
PL4 HTXD0	1	I/O O	Port L4:Input/output port Sending serial data 0 in high speed: Open drain output pin			○	
PL5 HRXD0	1	I/O I	Port L5 Input/output port Receiving serial data 0 in high speed				
PL6 ＊HSCLK0 HCTS0	1	I/O I/O I	Port L6:Input/output port High-speed serial clock input/output 0 : Open drain output pin Handshake input pin			○	
PL7 TCOUTB1	1	I/O O	Port L7:Input/output port Outputting 32-bit timer if the result of a comparison is a match				
PM0 INT0	1	I/O I	Port M0:Input/output port Interrupt request pin 0: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		DVCC32
PM1 INT1	1	I/O I	Port M1:Input/output port Interrupt request pin 1: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		
PM2 INT2	1	I/O I	Port M2:Input/output port Interrupt request pin 2: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		
PM3 INT3	1	I/O I	Port M3:Input/output port Interrupt request pin 3: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		

OpenDrain: Programmable open drain

Table 2.3 Pin Names and Functions (6/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
PM4 INT4	1	I/O I	Port M4:I/O port Interrupt request pin 4: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		DVCC32
PM5 INT5	1	I/O I	Port M5:I/O port Interrupt request pin 5: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		
PM6 TCOUTA0	1	I/O I	Port M6:I/O port Outputting 32-bit timer if the result of a comparison is a match				
PM7 TCOUTA1	1	I/O I	Port M7:I/O port Outputting 32-bit timer if the result of a comparison is a match				
PN0 INT6	1	I/O I	Port N0:I/O port Interrupt request pin 6: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		DVCC31
PN1 INT7	1	I/O I	Port N1:I/O port Interrupt request pin 7: Selectable between “H” level, “L” level, rising edge and falling edge **(With Noise filter)**		○		
PN2 INT8	1	I/O I	Port N2:I/O port Interrupt request pin 8: Selectable between “H” level, “L” level, rising edge, falling edge and both edges **(With Noise filter)**		○		
PN3 ADTRG-A	1	I/O I	Port N3:I/O port Pin for starting A/D trigger or A/D converter from an external source				
PN4	1	I/O	Port N4:I/O port				
PN5	1	I/O	Port N5 I/O port				
PN6	1	I/O	Port N6:I/O port				
PN7 ADTRG-B	1	I/O I	Port N7:I/O port Pin for starting A/D trigger or A/D converter from an external source				
PO0 KEY0	1	I/O I	Port O0:I/O port Key On Wake UP input 0 :**(With Noise filter)**	PU	○		DVCC34
PO1 KEY1	1	I/O I	Port O1:I/O port Key On Wake UP input 1 :**(With Noise filter)**	PU	○		
PO2 KEY2	1	I/O I	Port O2:I/O port Key On Wake UP input 2 :**(With Noise filter)**	PU	○		
PO3 KEY3	1	I/O I	Port O3:I/O port Key On Wake UP input 3 :**(With Noise filter)**	PU	○		
PO4 HTXD1	1	I/O O	Port O4:I/O port Sending serial data 1 in high speed: Open drain output pin			○	
PO5 HRXD1	1	I/O I	Port O5:I/O port Receiving serial data 1 in high speed				
PO6 *HSCLK1 HCTS1	1	I/O I/O I	Port O6:I/O port Serial clock I/O 1 : Open drain output pin Handshake input pin			○	
PO7	1	I/O	Port O7:I/O port				

OpenDrain: Programmable open drain

PU: Programmable pull-up

Table 2.3 Pin Names and Functions (7/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
PP0 TPC0 TPD0	1	I/O O O	Port P0:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				DVCC34
PP1 TPC1 TPD1	1	I/O O O	Port P1:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				
PP2 TPC2 TPD2	1	I/O O O	Port P2:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				
PP3 TPC3 TPD3	1	I/O O O	Port P3:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				
PP4 TPC4 TPD4	1	I/O O O	Port P4:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				
PP5 TPC5 TPD5	1	I/O O O	Port P5:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				
PP6 TPC6 TPD6	1	I/O O O	Port P6:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				
PP7 TPC7 TPD7	1	I/O O O	Port P7:Input/output port Outputting trace data from the program counter: Signal for DSU-ICE Outputting trace data from the data access address: Signal for DSU-ICE				
PQ0 DREQ2	1	I/O I	Port Q0:Input/output port DMA request signal 2: For inputting the request to transfer data by DMA from an external I/O device to DMA2				DVCC34
PQ1 DACK2	1	I/O O	Port Q1:Input/output port DMA acknowledge signal 2: Signal showing that DREQ2 have acknowledged a DMA transfer request				
PQ2 DREQ3	1	I/O I	Port Q2:Input/output port DMA request signal 3: For inputting the request to transfer data by DMA from an external I/O device to DMA3				
PQ3 DACK3	1	I/O O	Port Q3:Input/output port DMA acknowledge signal 3: Signal showing that DREQ3 have acknowledged a DMA transfer request				
DCLK	1	O	Debug clock: Signal for DSU-ICE				DVCC34
*EJE	1	I	EJTAG enable: Signal for DSU-ICE **(With Noise filter)**	PU*1	○		
*DINT	1	I	Debug interrupt: Signal for DSU-ICE **(With Noise filter)**	PU*1	○		
PCST0	1	O	PC trace status: Signal for DSU-ICE				
PCST1	1	O	PC trace status: Signal for DSU-ICE				
PCST2	1	O	PC trace status: Signal for DSU-ICE				
PCST3	1	O	PC trace status: Signal for DSU-ICE				
PCST4	1	O	PC trace status: Signal for DSU-ICE				

PU*1: Fixed to pull-up

Table 2.3 Pin Names and Functions (8/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
TOVR	1	O	Outputting the status of PD data overflow status: Signal for DSU-ICE				DVCC34
TCK	1	I	Test clock input: Signal for DSU-ICE **(With Noise filter)**	PU*1	○		
TMS	1	I	Test mode select input: Signal for DSU-ICE	PU*1	○		
TDI	1	I	Test data input: Signal for DSU-ICE	PU*1	○		
TDO	1	O	Test data output: Signal for DSU-ICE				
*TRST	1	I	Test reset input: Signal for DSU-ICE **(With Noise filter)**	PD*1	○		
*RESET	1	I	Reset:Intializing LSI **(With Noise filter)**	PU*1	○		DVCC34
X1/X2	2	I/O	Pin for connecting a high-speed oscillator **(X1:Input with Schmitt trigger)**		○*2		CVCC15
*NMI	1	I	Non-maskable interrupt request pin		○		DVCC15
BUSMD	1	I	Pin for setting an external bus mode: This pin functions as a multiplexed bus by sampling the "H (DVCC15) level" at the rise of a reset signal. It also functions as a separate bus by sampling "L" at the rise of a reset signal.		○		
ENDIAN	1	I	Pin for setting endian: It performs a big-endian operation by sampling the "H (DVCC15) level" at the rise of a reset signal, and performs a little-endian operation by sampling "L" at the rise of a reset signal.		○		
PLLSEL	1	I	Pin for setting PLL operation with MASK **(Input with Schmitt trigger)** High(DVCC15) :11~13.5MHz(=X1) Low:8~11MHz(=X1) When performing a reset operation, pull it up or down according to the type of oscillator to be used.		○		
BW0	1	I	TEST pin: To be fixed to DVCC34		○		DVCC34
BW1	1	I	TEST pin: To be fixed to DVCC15		○		DVCC15
TEST1	1	I	TEST pin: Set to OPEN				
TEST2	1	I	TEST pin: Set to OPEN				
TEST3	1	I	TEST pin: Set to OPEN				
AVREFH0	1	–	Reference power supply pin for the A/D converter (H) If the A/D converter is not used, connect (fix) this pin to AVCC3x.				AVCC3
AVREFH1	1	–	Reference power supply pin for the A/D converter (H) If the A/D converter is not used, connect (fix) this pin to AVCC3x.				

PU*1: Fixed to pull-up PD*1: Fixed to pull-down *2: X1 pin only

Table 2.3 Pin Names and Functions (9/10)

Pin name	# of pins	Input or output	Function	PU/ PD	Schmitt	Open Drain	PS
AVCC30	1	–	Power supply pin for the A/D converter. Connect this pin to power supply even if the A/D converter is not used.				
AVCC31	1	–	Power supply pin for the A/D converter. Connect this pin to power supply even if the A/D converter is not used.				
AVSS0	1	–	GND pin (0 V) for the D/A converter (0V)。Connect this pin to GND even if the A/D converter is not used.				
AVSS1	1	–	Power supply pin for a high-frequency oscillator: 1.5 V power supply				
CVCC15	1	–	Power supply pin for the A/D converter. Connect this pin to power supply even if the A/D converter is not used.				
CVSS	1	–	GND pin (0V) for a high-frequency oscillator				
DVCC15	6	–	Power supply pin: 1.5 V power supply				
DVCC30	3	–	Power supply pin: 3 V power supply				
DVCC31	2	–	Power supply pin: 3 V power supply				
DVCC32	1	–	Power supply pin: 3 V power supply				
DVCC33	1	–	Power supply pin: 3 V power supply				
DVCC34	3	–	Power supply pin: 3 V power supply				
DVSS	9	–	Power supply pin: GND pin (0V)				

Table 2.3 Pin Names and Functions (10/10)

2.4 Pin Names and Power Supply Pins

Pin name	Power supply	Pin name	Power supply
P0	DVCC30	PM	DVCC32
P1	DVCC30	PN	DVCC31
P2	DVCC30	PO	DVCC34
P3	DVCC30	PP	DVCC34
P4	DVCC30	PQ	DVCC34
P5	DVCC30	*NMI	DVCC15
P6	DVCC30	PCST4~0	DVCC34
P7	AVCC30	DCLK	DVCC34
P8	AVCC30	*EJE	DVCC34
P9	AVCC31	*TRST	DVCC34
PA	AVCC31	TDI	DVCC34
PB	DVCC31	TDO	DVCC34
PC	DVCC31	TMS	DVCC34
PD	DVCC31	TCK	DVCC34
PE	DVCC31	*DINT	DVCC34
PF	DVCC32	*RESET	DVCC34
PG	DVCC32	PLLSEL	DVCC15
PH	DVCC31	X1, X2	CVCC15
PI	DVCC31	BUSMD	DVCC15
PJ	DVCC32	BW0	DVCC34
PK	DVCC33	BW1	DVCC15
PL	DVCC33		

Table 2.4 Pin Names and Power Supplies

2.5 Pin Numbers and Power Supply Pins

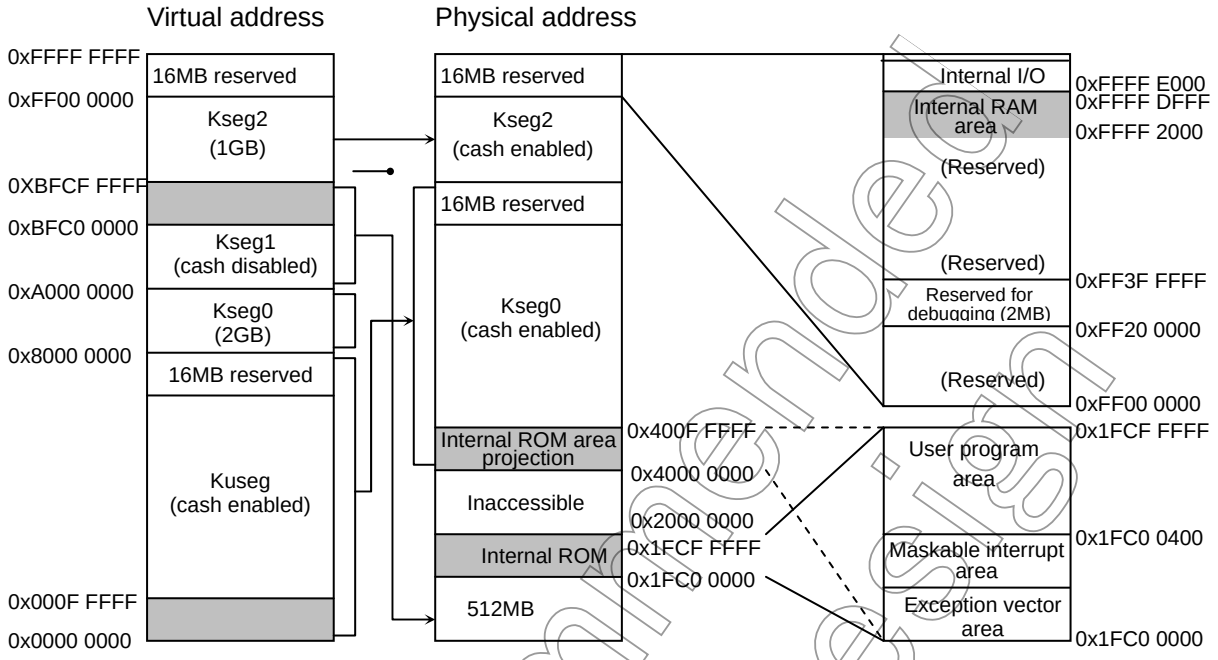
Power supply	Pin number	Voltage range
DVCC15	M8, M14, N11, H12 H11, N10	1.35V~1.65V
DVCC30 DVCC31 DVCC32 DVCC33	G9, G13, J8, K8, L8, P11, P12	1.65V~3.3V
DVCC34	G10, G11, G12	2.7V~3.3V
AVCC	J13, M13	2.7V~3.3V
CVCC15	N14	1.35V~1.65V

Table 2.5 Pin Numbers and Power Supplies

3. Memory Map

Fig. 3.1 shows the memory map of the TMP19A61.

1）1024KB



2）512KB

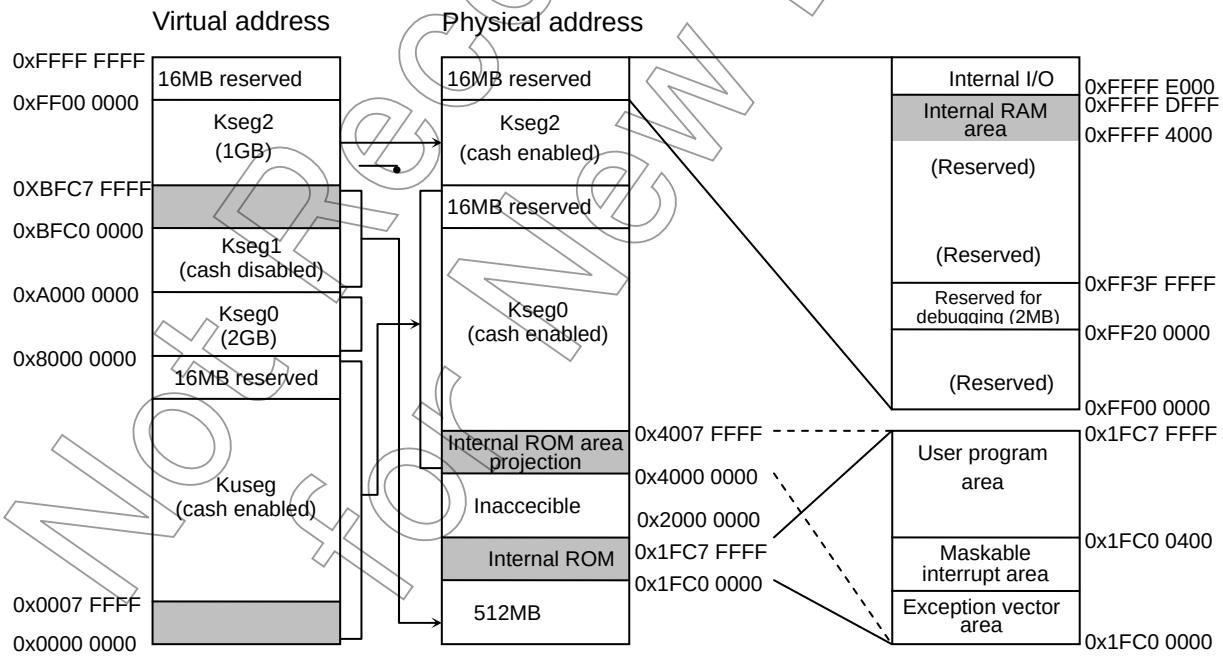


Fig. 3.1 Memory Map

(Note 1) **The internal ROM is mapped to:**
0x1FC0_0000~0x1FCF_FFFF (1024KB)
0x1FC0_0000~0x1FC7_FFFF (512KB)

The internal RAM is mapped to:
0xFFFF_2000~0xFFFF_DFFF (48KB)
0xFFFF_4000~0xFFFF_DFFF (40KB)

(Note 2) **For the TMP19A61, a physical space of only 16 MB is available as external address space to be accessed. It is possible to place this 16-MB physical address space in a chip select area of your choice inside the 3.5-GB physical address space of the CPU. However, access to internal I/O space and reserved areas are prioritized and access to external space is disabled.**

(Note 3) **Do not place an instruction in the last four words of a physical area.**
Internal ROM (1024KB): 0x1FCF_FFF0 ~ 0x1FCF_FFFF
Internal ROM (512KB): 0x1FC7_FFF0 ~ 0x1FC7_FFFF
The last four words of an area where memory is mounted for external ROM extension (this varies depending on the system of the user).

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

The letter x in equations represents the cycle period of the fsys clock selected through the programming of the SYSCR1 <SYSCK> bit. The x value may vary if clock gear or low-speed oscillator is used. All relevant values in this chapter are calculated with the high-speed (fc) system clock (SYSCR1.<SYSCK> = 0) and a clock gear factor of 1/1 (SYSCR1.GEAR[1:0] = 00).

Parameter		Symbol	Rating	Unit
Supply voltage		Vcc15(Core)	− 0.3~3.0	V
		Vcc3(I/O)	− 0.3~3.9	
		AVCC(A/D)	− 0.3~3.9	
Input voltage		V_{IN}	− 0.3~V_{CC}+0.3	V
Low-level output current	Per pin	I_{OL}	5	mA
	Total	ΣI_{OL}	50	
High-level output current	Per pin	I_{OH}	-5	
	Total	ΣI_{OH}	50	
Power consumption (Ta = 85˚C)		PD	600	mW
Soldering temperature (10s)		T_{SOLDER}	260	˚C
Storage temperature		T_{STG}	-40~125	˚C
Operating Temperature		T_{OPR}	-20~85	˚C

V_{CC15}=DVCC15=CVCC15, V_{CC}3=DVCC3n (n=0~4),

AVCC=AVCC3m (m=1~2), V_{SS}=DVSS*=AVSS*=CVSS

Note: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blowup and/or burning.

4.2 DC Electrical Characteristics (1/4)

Ta=-20~85˚C (n=0~4, m=1, 2)

Parameter		Symbol	Rating	Min.	Typ. (Note 1)	Max.	Unit
Supply voltage CVCC15=DVCC15 CVSS=DVSS=0V		DVCC15	fosc = 8~13.5MHz fsys = 4MHz~54MHz PLLON、	1.35		1.65	V
		DVCC3n (n=0~4)	fsys = 4~54MHz	1.65		3.3	
Low-level input voltage	P7~PA	V_{IL1}	2.7V≤AVCC32≤AVCC31≤3.3V	−0.3		0.3AVCC31 0.3AVCC32	V
	Normal port	V_{IL2}	1.65V≤DVCC3n≤3.3V (n=0~4)			0.3DVCC3n	
			2.7V≤ DVCC34≤3.3V				
	Schmitt-Triggered port	V_{IL3}	1.65V≤DVCC3n≤3.3V(n=0~4)			0.2DVCC3n	
			2.7V≤ DVCC34≤ 3.3V			0.2DVCC3n	
			1.35V≤DVCC15≤1.65V			0.1DVCC15	
	X1	V_{IL5}	1.35V≤CVCC15≤1.65V			0.1CVCC15	

4.3 DC Electrical Characteristics (2/4)

Ta=-20~85˚C (n=0~4, m=1, 2)

Parameter		Symbol	Rating		Min.	Typ. (Note 1)	Max.	Unit
High-level input voltage	P7~PA	V_{IH1}	2.7V≤AVCC32≤AVCC31≤3.3V		0.7AVCC31 0.7AVCC32		DVCC3n+0.3 DVCC15+0.2 CVCC15+0.2	V
	Normal port	V_{IH2}	1.65V≤DVCC3n≤3.3V（n=0~3）		0.7DVCC3n			
			2.7V≤DVCC34≤3.3V					
	Schmitt-Triggered port	V_{IH3}	1.65V≤DVCC3n≤3.3V（n=0~3）		0.8DVCC3n			
			2.7V≤DVCC34≤3.3V					
			1.35V≤DVCC15≤1.65V		0.9DVCC15			
	X1	V_{IH4}	1.35V≤CVCC15≤1.65V		0.9CVCC15			
Low-level output voltage		V_{OL}	I_{OL} = 2mA	DVCC3n≥2.7V			0.4	V
			I_{OL} = 500μA	DVCC3n＜2.7V			0.2DVCC3n ≤0.4	
High-level output voltage		V_{OH}	I_{OH} = −2mA	DVCC3n≥2.7V	2.4			
			I_{OH} = −500μA	DVCC3n<2.7V	0.8DVCC3n			

(Note 1) Ta=25˚C, DVCC15=1.5V, DVCC3n=3.0V, AVCC3m=3.3V, unless otherwise noted.

4.4 DC Electrical Characteristics (3/4)

Ta=-20~85˚C (n=0~4, m=1, 2)

Parameter	Symbol	Rating	Min.	Typ. (Note 1)	Max.	Unit
Input leakage current	I_{LI}	$0.0 \le V_{IN} \le$ DVCC15 $0.0 \le V_{IN} \le$ DVCC3n（n=0~4） $0.0 \le V_{IN} \le$ AVCC31 $0.0 \le V_{IN} \le$ AVCC32		0.02	±5	μA
Output leakage current	I_{LO}	$0.2 \le V_{IN} \le$ DVCC15−0.2 $0.2 \le V_{IN} \le$ DVCC3n−0.2（n=0~4） $0.2 \le V_{IN} \le$ AVCC31−0.2 $0.2 \le V_{IN} \le$ AVCC32−0.2		0.05	±10	
Power down voltage (@STOP)	V_{STOP} (DVCC15)		1.35		1.65	V
	V_{STOP2} (AVCC3)	V_{IL1} = 0.3AVCC31,32 V_{IH1} = 0.7AVCC31,32	2.7		3.3	
	V_{STOP3} (DVCC3)	V_{IL2} = 0.3DVCC3n, V_{IL3} = 0.1DVCC3n V_{IH2} = 0.7DVCC3n, V_{IH3} = 0.9DVCC3n （n=0~4）	1.65		3.3	
Pull-up resister at Reset	RRST	DVCC34 = 3.0V ± 0.3V	20	50	150	kΩ
Schmitt-Triggered port	VTH	1.65V≤DVCC3n≤3.3V（n=0~4） 1.35V≤DVCC15≤1.65V	0.3	0.6		V
Programmable pull-up/ pull-down resistor	PKH	DVCC3n = 1.65V~3.3V（n=0~3） DVCC34 = 2.7V~3.3V DVCC15 = 1.35V~1.65V	20	50	150	kΩ
Pin capacitance (Except power supply pins)	C_{IO}	Fc = 1MHz			10	pF

(Note 1) Ta=25˚C, DVCC15=1.5V, DVCC3=3.0V, AVCC3m=3.3V, unless otherwise noted.

4.5 DC Electrical Characteristics (4/4)

DVCC15=CVCC=1.5V±0.15V,
DVCC3n=3.0V±0.3V, AVCC3m=3.0V±0.3V,
Ta=-20~85˚C (n=0~4, m=1, 2)

Parameter	Symbol	Rating	Min.	Typ. (Note 1)	Max.	Unit
NORMAL(Note 2) Gear 1/1	I_{CC}	F_{sys}=54 MHz (f_{osc}=13.5 MHz, PLLON)		39	49	mA
IDLE(Doze)				18	28	
IDLE(Halt)				14	23	
STOP		DVCC15= CVCC15=1.35~1.65V DVCC3n=1.65~3.3V AVCC3m=2.7~3.3V		30	2000	μA

(Note 1) Ta=25˚C, DVCC15=1.5V, DVCC15x=1.5V, DVCC3n=3.0V, AVCC3m=3.3V, unless otherwise noted.

(Note 2) I_{CC} NORMAL

Measured with the CPU dhrystone operating and all the embedded peripheral I/O operating by the 4 system clock of external bus 16-bit width.

(Note 3) The currents flow through DVCC15, DVCC3n, CVCC15 and AVCC3m are included.

4.6 10-bit ADC Electrical Characteristics

DVCC15=CVCC15=1.35V~1.65V, CVCC3= DVCC3=AVCC3=VREFH=2.7V~3.3V,
AVCC=2.3V~2.7V, AVSS=DVSS, Ta=-20~85°C
AVCC3 load capacitance ≥3.3μF, VREFH load capacitance ≥3.3μF

Parameter		Symbol	Rating	Min	Typ	Max	Unit
Analog reference voltage (+)		VREFH		2.7	3.3	3.3	V
Analog reference voltage (–)		VREFL		AVSS	AVSS	AVSS	V
Analog input voltage		VAIN		VREFL		VREFH	V
Analog supply current	A/D conversion	IREF	DVSS = AVSS = VREFL		4.5	5.5	mA
	Non-A/D conversion		DVSS = AVSS = VREFL		±0.02	±5	μA
Supply current	A/D conversion	-	Non-IREF			3	mA
INL error		-	AIN resistance ≤1kΩ AIN load capacitance≥0.1μF Conversion time≥2.0μs @27MHz(ADCLK)		±2	±3	LSB
DNL error					±1	±2	
Offset error					±2	±4	
Full-scale error					±2	±4	
INL error		-	AIN resistance ≤10kΩ AIN load capacitance≥0.01μF Conversion time≥2.0μs @27MHz(ADCLK)		±2	±3	
DNL error					±1	±2	
Offset error					±2	±4	
Full-scale error					±2	±4	
INL error		-	AIN resistance ≤600Ω AIN load capacitance ≤30pF Conversion time ≥1.15μs @40MHz(ADCLK)		±2	±3	
DNL error					±1	±2	
Offset error					±2	±4	
Full-scale error					±2	±4	

(Note 1) 1LSB=(VREFH–VREFL)/ 1024[V]

4.7 AC Electrical Characteristics

［1］Separate bus mode

(1)DVCC15=CVCC15=1.35V~1.65V, DVCC3n=2.3V~3.3V

BUSCR<ALESEL>=”00”, 2 programmed wait state

No.	Parameter	Symbol	Equation		54 MHz (fsys)		Unit
			Min	Max	Min	Max	
1	System clock period (x)	t_{SYS}	18.5				ns
2	A0-23 valid to $\overline{RD}$ / $\overline{WR}$ /$\overline{HWR}$ asserted	t_{AC}	(1+ALE)x-20		17		ns
3	A0 – 23 hold after $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ negated	t_{CAR}	x-14		4.5		ns
4	A0 – 23valid to D0 – 15data in	t_{AD}		x(2+W+ALE)-42		50.5	ns
5	$\overline{RD}$ asserted to D0 – 15 data in	t_{RD}		x(1+W)-28		27.5	ns
6	$\overline{RD}$ pulse width low	t_{RR}	x(1+W)-10		45.5		ns
7	D0 – 15 hold after $\overline{RD}$ negated	t_{HR}	0		0		ns
8	$\overline{RD}$ negated to A0 – 23 output	t_{RAE}	x-15		3.5		ns
9	$\overline{WR}$ /$\overline{HWR}$ pulse width low	t_{WW}	x(1+W)-10		45.5		ns
10	$\overline{WR}$ or $\overline{HWR}$ asserted to D0-15 valid	t_{DO}		12.3		12.3	ns
11	D0-15 valid to $\overline{WR}$ /$\overline{HWR}$ negated	t_{DW}	x(1+W)-18		37.5		ns
12	D0 – 15 hold after $\overline{WR}$ /$\overline{HWR}$ rising	t_{WD}	x–15		3.5		ns
13	A0 - 23 valid to $\overline{WAIT}$ input	t_{AW}		x+(ALE)x+(w-1)x-30		25.5	ns
14	$\overline{WAIT}$ hold after $\overline{RD}$ / $\overline{WR}$ /$\overline{HWR}$	t_{CW}	x(TW-3)-1	x(TW-1)-30	17.5	25.5	ns

(Note) No. 1 to 14:

Internal 2 wait insertion, ALE “1” Clock, @54MHz

TW = W + 2N,

ALE=ALE output width

No. 21

(2W+2N)

TW = 2 + 2*1 = 4

AC measurement conditions:

Output levels: High = 0.8DVCC33 V/Low 0.2DVCC33 V, CL = 30 pF

Input levels:High = 0.7DVCC33 V/Low 0.3DVCC33 V

(2) DVCC15=CVCC15=1.35V~1.65V, DVCC3n=1.65V~1.95V

BUSCR<ALESEL>="00", 2 programmed wait state

No.	Parameter	Symbol	Equation		54 MHz (fsys)		Unit
			Min	Max	Min	Max	
1	System clock period (x)	t_{SYS}	18.5				ns
2	A0-23 valid to $\overline{RD}$ / $\overline{WR}$ /$\overline{HWR}$ asserted	t_{AC}	(1+ALE)x-20		17		ns
3	A0 – 23 hold after $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ negated	t_{CAR}	x-7		11.5		ns
4	A0 – 23 valid to D0 – 15 data in	t_{AD}		x(2+W+ALE)-42		50.5	ns
5	$\overline{RD}$ asserted to D0 – 15 data in	t_{RD}		x(1+W)-28		27.5	ns
6	$\overline{RD}$ pulse width low	t_{RR}	x(1+W)-10		45.5		ns
7	D0 – 15 hold after $\overline{RD}$ negated	t_{HR}	0		0		ns
8	$\overline{RD}$ negated to next A0 – 23 output	t_{RAE}	x-15		3.5		ns
9	$\overline{WR}$ /$\overline{HWR}$ pulse width low	t_{WW}	x(1+W)-10		45.5		ns
10	$\overline{WR}$ or $\overline{HWR}$ asserted to D0-15 valid	t_{DO}		12.3		12.3	ns
11	D0-15 valid to $\overline{WR}$ /$\overline{HWR}$ negated	t_{DW}	x(1+W)-18		37.5		ns
12	D0 – 15 hold after $\overline{WR}$ /$\overline{HWR}$ negated	t_{WD}	x–15		3.5		ns
13	A0 – 23 valid to $\overline{WAIT}$ input	t_{AW}		x+(ALE)x+(w-1)x-30		25.5	ns
14	$\overline{WAIT}$ hold after $\overline{RD}$ / $\overline{WR}$ /$\overline{HWR}$	t_{CW}	x(TW-3)-7	x(TW-1)-40	13.5	15.5	ns

(Note)

No. 1 to 14:

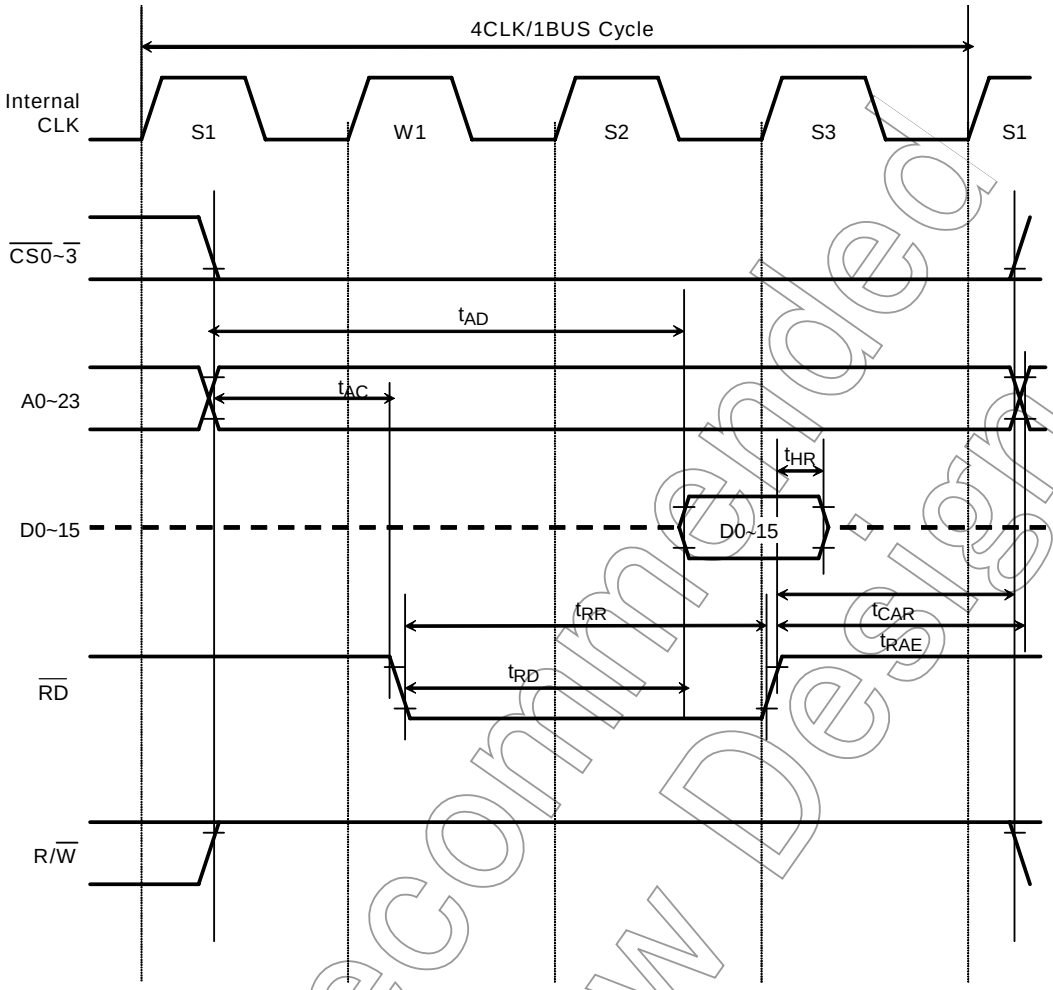
Internal 2 wait insertion, ALE "1" Clock, @54MHz
TW = W + 2N,
ALE=ALE output width
No. 21
(2W+2N)

TW = 2 + 2*1 = 4

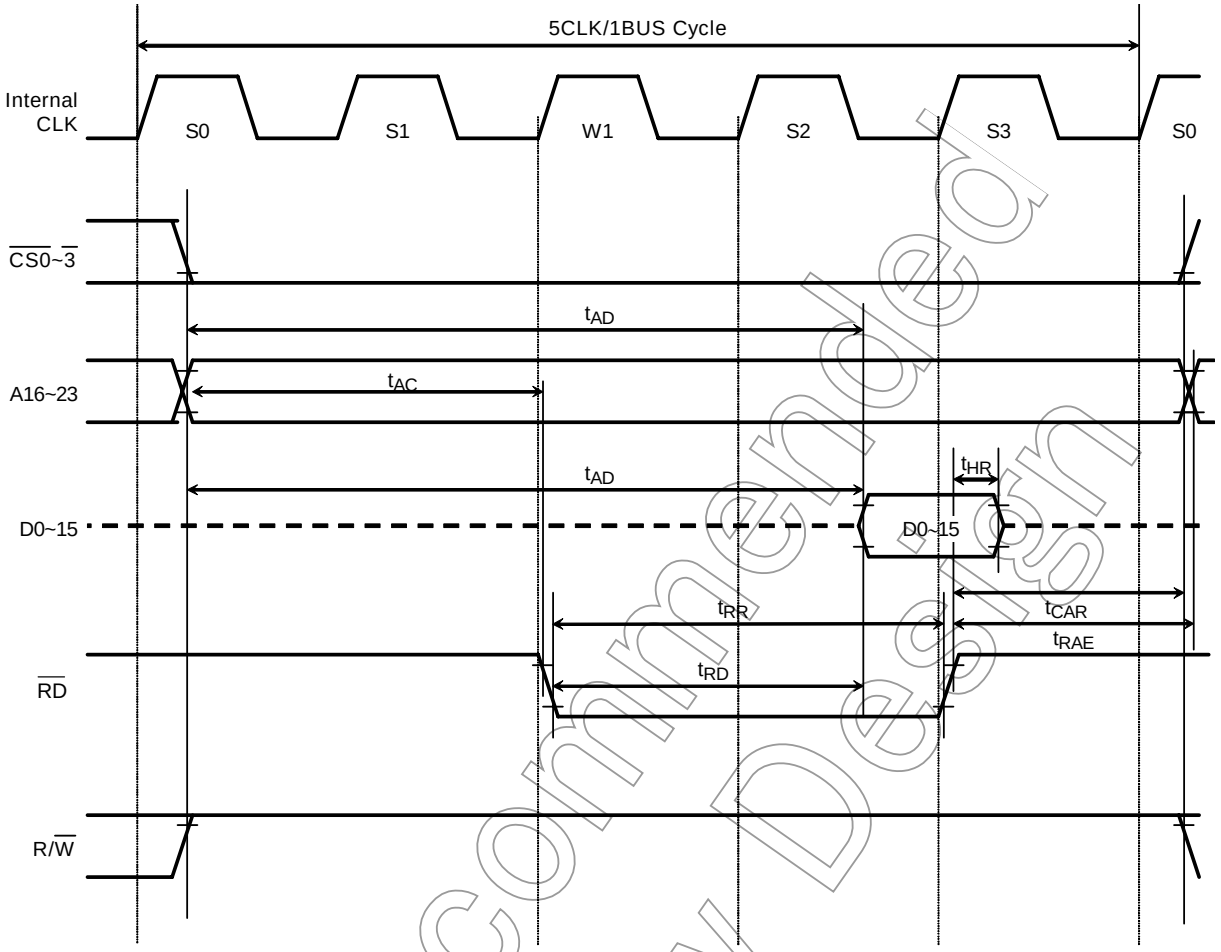
AC measurement conditions:

Output levels: High = 0.8DVCC33 V/Low 0.2DVCC33 V, CL = 30 pF
Input levels: High = 0.7DVCC33 V/Low 0.3DVCC33 V

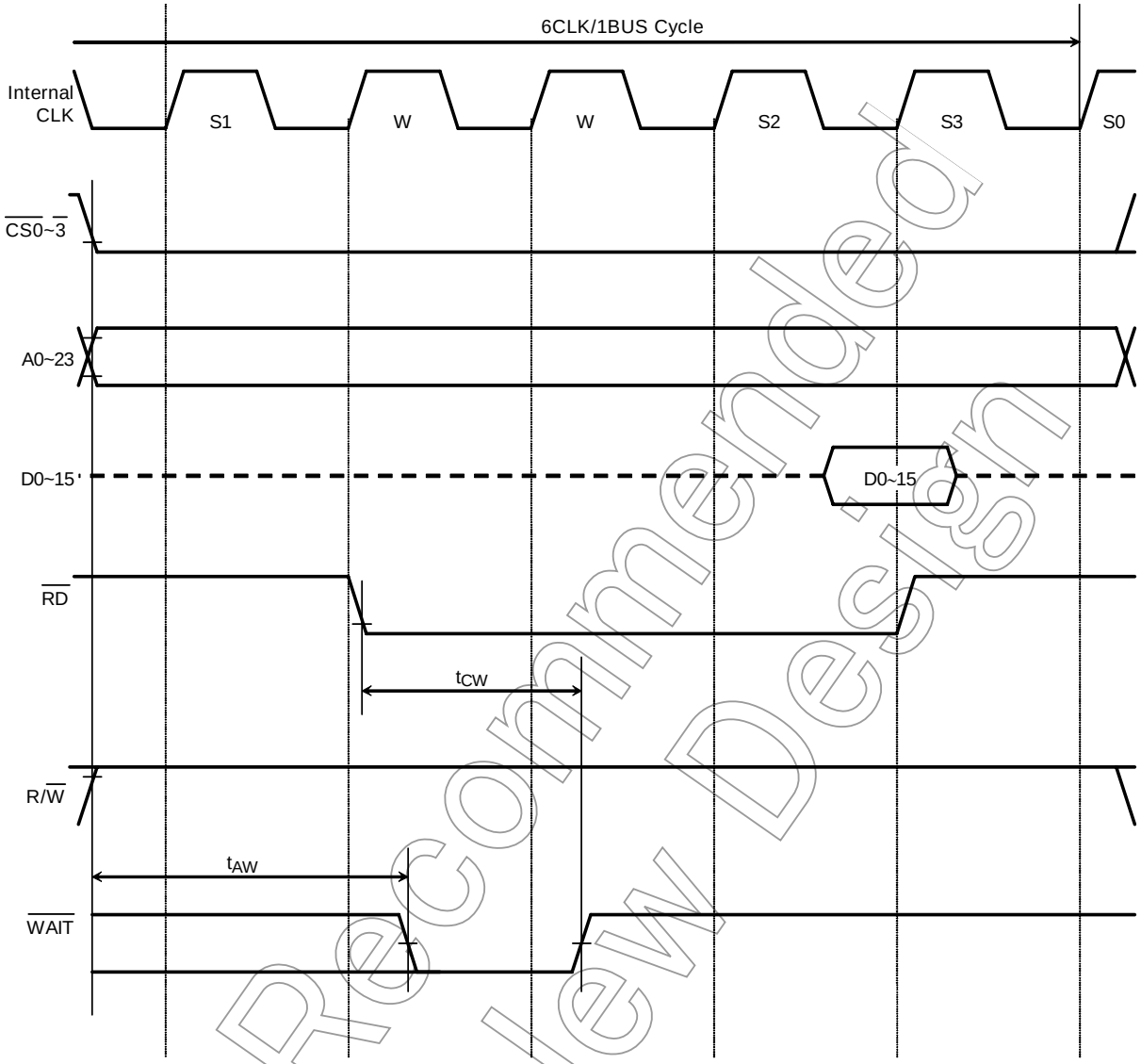
(1) Read cycle timing (BUSCR<ALESEL>="00", 1 programmed wait state)



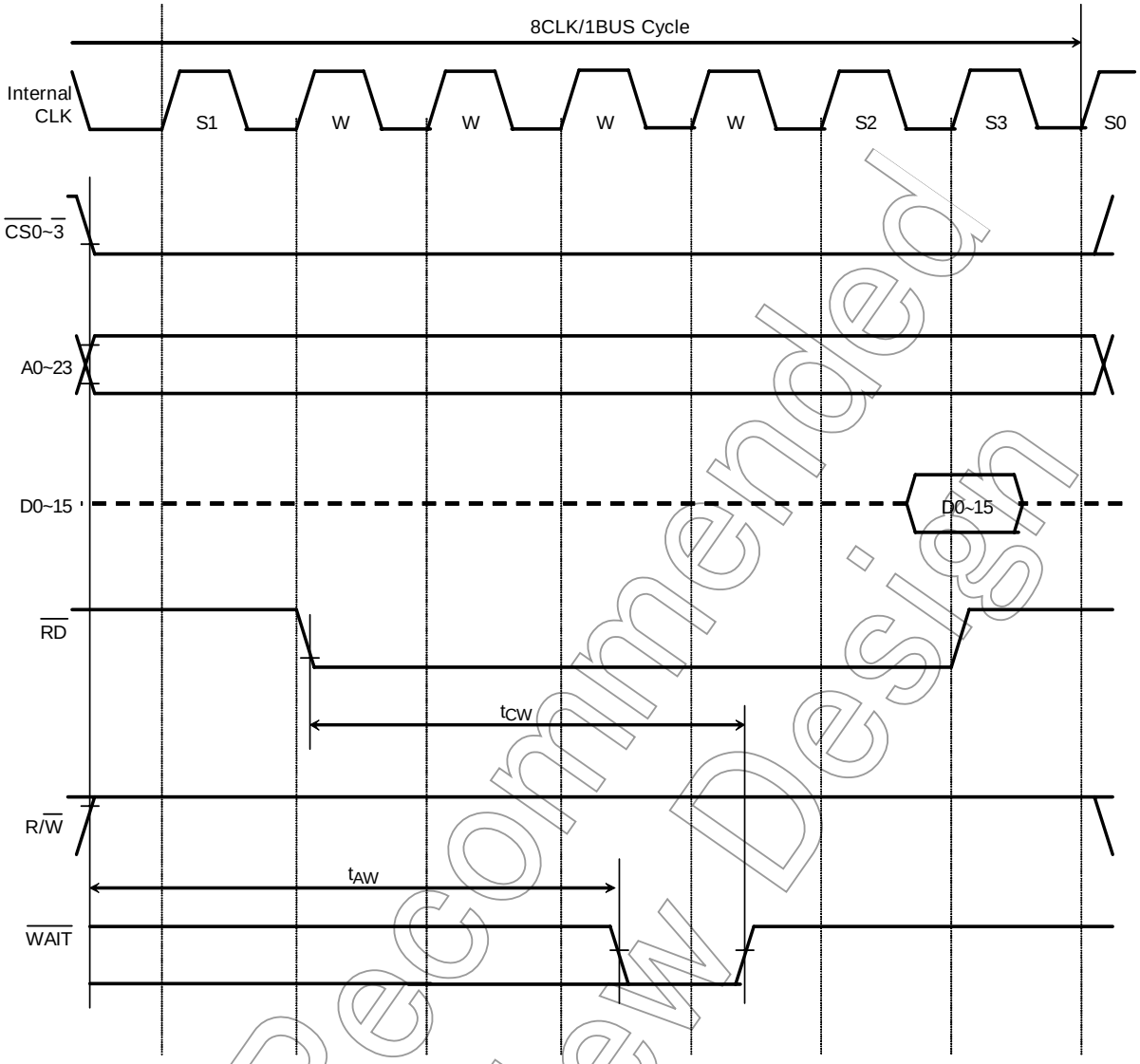
(2) Read timing (BUSCR<ALESEL>="01", 1 programmed wait state)



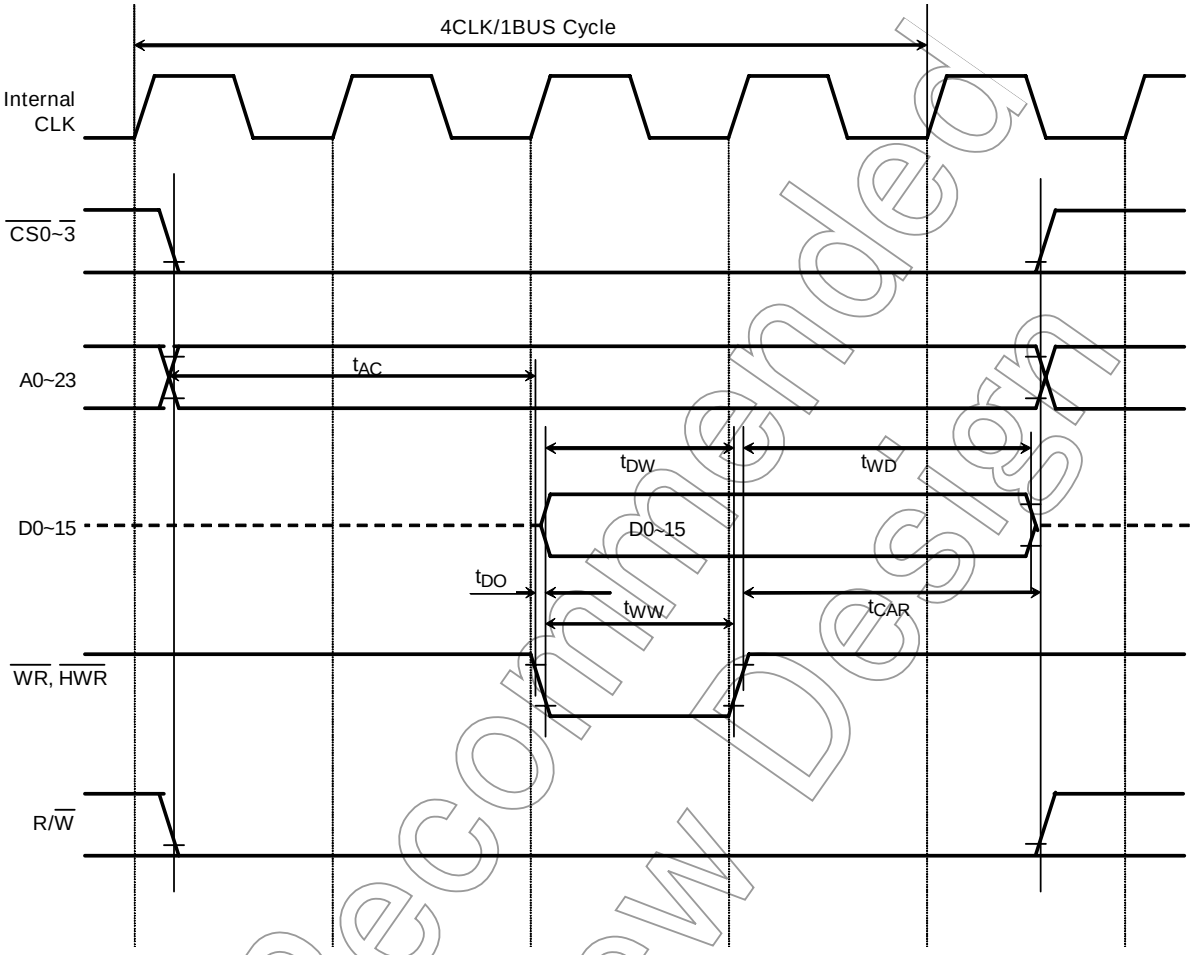
(3) Read timing (BUSCR<ALESEL>="01", 2 wait (1+N externally generated wait states with N=1)



(4) Read timing (BUSCR<ALESEL>="01", 4 wait (3+N externally generated wait states with N=1))



(5) Write timing (BUSCR<ALESEL>="01", 0 wait state)



［2］ Multiplex bus mode

(1) DVCC15=CVCC15=1.35V~1.65V, DVCC3n=2.3V~3.3V

1) ALE=1 clock cycle, 2 programmed wait state

No.	Parameter	Symbol	Equation		54 MHz (fsys)		Unit
			Min	Max	Min	Max	
1	System clock period (x)	t_{SYS}	18.5				ns
2	A0-15 valid to ALE low	t_{AL}	(ALE)x-12		6.5		ns
3	A0-15 hold after ALE low	t_{LA}	x-8		10.5		ns
4	ALE pulse width high	t_{LL}	(ALE)x-6		12.5		ns
5	ALE low to $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ asserted	t_{LC}	x-8		10.5		ns
6	$\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ negated to ALE high	t_{CL}	x-15		3.5		ns
7	A0-15 valid to $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ asserted	t_{ACL}	2x-20		17.0		ns
8	A16-23 valid to $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ asserted	t_{ACH}	2x-20		17.0		ns
9	A16-23 hold after $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ negated	t_{CAR}	x-14		4.5		ns
10	A0-15 valid to D0-15 data in	t_{ADL}		x(2+W+ALE)-42		50.5	ns
11	A16-23 valid to D0-15 data in	t_{ADH}		x(2+W+ALE)-42		50.5	ns
12	$\overline{RD}$ asserted to D0-15 data in	t_{RD}		x(1+W)-28		27.5	ns
13	$\overline{RD}$ pulse width low	t_{RR}	x(1+W)-10		45.5		ns
14	D0-15 hold after $\overline{RD}$ negated	t_{HR}	0		0		ns
15	$\overline{RD}$ negated to next A0-15 output	t_{RAE}	x-15		3.5		ns
16	$\overline{WR}$ / $\overline{HWR}$ pulse width low	t_{WW}	x(1+W)-10		45.5		ns
17	D0-15 valid to $\overline{WR}$ or $\overline{HWR}$ negated	t_{DW}	x(1+W)-18		37.5		ns
18	D0-15 hold after $\overline{WR}$ or $\overline{HWR}$ negated	t_{WD}	x-15		3.5		ns
19	A16-23 valid to $\overline{WAIT}$ input	t_{AWH}		x+(ALE)x+(W-1)x-30		25.5	ns
20	A0-15 valid to $\overline{WAIT}$ input	t_{AWL}		x+(ALE)x+(W-1)x-30		25.5	ns
21	$\overline{WAIT}$ hold after $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$	t_{CW}	x(TW-3)-1	x(TW-1)-30	17.5	25.5	ns

(Note)

No. 1 to 21:

Internal 2 wait insertion, ALE “1” Clock, @54MHz

TW = W + 2N,

ALE=ALE output width

TW = 2 + 2*1 = 4

AC measurement conditions:

Output levels: High = 0.8DVCC33 V/Low 0.2DVCC33 V, CL = 30 pF

Input levels: High = 0.7DVCC33 V/Low 0.3DVCC33 V

(2) DVCC15=CVCC15=1.35V~1.65V, DVCC3n=1.65V~1.95V

ALE=1 clock cycle, 2 programmed wait state

No.	Parameter	Symbol	Equation		54 MHz (fsys)		Unit
			Min	Max	Min	Max	
1	System clock period (x)	t_{SYS}	18.5				ns
2	A0-15 valid to ALE low	t_{AL}	(ALE)x-12		6.5		ns
3	A0-15 hold after ALE low	t_{LA}	x-8		10.5		ns
4	ALE pulse width high	t_{LL}	(ALE)x-6		12.5		ns
5	ALE low to $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ asserted	t_{LC}	x-8		10.5		ns
6	$\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ negated to ALE high	t_{CL}	x-15		3.5		ns
7	A0-15 valid to $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ asserted	t_{ACL}	2x-20		17.0		ns
8	A16-23 valid to $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ asserted	t_{ACH}	2x-20		17.0		ns
9	A16-23 hold after $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$ negated	t_{CAR}	x-7		11.5		ns
10	A0-15 valid to D0-15 data in	t_{ADL}		x(2+W+ALE)-42		50.5	ns
11	A16-23 valid to D0-15 data in	t_{ADH}		x(2+W+ALE)-42		50.5	ns
12	$\overline{RD}$ asserted to D0-15 data in	t_{RD}		x(1+W)-28		27.5	ns
13	$\overline{RD}$ pulse width low	t_{RR}	x(1+W)-10		45.5		ns
14	D0-15 hold after $\overline{RD}$ negated	t_{HR}	0		0		ns
15	$\overline{RD}$ negated to next A0-15 output	t_{RAE}	x-15		3.5		ns
16	$\overline{WR}$ / $\overline{HWR}$ pulse width low	t_{WW}	x(1+W)-10		45.5		ns
17	D0-15 valid to $\overline{WR}$ / $\overline{HWR}$ negated	t_{DW}	x(1+W)-18		37.5		ns
18	D0-15 hold after $\overline{WR}$ / $\overline{HWR}$ negated	t_{WD}	x-15		3.5		ns
19	A16-23 valid to $\overline{WAIT}$ input	t_{AWH}		x+(ALE)x+(W-1)x-30		25.5	ns
20	A0-15 valid to $\overline{WAIT}$ input	t_{AWL}		x+(ALE)x+(W-1)x-30		25.5	ns
21	$\overline{WAIT}$ hold after $\overline{RD}$ / $\overline{WR}$ or $\overline{HWR}$	t_{CW}	x(TW-3)-7	x(TW-1)-40	13.5	15.5	ns

(Note)

No. 1 to 21:

Internal 2 wait insertion, ALE “1” Clock, @54MHz

TW = W + 2N,

ALE=ALE output width

No. 21

(2W+2N)

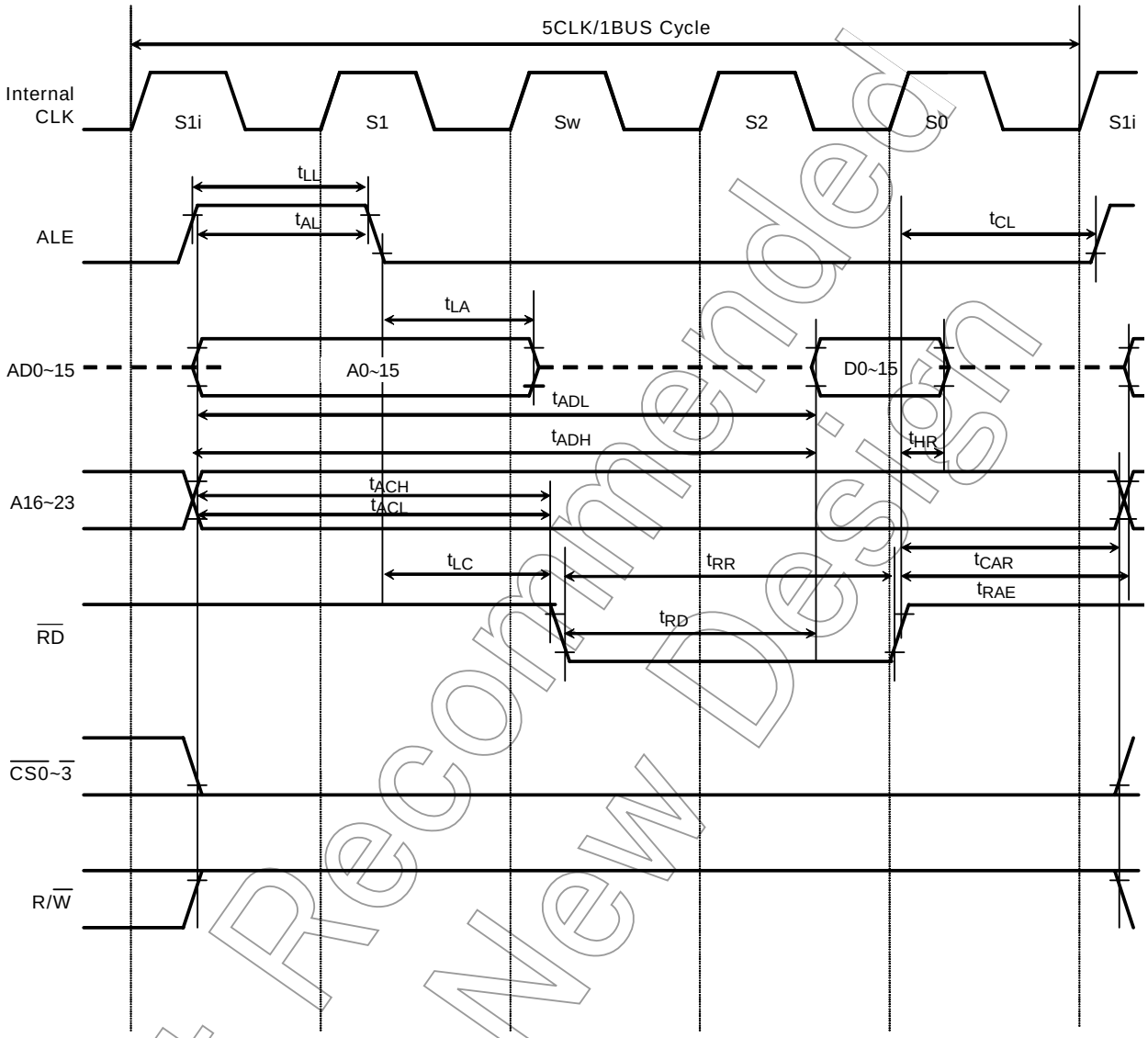
TW = 2 + 2*1 = 4

AC measurement conditions:

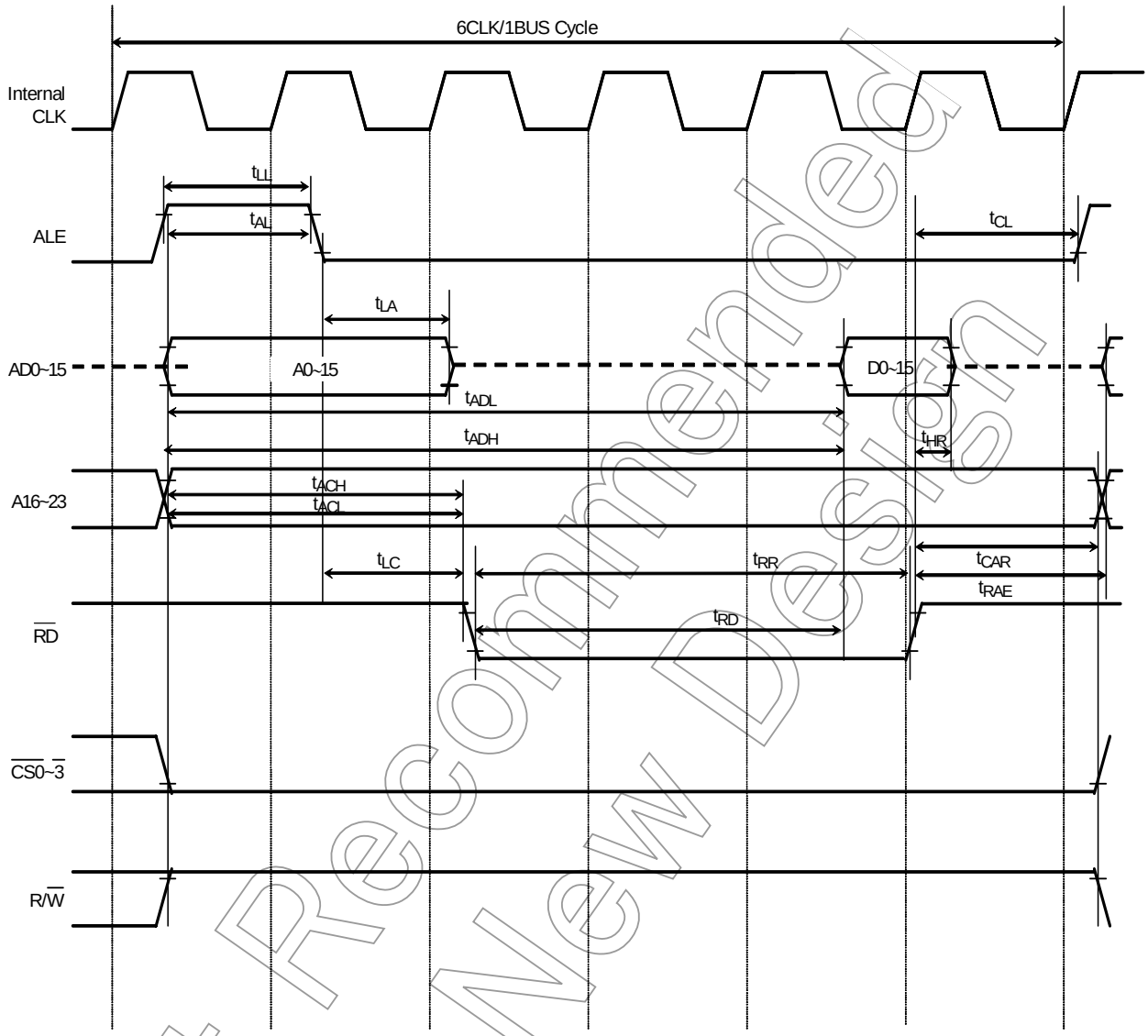
Output levels: High = 0.8DVCC33 V/Low 0.2DVCC33 V, CL = 30 pF

Input levels: High = 0.7DVCC33 V/Low 0.3DVCC33 V

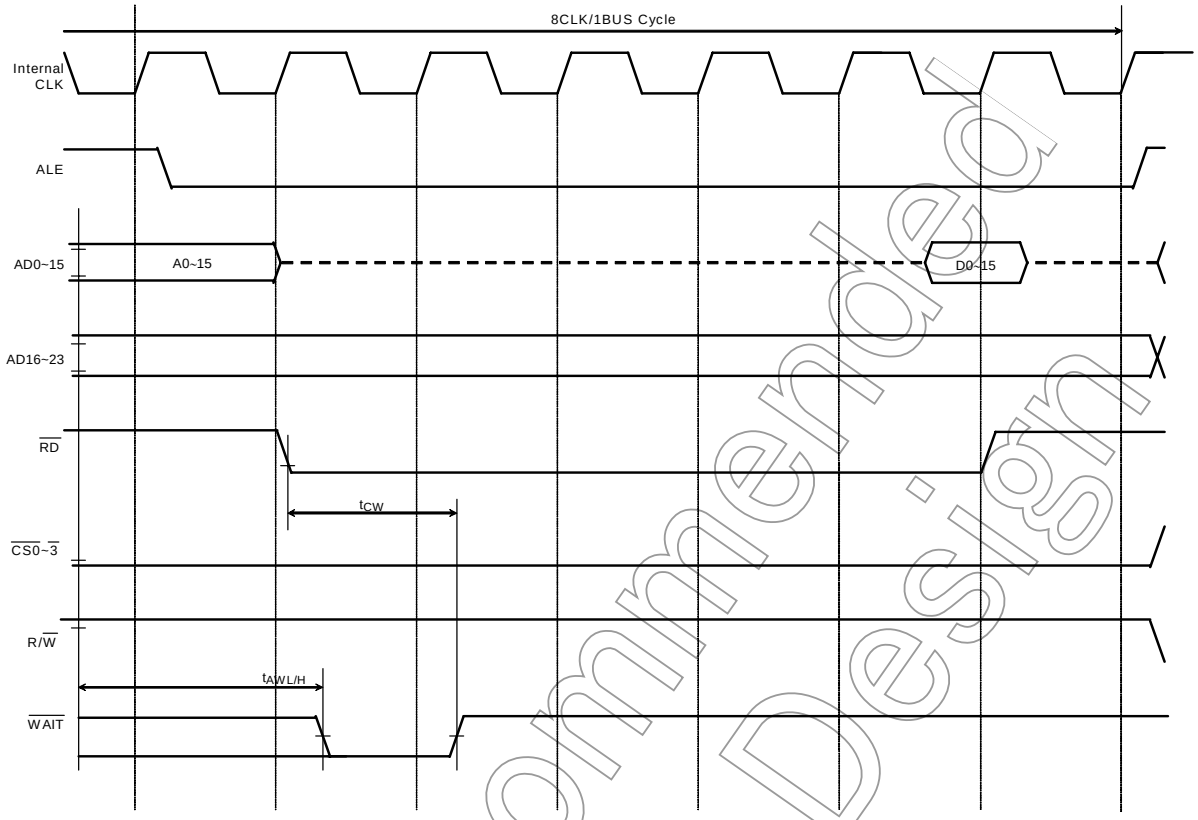
(1) Read timing (ALE=1 clock cycle, 1programmed wait state)



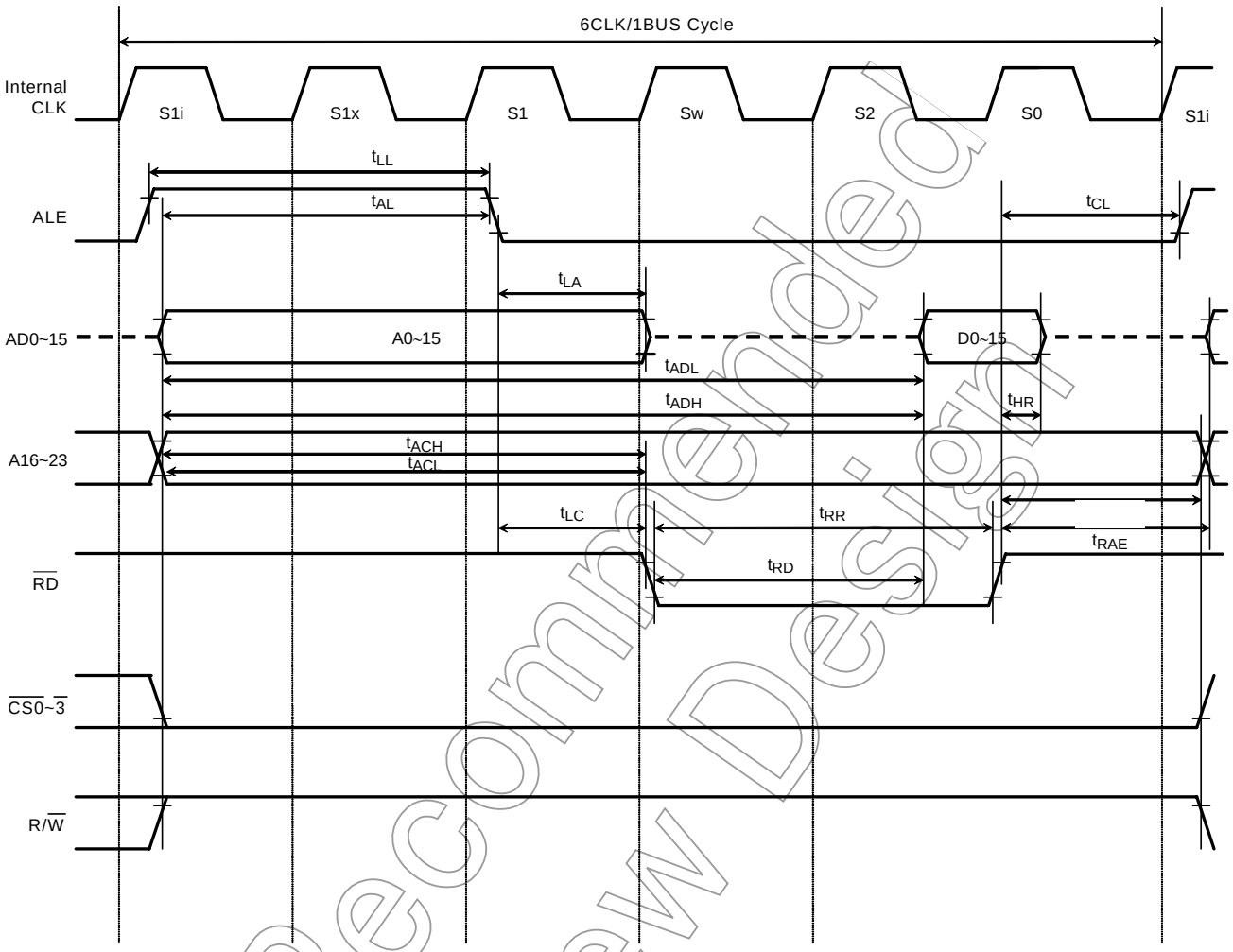
(2) Read timing (ALE=1 clock cycle, 2 programmed wait state)



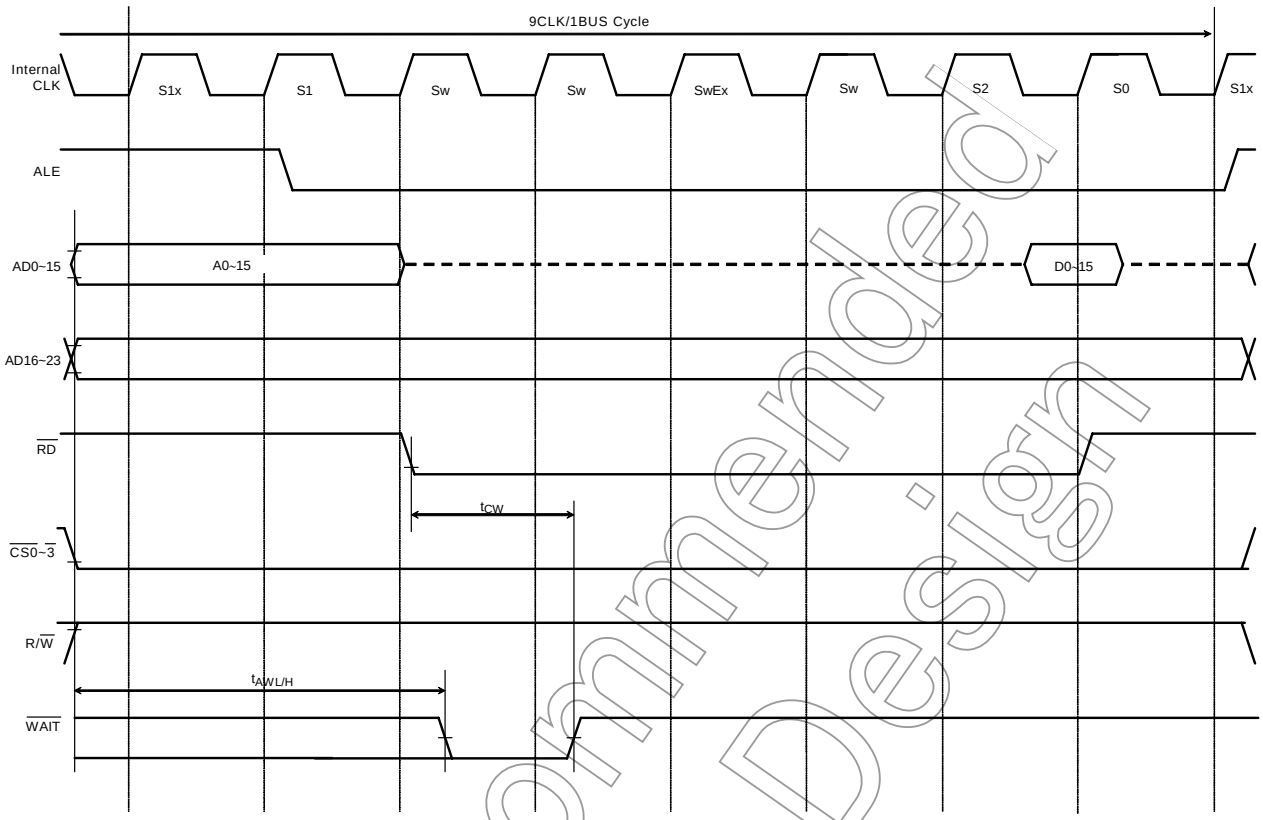
(3) Read timing (ALE = 1 clock cycle, 4 externally generated wait states (2+2N) with N=1



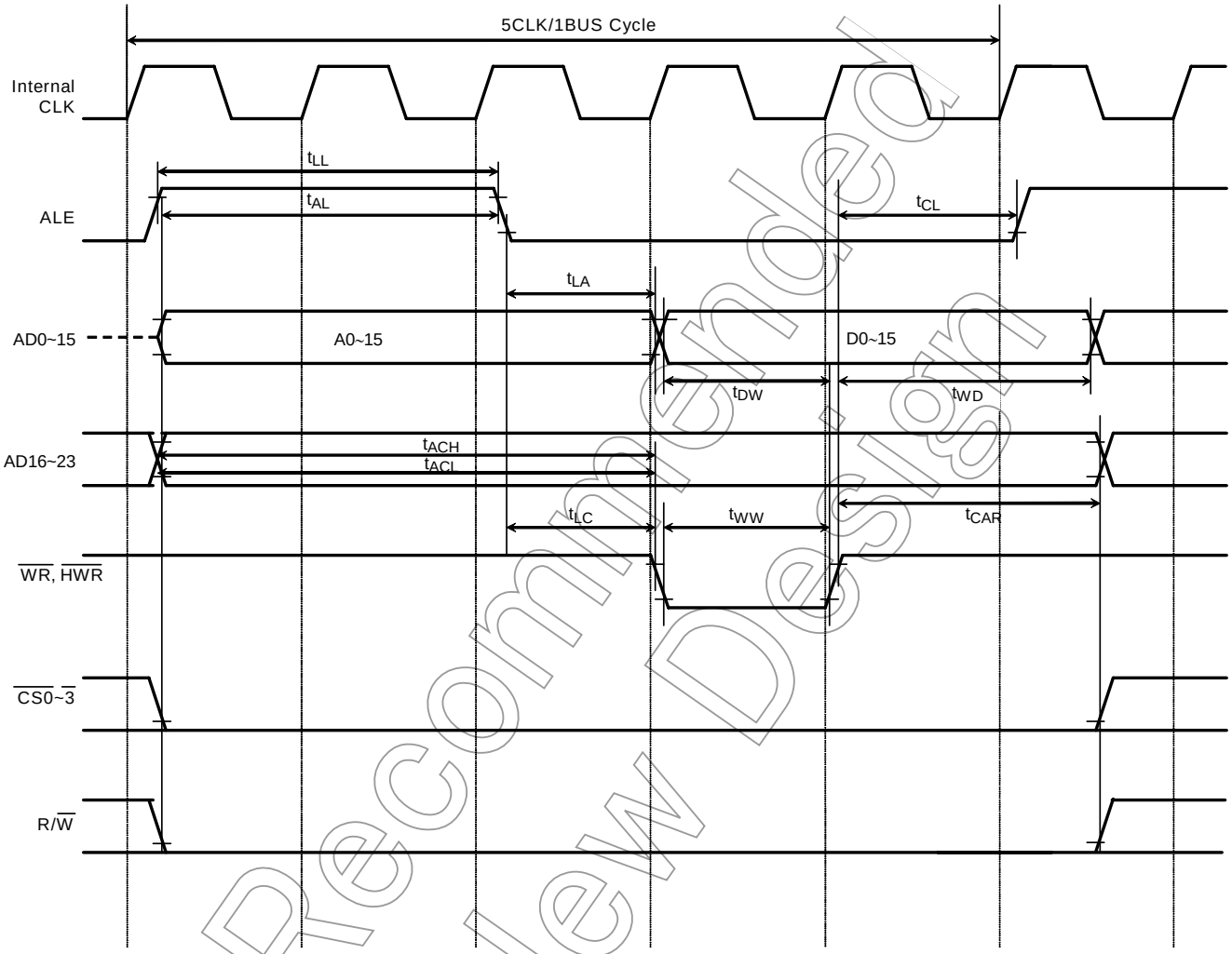
(4) Read timing (ALE = 2 clock cycle, 1programmed wait state)



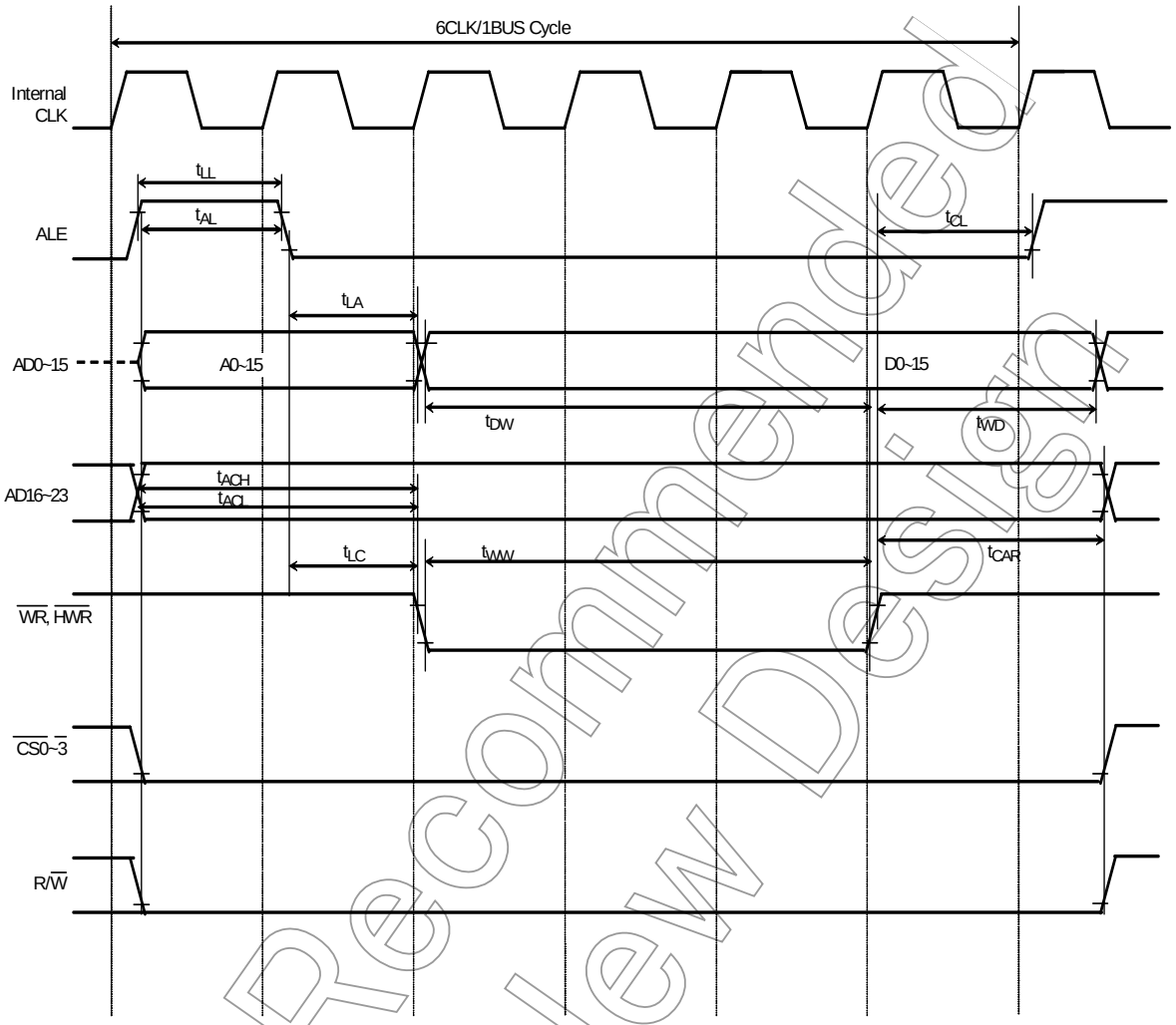
(5) Read timing (ALE = 2clock cycles, 4 externally generated wait states (2+2N) with N=1



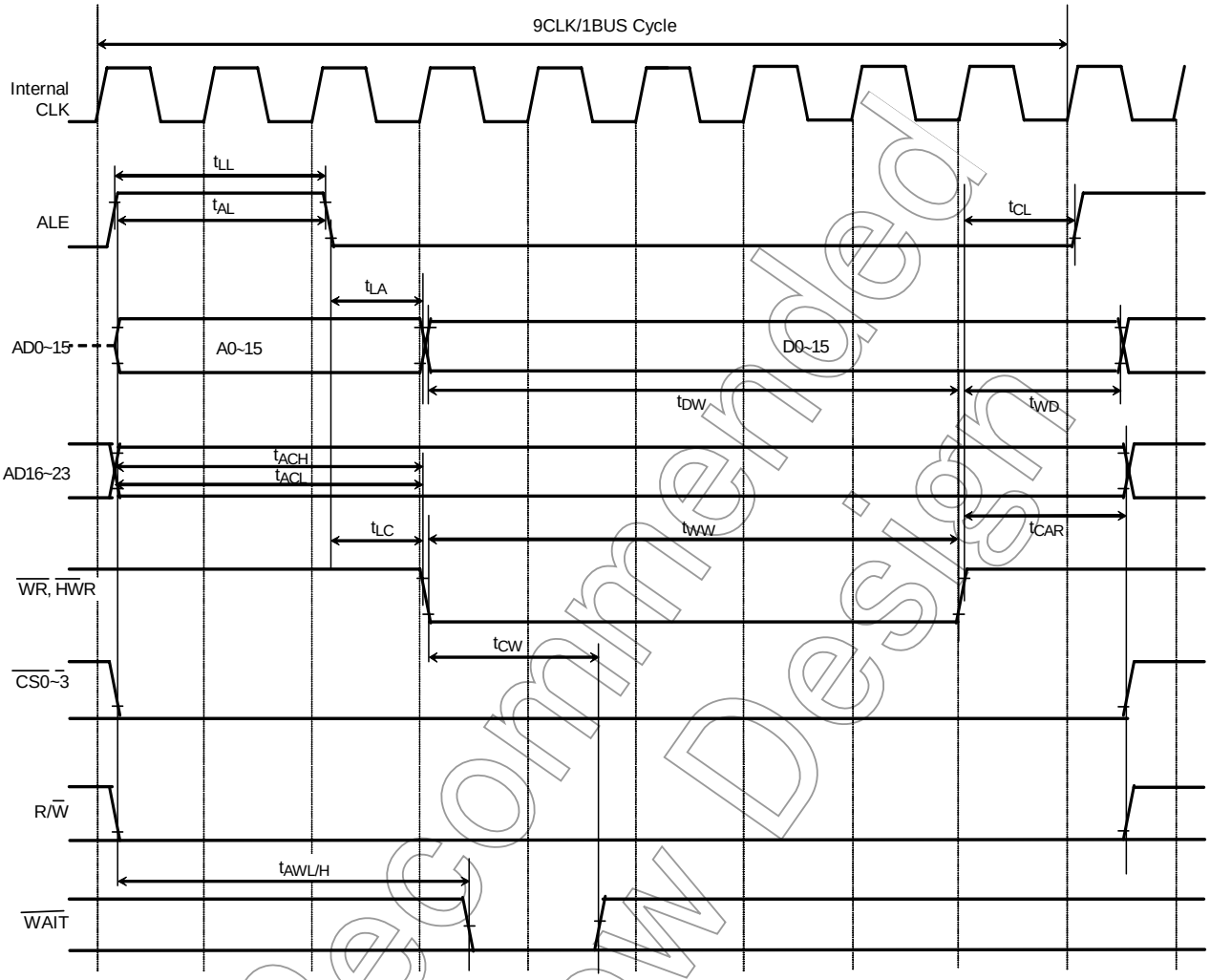
(6) Write timing (ALE = 2 clock timing, 0 wait state)



(7) Write timing (ALE = 1 clock cycle, 2 programmed wait state)



(8) Write timing (ALE = 2 clock cycle, 4 externally generated wait states (2+2N) with N=1)

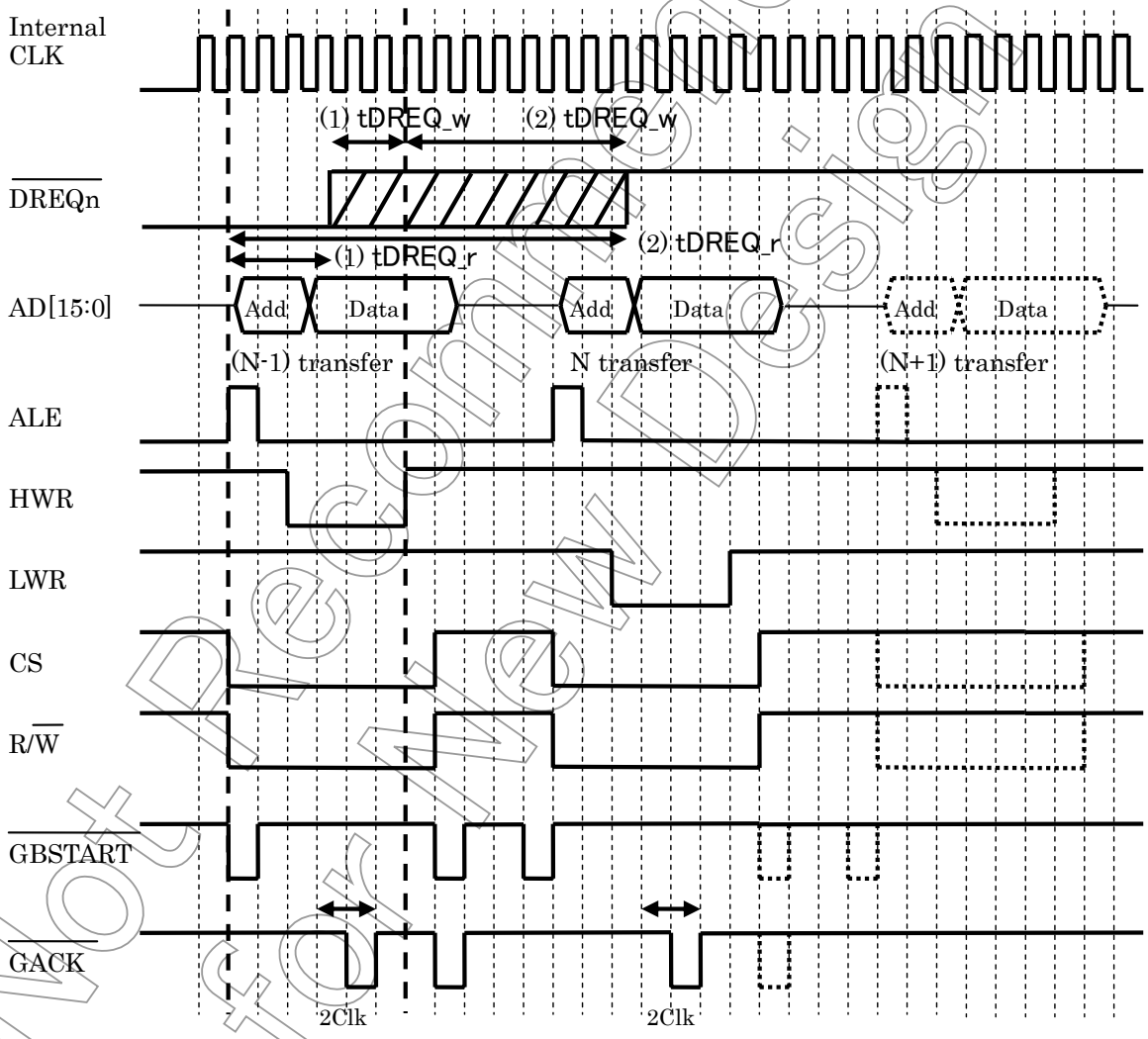


4.8 Transfer with DMA Request

The following shows an example of a transfer between the on-chip RAM and an external device in multiplex bus mode.

- 16-bit data bus width, non-recovery time
- Level data transfer mode
- Transfer size of 16 bits, device port size (DPS) of 16 bits
- Source/destination: on-chip RAM/external device

The following shows transfer operation timing of the on-chip RAM to an external bus during write operation (memory-to-memory transfer).



(1) Indicates the condition under which Nth transfer is performed successfully.
(2) Indicates the condition under which (N+1)th transfer is not performed.

(1) DVCC15=CVCC15=1.35V~1.65V, AVCC3m=2.7V~3.3V
DVCC33=2.3V~3.3V, DVCC30/31/32=1.65V~3.3V, Ta= -20~85°C (m=1~2)
DVCC34 = 2.7V~3.3V

No.	Parameter	Symbol	Equation		54 MHz (fsys)		Unit
			①Min	②Max	Min	Max	
2	$\overline{RD}$ asserted to $\overline{DREQn}$ negated (external device to on-chip RAM transfer)	tDREQ_r	(W+1)x	(2W+ALE+8)x-51	37	152.5	ns
3	$\overline{WR}$ / $\overline{HWR}$ rising to $\overline{DREQn}$ negated (on-chip RAM to external device transfer)	tDREQ_w	-(W+2)x	(5+WAIT)x-51.8	-55.5	59.2	ns

(2) DVCC15=CVCC15=1.35V~1.65V, AVCC3m =2.7V~3.3V
DVCC33=1.65V~1.95V, DVCC30/31/32=1.65V~3.3V, Ta=-20~85°C (m=1~2)
DVCC34 = 2.7V~3.3V

No.	Parameter	Symbol	Equation		54 MHz (fsys)		Unit
			①Min	②Max	Min	Max	
2	$\overline{RD}$ asserted to $\overline{DREQn}$ negated (external device to on-chip RAM transfer)	tDREQ_r	(W+1)x	(2W+ALE+8)x-56	37	147.5	ns
3	$\overline{WR}$ / $\overline{HWR}$ rising to $\overline{DREQn}$ negated (on-chip RAM to external device transfer)	tDREQ_w	-(W+2)x	(5+WAIT)x-56.8	-55.5	54.2	ns

W: number of wait
Ex.)
2 External wait +2N wait (N=1)
W=4
ALE: 1 is substituted for it at 1 clock cycle. 2 is substituted for it at 2 clock cycles.
The equations shown in the above table are calculated provided W=1 and ALE=1.

4.9 Serial Channel Timing

(1) I/O Interface mode (DVCC3=1.65V~3.3V)

In the table below, the letter x represents the fsys cycle period, which varies depending on the programming of the clock gear function.

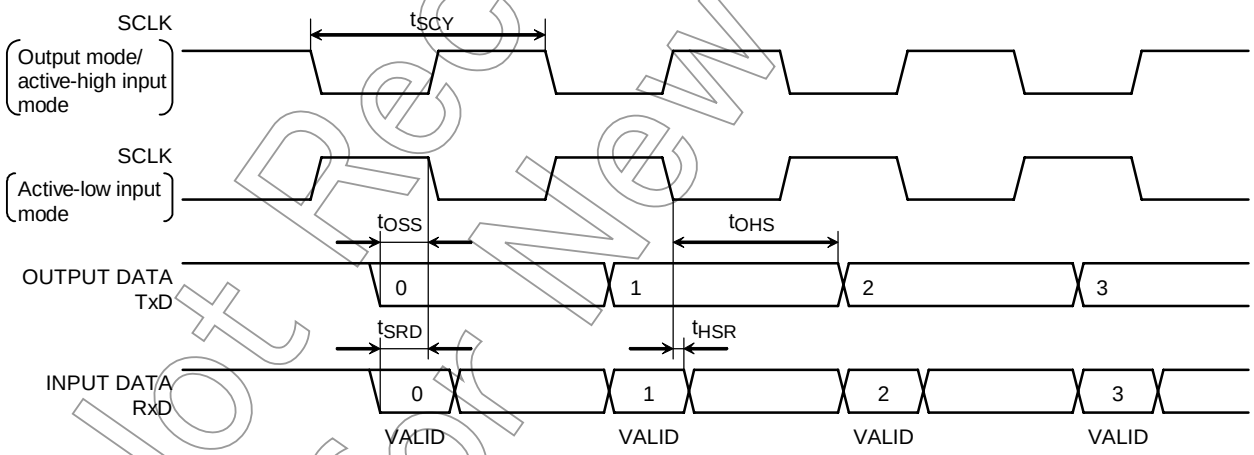
① SCLK input mode (SIO0~SIO8)

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
SCLK period	t_{SCY}	12x		222		ns
TxD data to SCLK rise or fall*	t_{OSS}	2x-35		2		ns
TxD data hold after SCLK rise or fall*	t_{OHS}	8x-15		133		ns
RxD data valid to SCLK rise or fall*	t_{SRD}	30		30		ns
RxD data hold after SCLK rise or fall*	t_{HSR}	2x+29		66		ns

*SCLK rise or fall: Measured relative to the programmed active edge of SCLK.

② SCLK output mode (SIO0~SIO8)

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
SCLK period (programmable)	t_{SCY}	8x		222		ns
TxD data to SCLK rise	t_{OSS}	4x-14		60		ns
TxD data hold after SCLK rise	t_{OHS}	4x-14		60		ns
RxD data valid to SCLK rise	t_{SRD}	45		45		ns
RxD data hold after SCLK rise	t_{HSR}	0		0		ns



4.10 High-speed Serial Channel Timing

(1) I/O Interface mode (DVCC3=1.65V~3.3V)

In the table below, the letter x represents the fsys cycle period, which varies depending on the programming of the clock gear function.

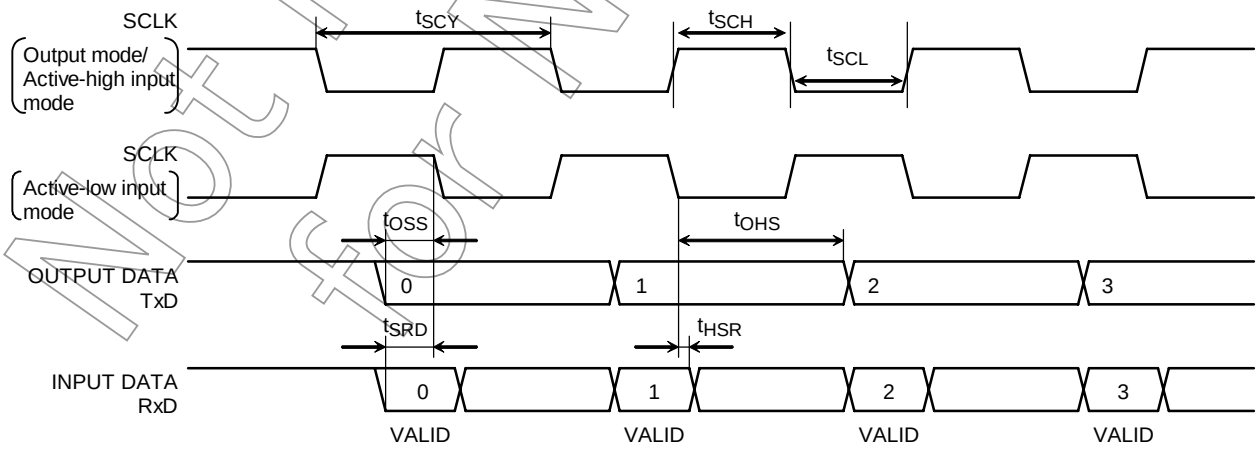
① HSCLK input mode (HSIO0~HSIO1)

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
SCLK period (programmable)	t_{SCY}	6x		111		ns
SCLK clock high width (Input)	Tsc_H	3x		55.5		ns
SCLK clock low width (Input)	Tsc_L	3x		55.5		ns
TxD data to SCLK rise	t_{OSS}	t_{SCY}/2-2x-30		-11.5		ns
TxD data hold after SCLK rise	t_{OHS}	8(x/2)-15		59		ns
RxD data valid to SCLK rise	t_{SRD}	30		30		ns
RxD data hold after SCLK rise	t_{HSR}	2(x/2)+30		48.5		ns

*SCLK rise or fall: Measured relative to the programmed active edge of SCLK.

② HSCLK output mode (HSIO0~HSIO1)

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
SCLK period (programmable)	t_{SCY}	8(x/2)		74		ns
TxD data to SCLK rise	t_{OSS}	4(x/2)-10		27		ns
TxD data hold after SCLK rise	t_{OHS}	4(x/2)-10		27		ns
RxD data valid to SCLK rise	t_{SRD}	45		45		ns
RxD data hold after SCLK rise	t_{HSR}	0		0		ns



4.11 SBI Timing

(1) I2C mode

In the table below, the letters x and t represent the fsys periods and ϕT0 respectively.

n denotes the value of n programmed into the SCK (SCL output frequency select) field in the SBI0CR1.

Parameter	Symbol	Equation		Standard mode f_{SYS} = 8 MHz n = 4		Fast mode f_{SYS} = 32 MHz n = 4		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	t_{SCL}	0		0	100	0	400	kHz
Hold time for START condition	$t_{HD:STA}$			4.0		0.6		μs
SCL clock low width (Input) (Note 1)	t_{LOW}			4.7		1.3		μs
SCL clock high width (Input) (Note 2)	t_{HIGH}			4.0		0.6		μs
Setup time for a repeated START condition	$t_{SU:STA}$	(Note 5)		4.7		0.6		μs
Data hold time (Input) (Note 3, 4)	$t_{HD:DAT}$			0.0		0.0		μs
Data setup time	$t_{SU:DAT}$			250		100		ns
Setup time for STOP condition	$t_{SU:STO}$			4.0		0.6		μs
Bus free time between STOP and START conditions	t_{BUF}	(Note 5)		4.7		1.3		μs

Note 1) SCL clock low width (output) is calculated with: $(2^{(n-1)}+4)$ T.

Normal mode: 6usec@Typ(fsys=8MHz, n=4)

Fast mode: 1.5usec@Typ(fsys=32MHz, n=4)

Note 2) SCL high width (output) is calculated with: $(2^{(n-1)})$ T.

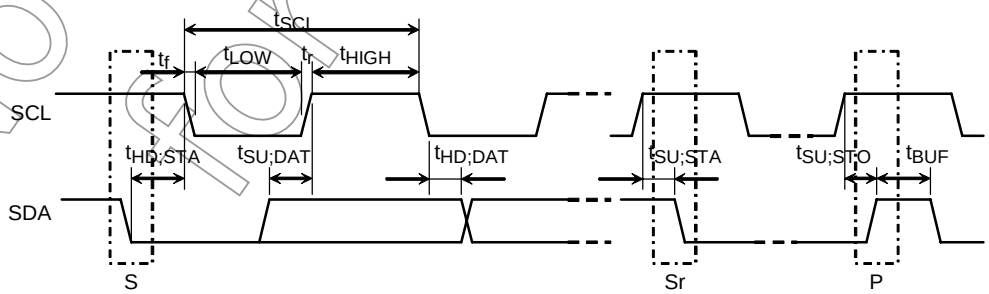
Normal mode: 4usec@Typ(fsys=8MHz, n=4)

Fast mode: 1usec@Typ(fsys=32MHz, n=4)

Note 3) The output data hold time is equal to 12x

Note 4) The Philips I^2C-bus specification states that a device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the fall edge of SCL. However, this SBI does not satisfy this requirement. Also, the output buffer for SCL does not incorporate slope control of the falling edges; therefore, the equipment manufacturer should design it to satisfy the input data hold time shown in the table, including tr/tf of the SCL and SDA lines.

Note 5) Software-dependent



S: START condition
Sr: Repeated START condition
P; STOP condition

Fast mode: fsys ≥ 20 MHz

Standard mode:fsys ≥ 4 MHz

(2) Clock-Synchronous 8-Bit SIO mode

In the table below, the letters x and t represent the fsys periods and ϕT0 respectively.
The letter n denotes the value of n programmed into the SCK (SCL output frequency select) field in the SBI0CR1.

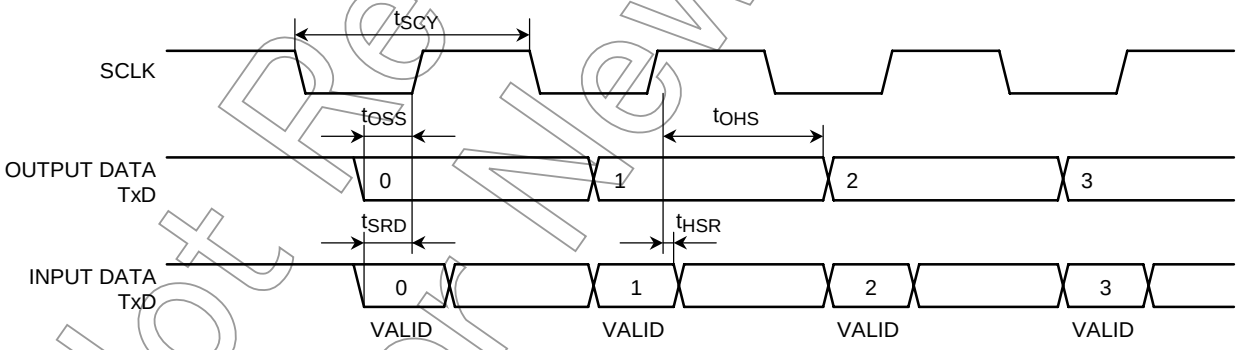
The electrical specifications below are for an SCLK signal with a 50% duty cycle.

③ SCK input mode

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
SCK period	t_{SCY}	16x		296		ns
TxD data to SCK rise	t_{OSS}	$(t_{SCY}/2)-(6x+20)$		17		ns
TxD data hold after SCK rise	t_{OHS}	$(t_{SCY}/2)+4x$		222		ns
RxD data valid to SCK rise	t_{SRD}	0		0		ns
RxD data hold after SCK rise	t_{HSR}	4x+10		84		ns

④ SCK output mode

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
SCK period (programmable)	t_{SCY}	16x		296		ns
TxD data to SCK rise	t_{OSS}	$(t_{SCY}/2)-20$		128		ns
TxD data hold after SCK rise	t_{OHS}	$(t_{SCY}/2)-20$		128		ns
RxD data valid to SCK rise	t_{SRD}	2x+30		67		ns
RxD data hold after SCK rise	t_{HSR}	0		0		ns



4.12 Event Counter

In the table below, the letter x represents the fsys cycle period.

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Clock low pulse width	t_{VCKL}	2X+100		137		ns
Clock high pulse width	t_{VCKH}	2X+100		137		ns

4.13 Capture

In the table below, the letter x represents the fsys cycle period.

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Low pulse width	t_{CPL}	2X+100		137		ns
High pulse width	t_{CPH}	2X+100		137		ns

4.14 General Interrupt (INTC)

In the table below, the letter x represents the fsys cycle period.

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Low pulse width for INT0-INTA	t_{INTAL}	X+100		118.5		ns
High pulse width for INT0-INTA	t_{INTAH}	X+100		118.5		ns

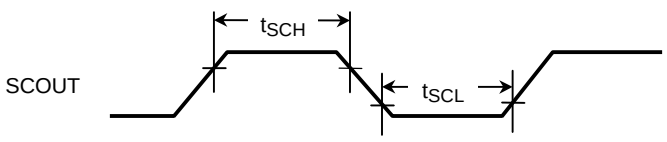
4.15 $\overline{\text{NMI}}$/STOP Release Interrupt

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Low pulse width for $\overline{\text{NMI}}$ and INT0-INT4	t_{INTBL}	100		100		ns
High pulse width for INT0-INT4	t_{INTBH}	100		100		ns

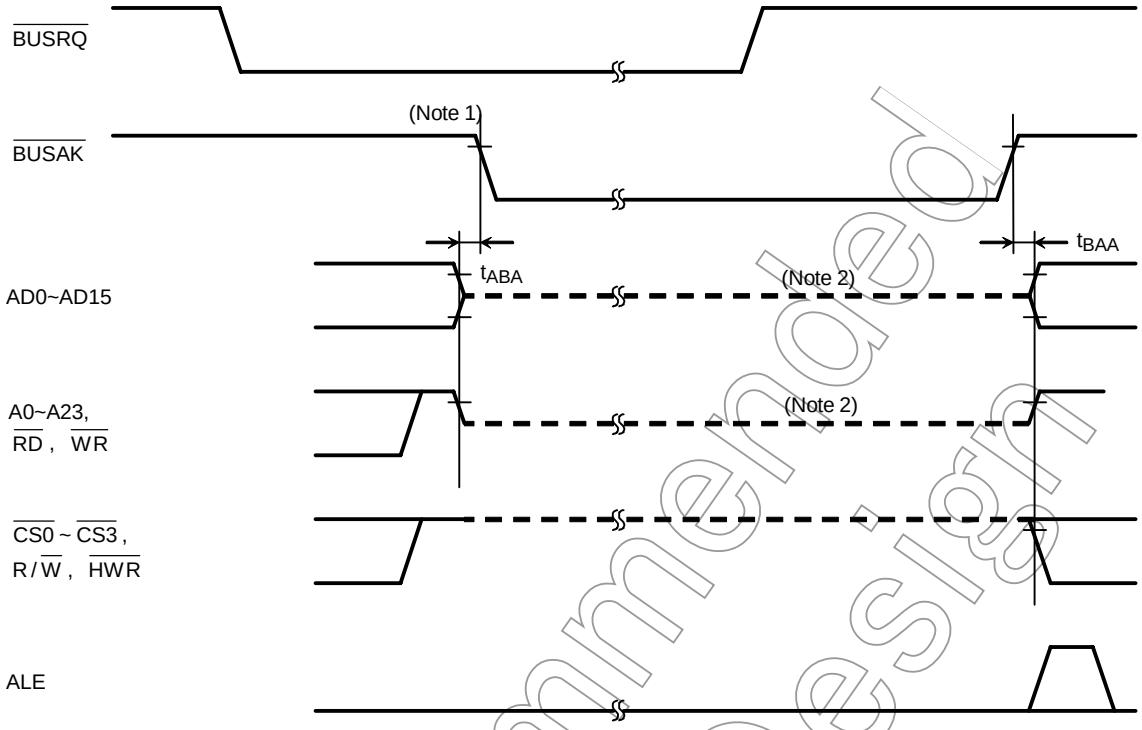
4.16 SCOUT Pin AC Characteristics

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Clock high pulse width	t_{SCH}	0.5T−5		4.3		ns
Clock low pulse width	t_{SCL}	0.5T−5		4.3		ns

Note: In the above table, the letter T represents the cycle period of the SCOUT output clock.



4.17 Bus Request and Bus Acknowledge Signals



Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Bus float to $\overline{BUSAK}$ fall	t_{ABA}	0	80	0	80	ns
Bus float to $\overline{BUSAK}$ rise	t_{BAA}	0	80	0	80	ns

(Note 1) If the current bus cycle has not terminated due to wait-state insertion, the TMP19A61 does not respond to $\overline{BUSRQ}$ low until the wait state ends.

(Note 2) This broken line indicates that output buffers are disabled, not that the signals are at indeterminate states. The pin holds the last logic value present at that pin before the bus is relinquished. This is dynamically accomplished through external load capacitances. In case of using the external load capacitance to maintain the bus at a predefined state, the equipment manufacturer needs to consider the additional time (determined by the CR constant) required for the signal transmission through the external load capacitances. The on-chip, integrated programmable pullup/pulldown resistors remain active, depending on internal signal states.

4.18 KWUP Input

With Pull up

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Low pulse width for KEY0~D	tky_{TBL}	X+100		118		ns
High pulse width for KEY0~D	tky_{TBH}	X+100		118		ns

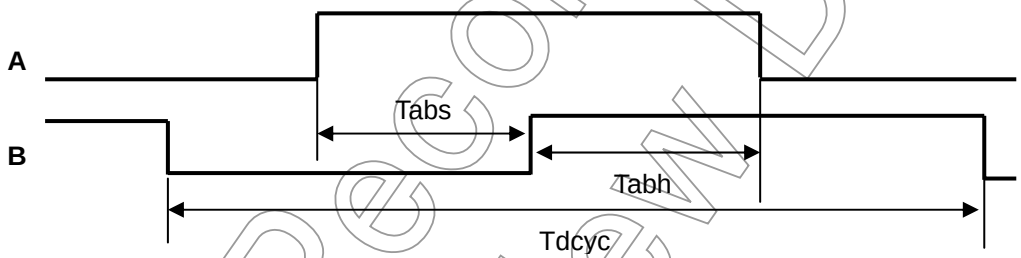
Without pull up

Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Low pulse width for KEY0~D	tky_{TBL}	100		100		ns

4.19 Dual Pulse Input

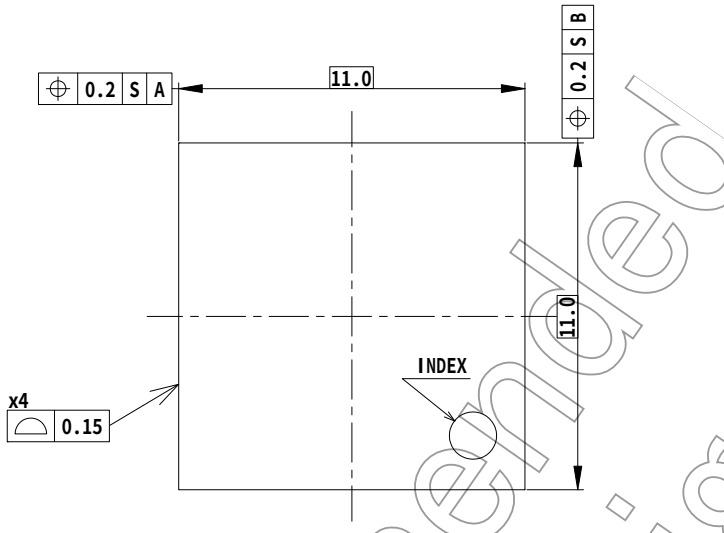
Parameter	Symbol	Equation		54 MHz		Unit
		Min	Max	Min	Max	
Dual input pulse period	Tdcyc	8Y		296		ns
Dual input pulse setup	Tabs	Y+20		57		ns
Dual input pulse hold	Tabh	Y+20		57		ns

Y: fsys/2

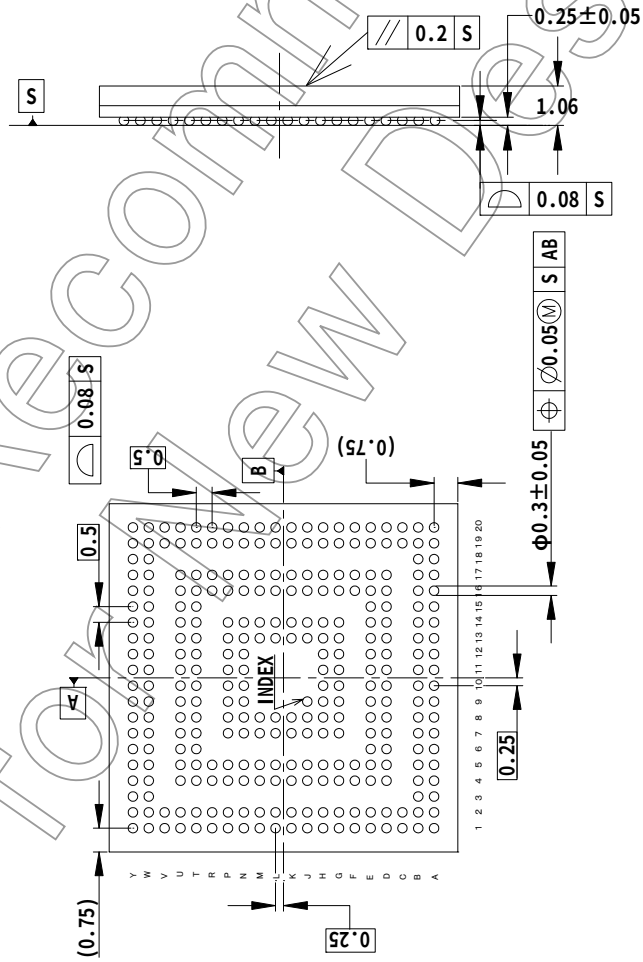


5. Package

P-TFBGA289-1111-0.50A



TOP VIEW



BOTTOM VIEW