POWER-FACTOR-CORRECTION/PMW CONTROLLER

FEATURES

- Power Factor Correction/Line Harmonics Reduction to Meet IEC1000-3-2 Requirements
- Optimized for Offline Operation
- Maximum Duty Ratio 88% (typ.)
- Frequency Reduction for Improved Over-Current Protection
- Low Standby Current for Current-Fed Startup
- Current-Mode or Voltage-Mode Control
- Built-In User-Adjustable Slope Compensation
- Functionally Integrated & Simplified 5-pin Design

APPLICATIONS

- Power Factor Correction Converters
- Off-Line Power Supplies
- Industrial Power Supplies
- Off-Line Battery Chargers

DESCRIPTION

The TK75003 is a five-pin primary side controller optimized for off-line switching power supplies including power-factor correctors. It is suitable for both voltage-mode and current-mode control and has advanced features not available in controllers with a higher pin count. The key to full functionality in a five-pin design is that the current signal and the error signal are added together and fed into the feedback pin. A sawtooth current flowing out of the feedback pin provides a slope compensation ramp (in current-mode applications) or a PWM ramp (in voltage-mode applications), in proportion to the resistance terminating that pin. If the sum of the current sense signal, error signal and ramp signal exceeds the Over-Current Detector threshold indicating that the Current Control Detector has lost control of the switch current, the charging current of the timing capacitor will be reduced to about 25% for the remainder of the clock period. The reduced charging current causes as much as about a one third reduction in switching frequency, effectively preventing short-circuit current runaway.

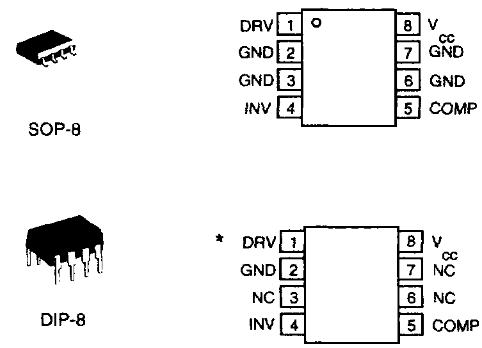
ORDERING INFORMATION

TK75003 □ □ □□

- Tape/Reel Code
- Temp. Range (Extended)
- Package Code

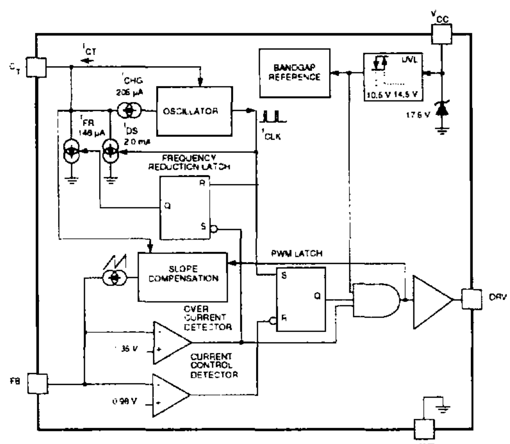
PACKAGE CODE	EXTENDED TEMP. RANGE (OPT)	TAPE/REEL CODE
D : DIP-8	I : -40 to + 85 °C	BX : Bulk/Bag
M: SOP-8		TL : Tape Left

TK75003



* For the DIP-8 package only, pins 2 and 3 must be externally shorted for proper operation.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 3)
75003D .... 825 mW
75003M .... 1000 mW
Power Derating, $T_A > 25$ °C
75003D .... 6.6 mW/°C
75003M .... 8 mW /°C
Supply Voltage (Low Impedance Source) .... 16 V

Supply Voltage ($I_{CC} < 30$ mA) .... Self Limiting
Output Energy (Capacitive Load) .... 5 µJ
CT and FB pins .... 16 V
Junction Temperature .... 150 °C
Operating Temperature Range
Standard Range .... -20 to +80 °C
Extended Range (I) .... -40 to + 85 °C

ELECTRICAL CHARACTERISTICS

V_{CC} = 13.0 V, C_{CC} = 4.7 µF, C_T = 800 pF, C_{DRV} = 1 nF, $T_A = T_J$ = Full Operating Temperature Range, unless otherwise specified. Typical numbers apply at $T_A = T_J$ = 25 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CC(START)}$	Start-up Supply Current	Current Source to V_{CC} pin		0.5	1.0	mA
$I_{CC(on)}$	Operating Supply Current			14.5	19.0	mA
$V_{CC(on)}$	UVLO On Voltage	(Note 1)	12.5	14.5	16.0	V
$V_{CC(off)}$	UVLO Off Voltage		9.0	10.5	12.0	V
V_{HYST}	Hysteresis		2.8	4.0		V
$V_{CC,CLAMP}$	Internal Clamp Voltage	I_{CC} = 25 mA (Note 1)	16.0	17.5	19.0	V
Oscillator Section (CT Pin)						
f_{DRV}	Frequency at DRV pin	$T_A = T_J$ = 25 °C	90	100	110	kHz
		$T_A = T_J$ = -20 to 80 °C	80		115	kHz
$V_{CT,PK}$	Peak Voltage		2.5	3.2	3.9	V
$V_{CT,VL}$	Valley Voltage			1.1		V
$I_{CT,DIS}$	Discharge Current		1.0	1.8	3.0	mA
$C_{T,MAX}$	Maximum Timing Capacitance		4.7			nF
Current Detector, Feedback, and Frequency Reduction Sections (FB Pin)						
V_{CCD}	Current Ctrl. Detector Reference Voltage	$T_A = T_J$ = 25 °C	0.950	0.980	1.01	V
		$T_A = T_J$ = Full range	0.925		1.035	V
V_{OCD}	Over Current Detector Reference Voltage	$T_A = T_J$ = 25 °C	1.320	1.350	1.380	V
		$T_A = T_J$ = Full range	1.305		1.395	V
$t_{FB,OC,PD}$	Propagation Delay to DRV pin	V_{FB} steps from 0 to 2 V		60	130	ns
$t_{FB,CC,PD}$	Propagation Delay to DRV pin	V_{FB} steps from 0 to 1.20 V (Note 4)		80	180	ns
$i_{SC,PK}$	Slope Compensation Peak Current	$V_{CT} = V_{CT,PK}$ (Note 2) $T_A = T_J$ = 25 °C	-245	-200	-155	µA
$i_{SC,VL}$	Slope Compensation Valley Current	$V_{CT} = V_{CT,VL}$ (Note 2) $T_A = T_J$ = 25 °C	-65	-40	-15	µA
$i_{SC,PK\text{-}VL}$	Slope Compensation Peak to Valley	$V_{CT} = V_{CT,VL}$ (Note 2) $T_A = T_J$ = 25 °C	-200	-160	-120	µA

ELECTRICAL CHARACTERISTICS (CONT.)

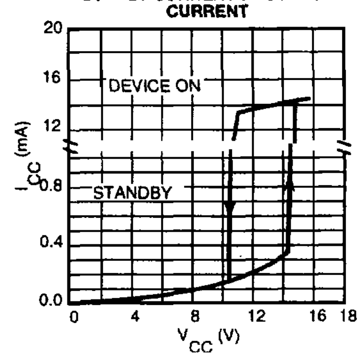
V_{CC} = 13.0 V, C_T = 800 pF, C_{DRV} = 1 nF, $T_A = T_J$ = Full Operating Temperature Range, unless otherwise specified. Typical numbers apply at $T_A = T_J$ = 25 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Reducer (Over Current Protection Timing)						
$f_{DRV,FR}/f_{DRV}$	Frequency Reduction Ratio	$V_{FB} = V_{DRV}$	20	30	40	%
Output Section (DRV Pin)						
$D_{DRV,(max)}$	Maximum Duty Ratio		85	88	91	%
$t_{DRV,RISE}$	Rise Time	1000 pF load, V_{CC} = 15 V		25	75	ns
$t_{DRV,FALL}$	Fall Time	1000 pF load, V_{CC} = 15 V		25	75	ns
$V_{DRV,HIGH}$	Output HighVoltage	I_{DRV} = -40 mA	10.1	11		V
		I_{DRV} = -100 mA	10.0	10.8		V
$V_{DRV,LOW}$	Output Low Voltage	I_{DRV} = 40 mA		0.1	0.25	V
		I_{DRV} = 100 mA		0.2	0.50	V
		I_{DRV} = 5 mA and V_{CC} = 9 V		1.0	1.5	V

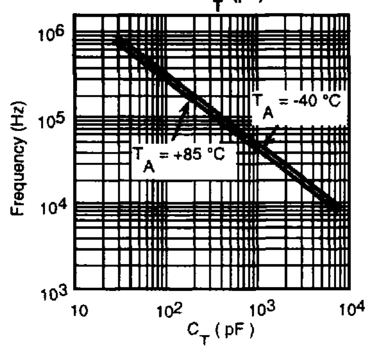
Note 1: The UVLO "ON" voltage is guaranteed to be always below the internal clamp voltage.
Note 2: For temperature dependence see chart. (Slope Compensation Peak Current vs. Temperature)
Note 3: Thermal specifications apply when using appropriate mounting technique. See "Layout Considerations" section for further details.
Note 4: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

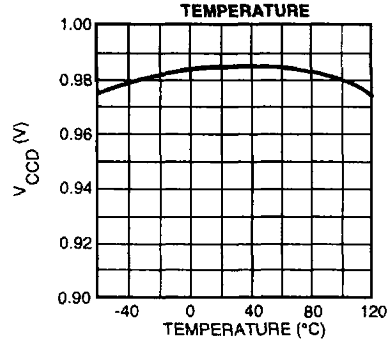
SUPPLY CURRENT vs. OUTPUT CURRENT



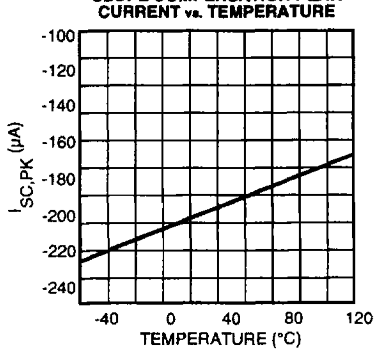
FREQUENCY AT DRV vs. C_T (pF)



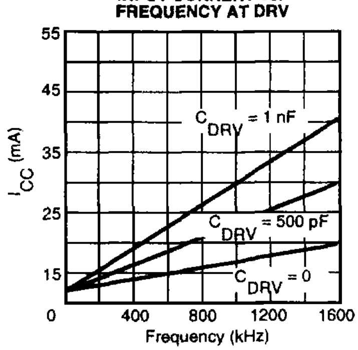
CURRENT CONTROL REFERENCE vs. TEMPERATURE



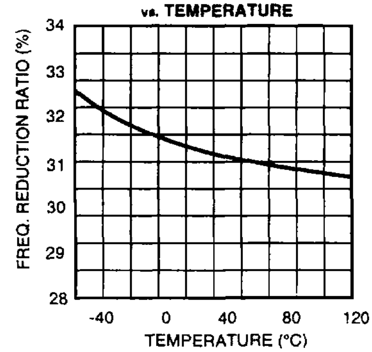
SLOPE COMPENSATION PEAK CURRENT vs. TEMPERATURE



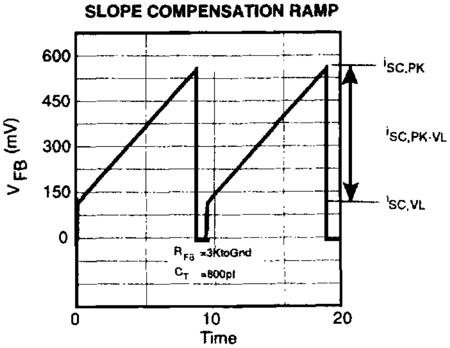
INPUT CURRENT vs. FREQUENCY AT DRV



FREQUENCY REDUCTION RATIO vs. TEMPERATURE



SLOPE COMPENSATION RAMP



THEORY OF OPERATION

The TK75003 is intended for use as a primary-side PWM controller. Using a control technique referenced in the "Application Information" section, the TK75003 can be used as a highly cost-effective controller for power factor correction. The many features integrated into a simple five-pin design allow it to be easily configured for voltage-mode or current-mode control, fixed-frequency or fixed-off-time operation, off-line bootstrapping, and direct drive of a power MOSFET. The polarity of the feedback signal allows for simpler interface with a TL431-derived error signal (see Applications Information section).

The most noteworthy integrated feature in the TK75003 is the way in which the feedback control pin is configured to receive the error signal and the current signal for current-mode control. Rather than receiving both inputs into a comparator, a single input receives both signals summed together and compares them against a fixed internal reference. This yields two desirable effects: a) a current-limit threshold is automatically established, and b) the required error-signal polarity is the inverse of that of a standard two-input current-mode control system. Generally, the signal summation requires no additional external components and the required error-signal polarity is simpler to achieve.

Two other functions are integrated into the feedback pin. A current ramp, which can be used to establish either the slope-compensation ramp for a current-mode control design or the voltage-comparison ramp for a voltage-mode control design, flows out of the feedback pin. By adjusting the terminating resistance at the feedback pin, the desired ramp magnitude is established. For over-current protection, a second fixed-reference comparator monitors the feedback pin. If the feedback pin voltage should reach this second threshold, this indicates that cycle-by-cycle PWM control is not sufficient for maintaining control of the current, (i.e., the minimum duty-ratio is too large to achieve volt-second balance in the magnetics). The over-current detection comparator latches (for one cycle) a reduction in the source current which feeds the timing capacitor. This has the effect of reducing the switching frequency and thus, effectively, the minimum duty ratio, which is just what is needed to maintain control of the current.

The switching frequency is determined by an internal current source charging an external timing capacitor. The timing capacitor is ramped between internally-fixed thresholds, valley to peak, and then quickly discharged. A fixed off-time control technique can readily be implemented by using a small transistor to keep the timing capacitor discharged during the on-time. When the on-pulse is terminated, the timing capacitor ramps up to a fixed threshold at a fixed rate to fix the off-time.

The UVLO feature with hysteresis minimizes the start-up current which allows a low-power bootstrap technique to be used for the housekeeping power. The duty ratio of the TK75003 is limited to approximately 88% by the time required to discharge the timing ramp.

PIN DESCRIPTION

V_{CC} Pin

This pin is connected to the supply voltage. The IC is in a low-current (500 µA typ.) stand-by mode before the supply voltage exceeds 14.5 V (typ), which is the upper threshold of the undervoltage lockout circuit. The IC switches back to stand-by mode when the supply voltage drops below 10.5 V (typ). An internal clamp limits the peak supply voltage to about 17.5 V (typ). The absolute maximum supply voltage from a low impedance source is 16 V. The device is always guaranteed to turn on before the internal clamp turns on.

GND Pin

This pin provides ground return for the IC.

DRV Pin

This pin drives the external MOSFET with a totem pole output stage capable of sinking or sourcing a peak current of about 1 A. In stand-by mode, the drive pin can sink about 5 mA while keeping the drive pin pulled down to about 1 V. The maximum duty cycle of the output signal is typically 88%.

C_T Pin

The external timing capacitor is connected to the C_T pin. That capacitor is the only component needed for setting the clock frequency. The frequency measured at the C_T pin is the same frequency as measured at the Drive pin. The maximum recommended clock frequency of the device is 1.6 MHz. At normal operation, during the rising section of the timing-capacitor voltage, a trimmed internal current of 205 µA flows out from the C_T pin and charges the capacitor. During the falling section of the timing-capacitor voltage an internal current of about 1.8 mA discharges the capacitor. If the voltage at the FB (feedback) pin exceeds 1.35 V (e.g. due to the turn-off delay during a short-circuit at the output of a converter using the IC), the charging current is reduced to about 59 µA, leading to a 3.2-fold reduction in switching frequency. The frequency reduction is useful for preventing short-circuit current runaway.

FB (feedback) Pin

The feedback pin receives the sum of three signals: the error signal (from the external error amplifier), the switch current signal and a voltage ramp generated across the terminating resistance by an internal sawtooth-shaped current with a peak value of about 200 µA. The error signal is needed for stabilizing the output voltage or current. The switch current signal is needed in current-mode controlled converters and in converters with cycle-by-cycle overload protection. Also, the switch current signal is required for detecting impending short-circuit current runaway, and for initiating a frequency reduction for preventing the runaway. The voltage ramp is needed for slope compensation (necessary for avoiding subharmonic instability in constant-frequency peak-current controlled current-mode converters above 50% duty ratio), or for pulse-width modulation (in voltage-mode controlled converters).

At higher clock frequencies, the bandwidth limitation of the internally-generated sawtooth-shaped current source becomes more apparent. The degree to which ramp bandwidth is tolerable depends on performance requirements at narrow pulse widths. A low impedance at the feedback pin can effectively eliminate the internally-generated ramp effects and an external ramp can be readily created to attain higher performance at high frequencies, if desired.

DESIGN CONSIDERATIONS

Selecting the start-up resistor

Figure 1a(a) shows the typical application of the TK75003 in an off-line flyback power supply (input full-wave bridge and capacitor not shown). The IC starts when the voltage across the capacitor C_{aux} reaches the UVLO on Voltage $V_{CC(on)}$ of the IC. The starting resistor R_{st} can be designed as follows:

$$R_{st,max} = \frac{V_{in,min} - V_{CC(on),max} - 2V}{I_{CC(start),max}} \qquad (1)$$

At 85-Vrms line voltage, and taking into account the specified maximum values of the UVLO on voltage and the standby supply current $I_{CC(off)}$, the maximum allowed value of the starting resistor is:

$$R_{st,max} = \frac{85\sqrt{2} - 16 - 2}{1.0m} = 102.2k\Omega \qquad (2)$$

A practical choice for the starting resistor is R_{st} = 100 kΩ. The worst-case dissipation of the resistor appears at high line and at the minimum V_{CC} voltage. At 265-Vrms line voltage and 9-V V_{CC}, the dissipation is 2.2 W, so a 3-W resistor should be used. Note that 1.0 mA reflects the worst case $I_{CC(START)}$ at the edge of UVLO release.

Selecting the transformer turns ratio

During steady-state operations, the auxiliary supply voltage is generated by the auxiliary winding n_3 and the rectifier diode D3. In the flyback power supply, neglecting the effect of the leakage inductance of the transformer, the number of turns of the auxiliary winding can be calculated from the following equation:

$$n_3 = n_1 \frac{V_{aux} + V_{D3}}{V_O + V_{D2}} \qquad (3)$$

where VD2 and VD3 are the forward voltage drops of the output rectifier diode and the auxiliary rectifier diode. The voltage Vaux should be selected such that it stays between the specified worst-case upper and lower limits of the IC, considering the component tolerances, ripple, and other second-order effects. The upper limit for Vaux is the minimum voltage of the built-in clamp (16V). The lower limit for Vaux is the maximum UVLO off voltage (12.0 V). It is prudent to choose the mean value of those two voltages (i.e. 14.0 V), as V_{aux}.

Compensating for the effect of leakage inductance

The leakage inductance of the flyback transformer causes a voltage overshoot at turn-off of the MOSFET. The magnitude and duration of the overshoot depends on the leakage inductance, the peak current at turn-off, and the voltage-clamping circuit employed to limit the overshoot.

The overshoot tends to increase the auxiliary voltage. The simplest solution to reduce that increase is to add a resistor R_{aux} in series with the rectifier diode D_3. The optimal value of the resistor can be calculated from the subcircuit shown in Figure 1b.

The average current flowing in R_{aux} is equal to the current I_{aux} drawn by the IC. The following equation can be written from the equality:

$$I_{aux} = \frac{1}{R_{aux}}\left[\left(V_1 - V_{D3} - V_{aux}\right)\frac{T_1}{T} + \left(V_2 - V_{D3} - V_{aux}\right)\frac{T_2}{T}\right] \quad (4)$$

The voltage V_1 can be calculated as follows:

$$V_1 = \left(V_O + V_{D2}\right)\frac{n_1}{n_2} + V_{overshoot}\frac{n_3}{n_1} \qquad (5)$$

where $V_{overshoot}$ is the additional voltage appearing across the MOSFET due to the leakage inductance.

The voltage V_2 can be calculated as follows:

$$V_2 = \left(V_O + V_{D2}\right)\frac{n_3}{n_2} \qquad (6)$$

T_1 is the time required for the leakage inductance of the flyback transformer to completely discharge its stored energy into the voltage clamp. T_1 can be calculated as:

$$T_1 = \frac{I_{pk} L_{leakage}}{V_{overshoot}} \qquad (7)$$

where I_{pk} is the peak current in the MOSFET at turn-off and $L_{leakage}$ inductance of the flyback transformer measured at winding n_1.

T_2 is the conduction time of the output diode D_2 and T is the switching period.

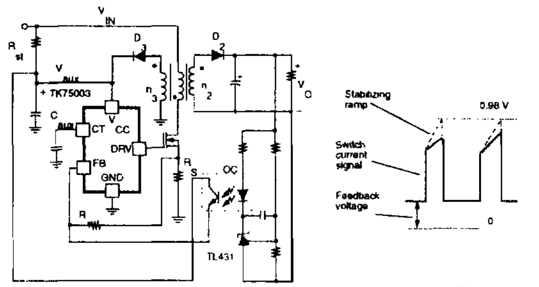
From (4) the resistance R_{aux} or the voltage V_{aux} can be calculated. As an example, let us calculate the value of R_{aux} with the following typical values:

$V_o = 12$ V	$V_{D2} = V_{D3} = 1$ V	$I_{pk} = 1$ A
$L_{leakage} = 2\ \mu H$	$V_{overshoot} = 20$ V	$V_{aux} = 13.5$ V
$I_{aux} = 18$ mA	$T_2 = 2\ \mu s$	$T = 5\ \mu s$
$n_1 = 31$	$n_2 = 6$	$n_3 = 7$

Equations (5), (6) and (7) yield $V_1 = 19.7$ V, $V_2 = 15.2$ V, and $T_1 = 100$ ns. Substituting those values into (4) and solving for R_{aux} yields:

$$R_{aux} = 20.6\Omega$$

Rounding the result to the nearest 5% standard value gives $R_{aux} = 20\Omega$.



(a) (b)

Figure 1a. The TK75003 in a flyback power supply

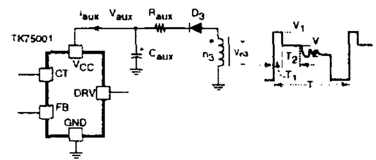
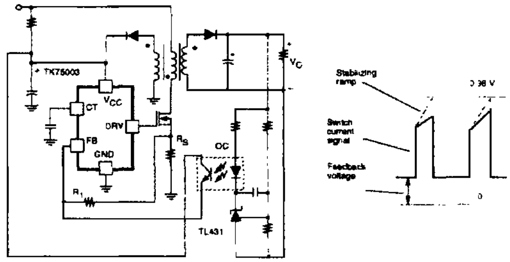


Figure 1b. Subcircuit for calculating the value of R_{aux}.

APPLICATION INFORMATION

Self-biased power supply with constant-frequency current-mode control

Figure 1c(a) shows the TK75003 IC in the typical application: a flyback converter with self bias and constant-frequency current-mode control. Figure 1c(b) shows the feedback-pin voltage. In the converter, the voltage-error amplifier (a TL431 shunt regulator IC) is located at the output side and the error signal is transmitted to the input side through the opto-coupler OC. Three signals are added together at the feedback pin: the feedback voltage that develops across the resistor R_1, the switch current signal, and the stabilizing ramp. In each cycle, the MOSFET switch is turned off when the sum of those three signals reaches 0.92 V.



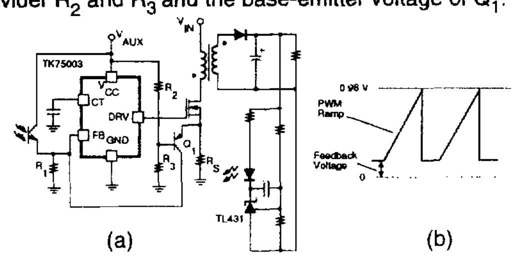
(a) (b)

Figure 1c. The TK75003 in a self-biased flyback converter with constant-frequency current-mode control: (a) schematic, (b) voltage at feedback pin.

Power supply with constant-frequency voltage-mode control and cycle-by-cycle current limit

Voltage-mode control is free from some of the disadvantages (e.g. subharmonic instability and noise sensitivity) of current-mode control. It is very easy to implement that control method with the TK75003 IC. Figure 2a shows the IC in a voltage-mode-controlled flyback converter. Figure 2b shows the feedback-pin voltage. The only circuit difference between current-mode control and voltage-mode control is in the connection of the resistor R_1, that terminates the feedback pin. In current-mode control, that resistor is connected to the current-sense resistor of the converter. In voltage-mode control, that resistor is connected to ground.

In voltage-mode control, overload protection can be realized by adding a simple circuit to the control IC, as shown in the figure. The pnp transistor Q_1, turns on and pulls up the feedback pin when the switch current times the resistance of the sense R_S reaches the threshold set by the resistive divider R_2 and R_3 and the base-emitter voltage of Q_1.



(a) (b)

Figure 2. The TK75003 in a voltage-mode-controlled converter with additional cycle-by-cycle current limit: (a) schematic, (b) voltage at the feedback pin.

Power supply with constant-off-time current-mode control

The advantages of constant-off-time current-mode control over constant-frequency current-mode control are that (1) there is no need for a stabilizing ramp, (2) the converter is free from subharmonic instability (i.e. there is no need for slope compensation), and (3) the line-voltage variation is automatically canceled in buck-derived converters, e.g. the forward converter. Figure 3 shows the implementation of that control method. As can be seen, a transistor Q_1 must be added to the controller. Figure 4 shows the timing-pin and feedback-pin voltages for the TK75003. The transistor Q_1 keeps the timing pin at ground potential during the on time of the switch. Timing begins when the drive output returns to low and Q_1 is turned off. The off time for typical charge and discharge currents and peak and valley voltages is:

$t_{OFF} = C_T \times 14\ k\Omega$.

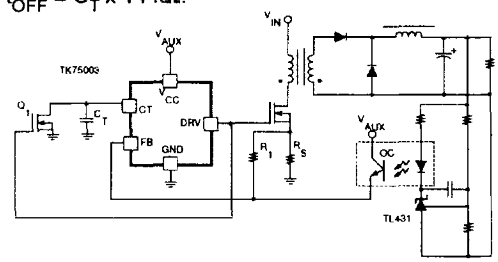


Figure 3. The TK75003 in a forward converter with constant-off-time current-mode control.

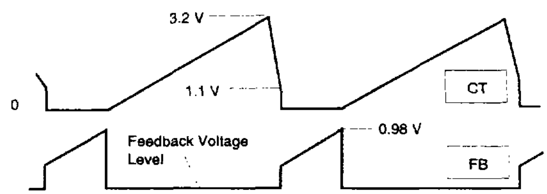


Figure 4. Timing-pin and feedback-pin voltages with constant-off-time current-mode control.

The TK75003 in non-isolated applications

Although the IC was intended for off-line power-supply applications with the voltage-error amplifier at the isolated output, it is easy and economical to use the device in non-isolated applications, too. Figure 5 shows a low-cost boost power-factor corrector controlled by the TK75003. Power-factor correction is achieved by controlling the boost converter with constant-frequency peak-current control and exploiting the variation of the allowed peak-current level caused by the variable duty ratio and the stabilizing ramp. Figure 6 shows a buck-boost converter with negative input voltage and positive output voltage, controlled by the TK75003. In both cases, the voltage-error amplifier is a TL431 shunt regulator, and a pnp transistor provides interface between the TL431 and the control IC.

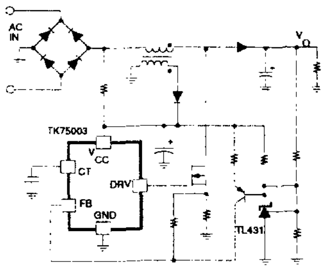


Figure 5. Low cost boost power-factor corrector using the TK7003

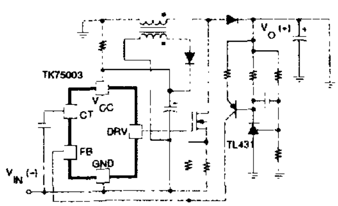


Figure 6. Buck-boost converter with neative input and positive output, using the TK75003

Figure 7 shows a universal-input, 100-watt boost power-factor corrector application circuit. The control technique is called "current-clamped control." Both the control technique and the application circuit with waveforms are described in the paper "Low-Cost Power-Factor Correction/ Line-Harmonics Reduction with Current-Clamped Boost Converter," published in the conference proceedings of Power Conversion Electronics '95/Powersystems World™ '95. A copy of the paper can be obtained by contacting Toko.

For designers who wish to explore other performance optimizations of the current-clamped boost power-factor corrector, aside from the conference paper Toko offers a Mathcad© file which can accurately display current waveforms and predict power factor, harmonic distortion, and individual harmonic currents. The Mathcad file and the text which describes how to use it are available from the Toko Design Center.

The power-factor corrector in Figure 7 has been optimized for general wide-range-input use. In order to obtain the same performance at power levels other than 100 W, the control components do not need to change. The power component values change as follows: C8 scales in proportion to the power level, and L1 and R8 scales in inverse proportion to the power level. Typically, although not directly related to the line-current shaping capability of the application circuit, C1 and C10 would scale in proportion to the power level. All the components in the power stage should have a current rating as needed to accommodate the power level.

Here follows a step-by-step design example, showing how to determine the resistance of R7 terminating the feedback pin and the resistance of the current-sense resistor R8, for the boost corrector of Figure 7.

Assumptions:

Output power:	$P_o = 100$ W
Output voltage:	$V_o = 380$ Vdc
Minimum line voltage:	$V_{i,min} = 85$ Vrms
Efficiency at 85 Vrms:	$\eta = 0.93$
Switching frequency:	f = 100 kHz
Inductance of boost inductor:	L1 = 2.5 mH
Maximum duty ratio of TK75003:	$D_{MAX} = 0.88$
Peak value of ramp current flowing out of the FB pin:	$I_{SC,PK} = 200\ \mu A$
Threshold voltage of the current-control detector:	$V_{CCD} = 0.98$ V

Calculations:

Peak value of minimum line voltage:

$V_{i,min,pk} = \sqrt{2} \bullet V_{i,min} = 120$ Vpk

Switch duty ratio at peak of minimum line voltage:

$D = 1 - V_{i,min,pk}/V_o = 0.684$

Peak-to-peak ripple current in inductor L1:

$I = V_{i,min,pk} \bullet D/(f \bullet L1) = 0.33$ A

Input power at minimum line voltage:

$P_i = P_o/\eta = 107.5$ W

Peak current in L1 (at peak of minimum line voltage):

$I_{L1,pk} = \sqrt{2} \bullet P_i/V_{i,min,pk} + I/2 = 1.95$ A

Resistance[1] of resistor R7:

$R7 = D_{MAX} \bullet V_{CCD}/I_{SC,PK} = 4.312$ kohms

Select for R7:

R7 = 4.3 kohms

Resistance[2] of current-sense resistor R8:

$R8 = (V_{CCD} - I_{SC,PK} \bullet R7 \bullet D)/I_{L1,pk} = 0.201$ ohms

Select for R8:

R8 = 0.18 ohms

[1]This value of R7 ensures that the line current will be zero around the zero-crossing of the line voltage, which is the required condition for low-distortion line current.

[2]This value of R8 ensures that the sum of the voltage drop across R8 (caused by the peak inductor current) and the voltage drop across R7 (caused by the instantaneous value of the stabilizing current) is equal to the threshold voltage of the current-control detector at the peak of the line voltage.

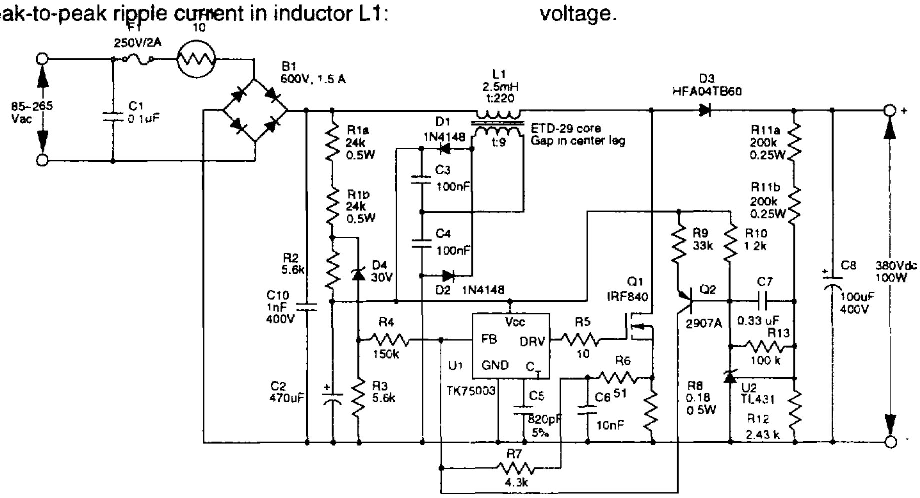
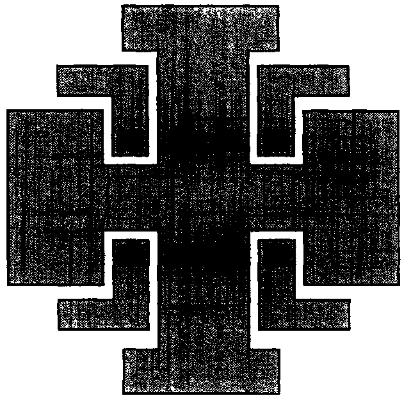


Figure 7. Boost Power Factor Corrector Application Circuit

RECOMMENDED PAD



Copper Pattern should be as large as possible. The power dissipation rating for the above pattern is ~800 mW at 25 °C, assuming standard one-once copper on a single-sided board. 1000 mW rating can be achieved by using heavier copper or vias under the device to conduct heat to the opposite side of a glass-apoxy printed wiring board. Forced-air cooling or use of a ceramic substrate can inprove the dissipation rating as high as -2000 mW. Always derate power dissipation above 25 °C linearly to zero at 150 °C.