



Reprogrammable 16K x 16 Registered PROM

Features

- 0.8-micron CMOS for optimum speed/power
- High speed
 - 25 ns max set-up
 - 25 ns clock to output
- 16-bit-wide words
- Registered outputs
- Programmable synchronous or asynchronous output enable
- Initialization capability
 - Separate control pin (INIT)
 - Programmable initialization word
- 40-pin, 600-mil-wide DIP packages
- 44-pin PLCC and 44-pin LCC packages
- 100% reprogrammable in windowed packages
- TTL-compatible I/O

- Capable of withstanding greater than 2001V static discharge

Functional Description

The CY7C272 is a high-performance 16K-word by 16-bit CMOS PROM with output registers. It is available in 40-pin, 600-mil-wide DIP packages and 44-pin PLCC and LCC packages. The 7C272 is 100% reprogrammable in windowed packages. The memory cells utilize proven EPROM floating gate technology and word-wide programming algorithms. The CY7C272 is a plug-in replacement for EPROM devices.

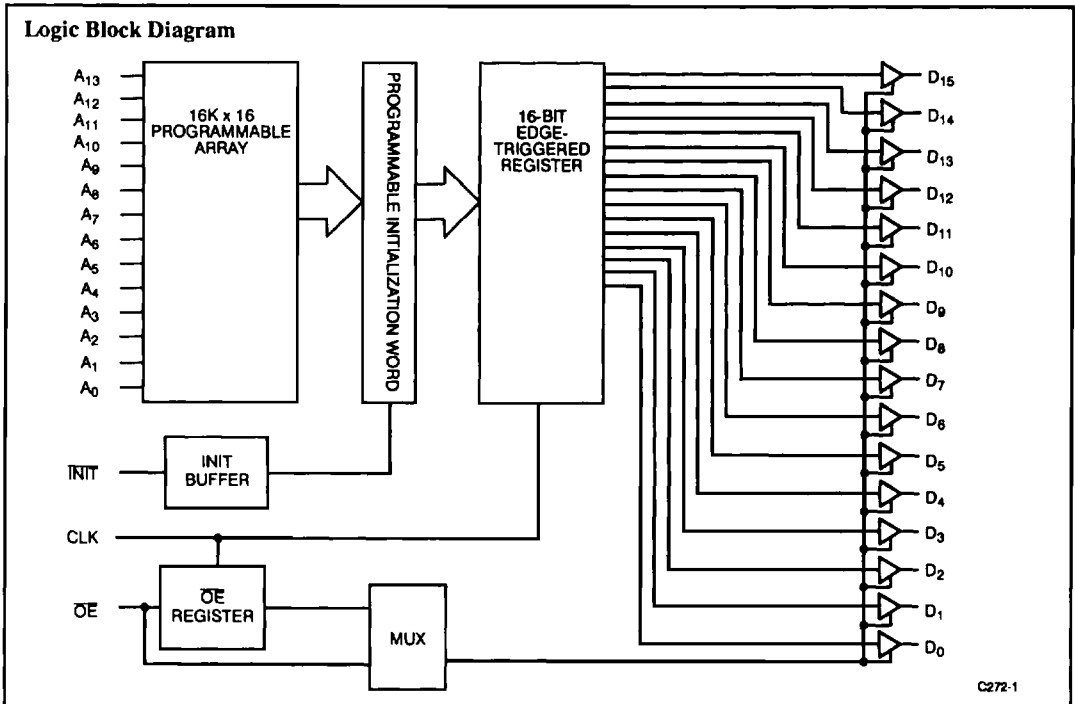
The CY7C272 features a programmable synchronous or asynchronous output enable and a programmable initialization word.

In order to read the CY7C272, an address is placed on the address lines ($A_{13} - A_0$). The data stored at the array location addressed by the address lines is placed in

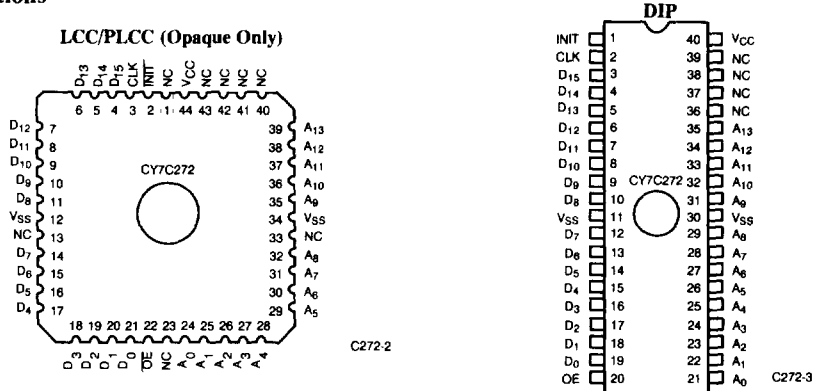
the output registers at the rising edge of CLK. The data will remain on the outputs until the following rising edge of CLK.

If asynchronous output enable is being used, the outputs will enter the active state whenever a LOW is placed on OE. If a HIGH is placed on OE, the outputs will be tri-stated. If the synchronous output enable is being used, the outputs will enter the active state following the first rising edge of CLK after a LOW is placed on OE. The outputs will be three-stated following the first rising edge of CLK after a HIGH is placed on OE.

An initialization control input (INIT) is provided. Applying a LOW to INIT causes an immediate load of the programmable initialize word into the output registers and onto the outputs. The output enable must be active when reading the initialization word. The INIT LOW disables CLK and must return HIGH to re-enable CLK.



Pin Configurations



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PROMS

Selection Guide

		CY7C272-25	CY7C272-30
Maximum Set-Up Time (ns)		25	30
Maximum Clock to Output (ns)		25	30
Maximum Operating Current (mA)	Commercial	200	200
	Military		250

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature - 65°C to +150°C
- Ambient Temperature with Power Applied - 55°C to +125°C
- Supply Voltage to Ground Potential - 0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State - 0.5V to +7.0V
- DC Input Voltage - 3.0V to +7.0V
- DC Program Voltage 13.0V
- UV Erasure 7258 Wsec/cm²
- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	- 40°C to +85°C	5V ±10%
Military ^[2]	- 55°C to +125°C	5V ±10%

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature

Electrical Characteristics^[3,4]

Parameter	Description	Test Conditions	CY7C272-25		CY7C272-30		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 2.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA (6.0 mA Mil)		0.4		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs.	2.0	V _{CC}	2.0	V _{CC}	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs.	- 3.0	0.8	- 3.0	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	- 10	+ 10	- 10	+ 10	μA
V _{CD}	Input Clamp Diode Voltage		Note 3				
I _{OZ}	Output Leakage Current	V _{CC} = Max., V _{OL} ≤ V _{OUT} ≤ V _{OH} , Output Disabled	- 40	+ 40	- 40	+ 40	μA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[5]	- 20	- 90	- 20	- 90	mA
I _{CC}	Power Supply Current	V _{CC} = Max., I _{OUT} = 0.0 mA	Com'l	200		200	mA
			Mil			250	mA

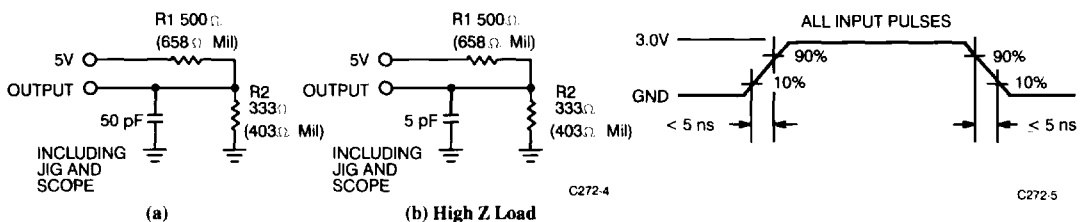
Capacitance^[3]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

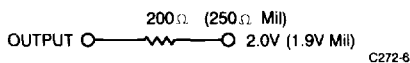
Notes:

- See Introduction to CMOS PROMs in this Data Book for general information on testing.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

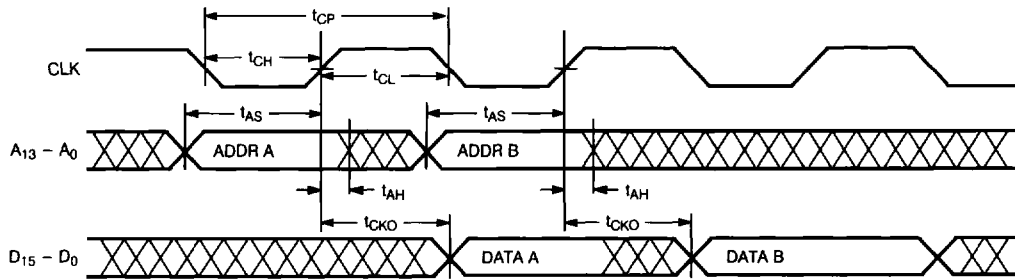


Switching Characteristics Over the Operating Range^{3,4}

Parameters	Description	CY7C272-25		CY7C272-30		Units
		Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	25		30		ns
t_{CH}	Clock HIGH Pulse Width	$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		ns
t_{CL}	Clock LOW Pulse Width	$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		ns
t_{AS}	Address Valid to CLK Rise	25		30		ns
t_{AH}	Address Hold from CLK Rise	0		0		ns
t_{CKO}	Clock Rise to Output Data		25		30	ns
t_{OES}	\overline{OE} Set-Up to CLK Rise	20		25		ns
t_{OEH}	\overline{OE} Hold from CLK Rise	10		15		ns
t_{COV}	Clock Rise to Output Valid		25		30	ns
t_{COZ}	Clock Rise to High Z Output		25		30	ns
t_{OEV}	\overline{OE} LOW to Output Valid		25		30	ns
t_{OEZ}	\overline{OE} HIGH to High Z Output		25		30	ns
t_{IW}	\overline{INIT} Pulse Width	15		18		ns
t_{IDV}	\overline{INIT} LOW to Data Valid		30		35	ns
t_{ICR}	\overline{INIT} Recovery to CLK	15		18		ns

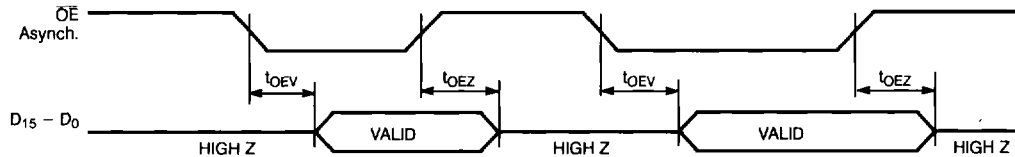
Switching Waveforms

Read Operation Timing Diagram⁶



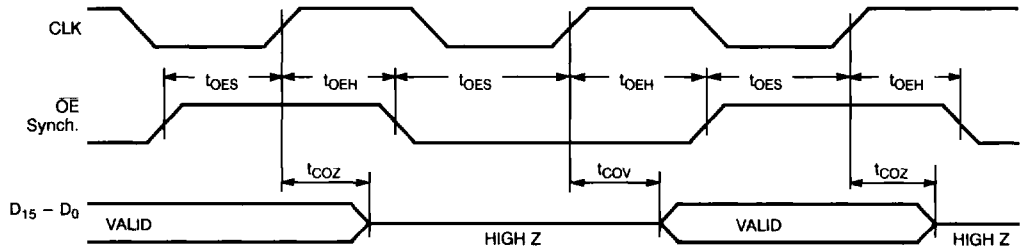
C272-7

Asynchronous Output Enable

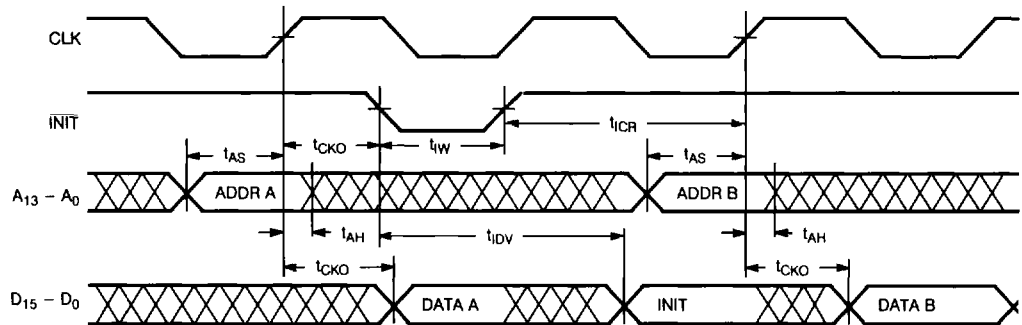


C272-8

Notes:
6. \overline{OE} assumed active

Switching Waveforms (continued)
Synchronous Output Enable


C272-9

Asynchronous Initialization Timing Diagram^[6]


C272-10

Architecture Configuration Bits

The CY7C272 has two user-programmable options in addition to the reprogrammable data array. For detailed programming information, contact your local Cypress representative.

The first programmable option determines the operation of the output enable. When this control bit is programmed with a 0, the output enable operates asynchronously. When this control bit is programmed with a 1, the output enable operates synchronously. The initialization word is also user-programmable.

Control Option	Control Word		Function
	Bit	Programmed Level	
OS	D ₀	0 1	\overline{OE} Asynchronous \overline{OE} Synchronous

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
3FFF	Data
4000	Control Word
4001	Initialization Word

Control Word (4000H)

 D_{15} D_0
 X X X X X X X X X X X X X X X X OS

Erase Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C272 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) or 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating the exposure time would be approximately 35 minutes. The 7C272 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please

see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Program Mode Table

Mode	V _{PP}	PGM	V _{FY}	D ₀ - D ₁₅
Program Inhibit	V _{PP}	V _{IHP}	V _{IHP}	High Z
Program Enable	V _{PP}	V _{ILP}	V _{IHP}	Data
Program Verify	V _{PP}	V _{IHP}	V _{ILP}	Data

Table 2. Signature Mode Table

Signature Mode	A ₀	A ₉	D ₀ - D ₁₅
Cypress Code	V _{ILP}	V _{PP}	0034 (hex)
Device Code	V _{IHP}	V _{PP}	0016 (hex)

Table 3. Configuration Mode Table^[7]

Mode	V _{PP}	PGM	V _{FY}	A ₂	A ₄	D ₀ - D ₁₅
Program Inhibit	V _{PP}	V _{IHP}	V _{IHP}	X	X	High Z
Program Control Word	V _{PP}	V _{ILP}	V _{IHP}	V _{PP}	V _{ILP}	Control Word
Verify Control Word	V _{PP}	V _{IHP}	V _{ILP}	V _{PP}	V _{ILP}	Control Word
Program Init Word	V _{PP}	V _{ILP}	V _{IHP}	V _{ILP}	V _{PP}	Init Word
Verify Init Word	V _{PP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{PP}	Init Word

Notes:

7. X = "don't care" but not to exceed V_{CC} ±5%.

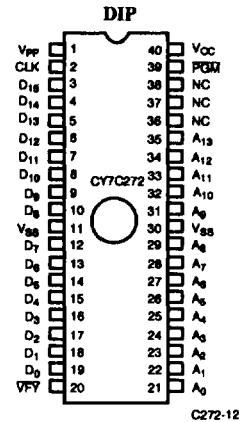
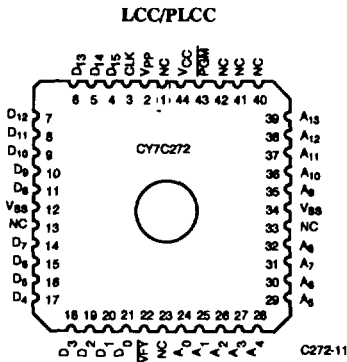


Figure 1. Programming Pinouts

Ordering Information^[8]

Speed (ns)		Ordering Code	Package Type	Operating Range
t _{AS}	t _{CKO}			
25	25	CY7C272-25DC	D18	Commercial
		CY7C272-25HC	H67	
		CY7C272-25JC	J67	
		CY7C272-25PC	P17	
		CY7C272-25WC	W18	
30	30	CY7C272-30DC	D18	Commercial
		CY7C272-30HC	H67	
		CY7C272-30JC	J67	
		CY7C272-30PC	P17	
		CY7C272-30WC	W18	
		CY7C272-30DMB	D18	Military
		CY7C272-30HMB	H67	
		CY7C272-30LMB	L67	
		CY7C272-30QMB	Q67	
		CY7C272-30WMB	W18	

Notes:

8. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t _{AS}	7, 8, 9, 10, 11
t _{AH}	7, 8, 9, 10, 11
t _{CKO}	7, 8, 9, 10, 11
t _{OES}	7, 8, 9, 10, 11
t _{OEH}	7, 8, 9, 10, 11
t _{COV}	7, 8, 9, 10, 11
t _{OEV}	7, 8, 9, 10, 11
t _{IW}	7, 8, 9, 10, 11
t _{IDV}	7, 8, 9, 10, 11
t _{ICR}	7, 8, 9, 10, 11

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