MICRONAS

T-75-33-05

MAS 7844
AMPS/TACS MODEM
CMOS

APPLICATIONS:

AMPS/TACS mobile phones

FEATURES:

- Single chip modem
- Bus compatible version for Intel and Motorola MP:s
- 10 ms interrupt timer
- Internal bit and frame synchronization
- Manchester encoding / decoding
- Byte (parallel) interface for data and controls
- SAT filtering, regeneration, freguency detection (5970, 6000 or 6030 Hz)
- Busy / idle bit separation from data flow
- Framing error detection
- Dotting detection
- 19.2 kHz for external UART
- Low power (40 mW typical)
- Stand by mode (20 mV typical)
- Single voltage (5V)
- 28 PIN PLCC or DIP

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GENERAL DESCRIPTION (Referring to the pictures on pages 3 and 6)

The TACS/AMPS modem is a one chip modem for TACS/AMPS networks. The modem is compatible with most 8-bit CMOS microprocessors. Intel/Motorola modes are packaging options. TACS/AMPS mode is selected through pin 3 (T/A). The internal clock oscillator generates all clock frequencies required for the operation of the modem. The modem generates a 19.2 kHz (pin 7) for UART and also 10 ms timing interrupt for the microprocessor. The modem interfaces the micro-processor via a data bus D0 - D7 (pins 11 - 13 and 15 - 19), and control lines: write WR (pin 4), read RD (pin 5), interrupt INT (pin 6), reset RES (pin 8), address lines A0, A1 (pins 10, 9) and chip select CS (pin 20).

The data and SAT (Supervisory audio tone) signals are applied from the receiver to the modem input DI (pin 22). The data is applied through a comparator to a Manchester decoder. A digital phase-locked loop generates the bit synchronization. After a synchronization circuit locks into a frame mark and a synchronization flag is turned on in a status register. The serial data from the Manchester decoder is converted to parallel form in a serial-to-parallel register (S/P). The data from the S/P-register is fed to a receiver register (RX) where it is buffered to the microprocessor data bus. The receiver timing block generates interrupts to the microprocessor. The BCH-decoding logic is used for the error correction of the received data.

The SAT signal is applied via the DI input (pin 22) and it is filtered by a 6 kHz band-pass filter. The filtered SAT signal is fed from the output PLL1 (pin 26) to an external phase-locked loop that locks into the received SAT frequency. This signal is then routed back to the modem input PLL2 (pin 23) and into a SAT detector. The SAT detector converts the three possible SAT frequencies into two bit combination in the status register. The received SAT frequency is then fed through a digital phase-shift controller, a 6 kHz band-pass filter, a summing amplifier, and through a 16 kHz (TACS) / 20 kHz (AMPS) low-pass filter to the data output DO (pin 27).

The data to be transmitted is loaded into a transmitter register TX. From the TX register the data is fed to a parallel-to-serial register P/S. The serial data is fed to a Manchester encoder, through a summing amplifier and a 16 kHz (TACS) / 20 kHz (AMPS) low pass filter to the data output DO.

The signal from a signalling-tone (ST) generator is also fed to the summing amplifier and through the 16 kHz (TACS) / 20 kHz (AMPS) low-pass filter to the data output.

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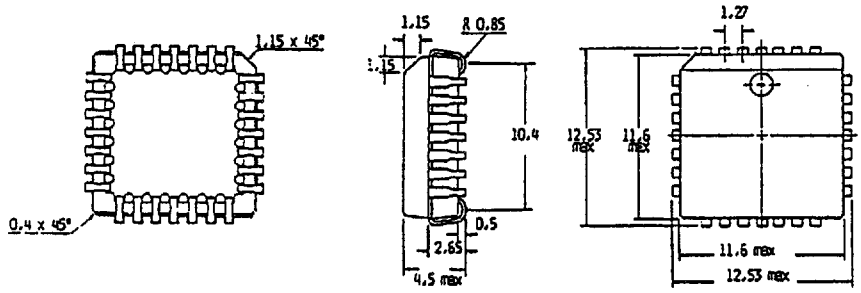
PACKAGE INFORMATION

PLCC



BOTTOM VIEW SIDE VIEW TOP VIEW

ALL DIMENSIONS: mm

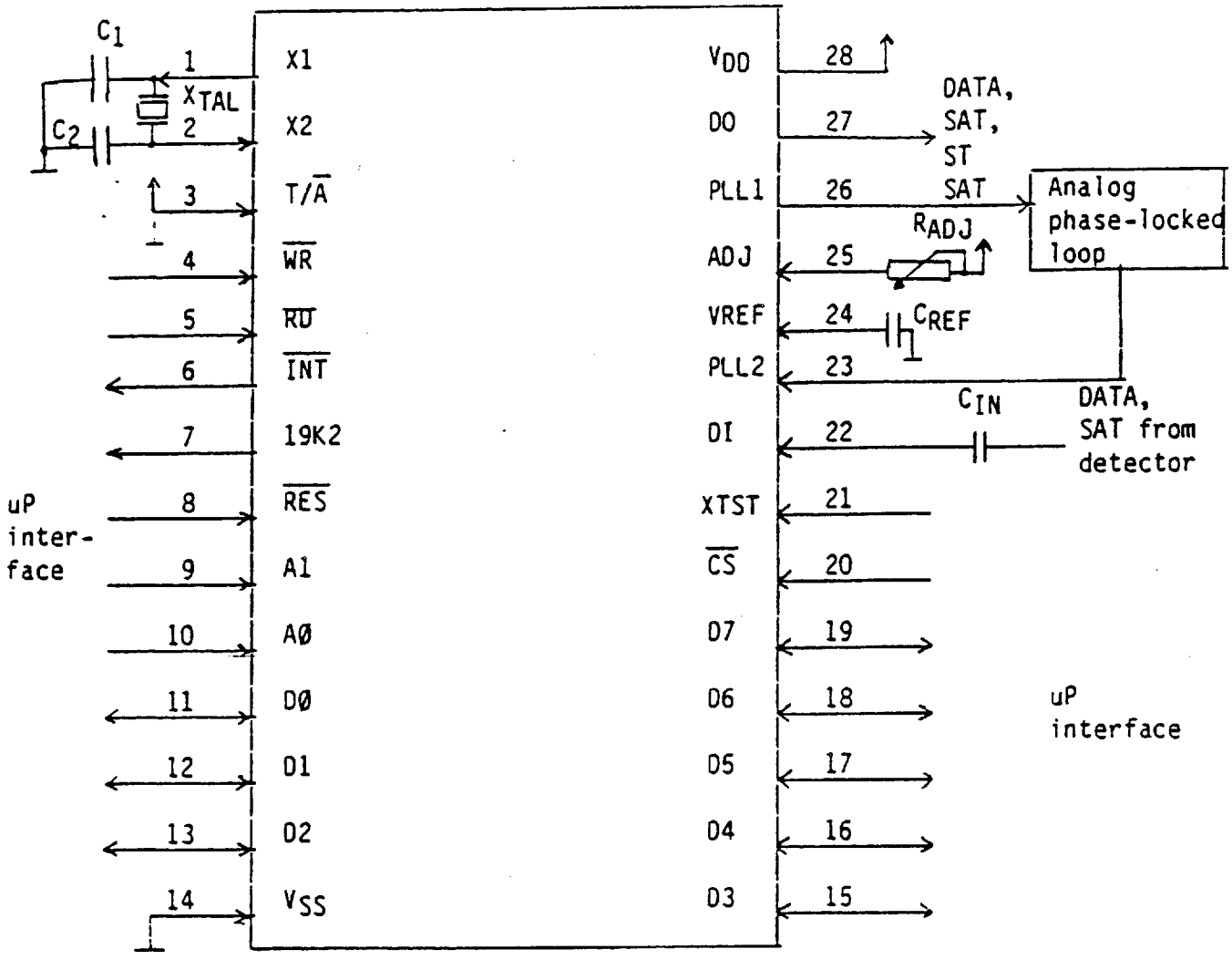
ORDERING INFORMATION

Our product code:	Product:	Package:
7844EMPD28X	MAS7844 AMPS/TACS MODEM MOTOROLA VERSION	PDIL28
7844EMPL28X		PLCC28
5A144PD28X	MAS7844 AMPS/TACS MODEM INTEL VERSION	PDIL28
5A144PL28X		PLCC28

Please refer to our product code in ordering.

Your Local Source:

3. PIN CONFIGURATION (AND EXTERNAL COMPONENTS)



Typical values of external components

C_{IN} = 2.2 nF
C_{REF} = 100 nF
R_{ADJ} = 100 k
X_{TAL} = 4.8 MHz ±100 ppm crystal
C_1 = 18 pF
C_2 = 33 pF

Analog phase-locked loop (4046) with external components.

4. INTERFACE CONFICURATION

PIN		
1	X1	Crystal oscillator output
2	X2	Crystal oscillator input
3	T/$\overline{A}$	Input for the TACS/AMPS mode selection
4	$\overline{WR}$	Write control signal
5	$\overline{RD}$	Read control signal
6	$\overline{INT}$	Interrupt output
7	19K2	19.2 kHz clock output
8	$\overline{RES}$	HW-reset input
9	A1	Two address bits (inputs) for selection of the modem registers
10	AØ	
11-13	DØ-D2	8-bit bidirectional data bus lines
15-19	D3-D7	
14	V_{SS}	Digital ground
20	$\overline{CS}$	Chip select input for controlling reading and writing of the modem registers

PIN		
21	XTST	Control signal for modem testing. In nominal conditions this input must be left open circuit. Active low.
22	DI	Audio input for the received serial data and control signals
23	PLL2	Digital input to the SAT-detector from the analog phase-locked loop
24	VREF	Signal ground
25	ADJ	Input for the data level trimming
26	PLL1	Output for the analog phase-locked loop
27	DO	Audio output for the serial data, supervisory audio tone (SAT) and signalling tone (ST)
28	V_{DD}	Supply voltage

All input and output requirements should be compatiple with 4000 B-series except pins 1, 14, 22, 24, 25, 27 and 28.

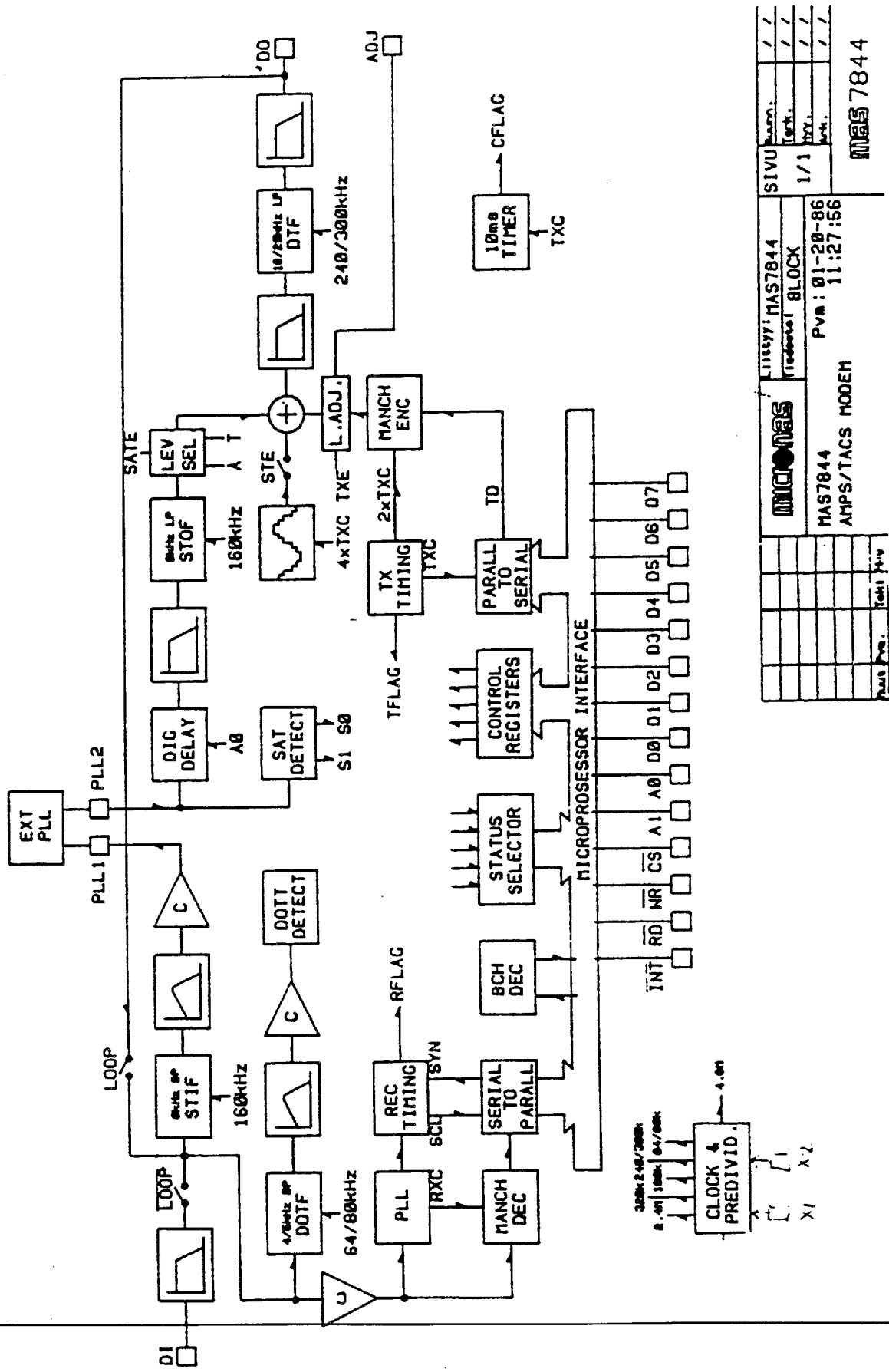
Motorola/Intel selection can be done with internal bonding of I/$\overline{M}$-pad.

RXC Clock generated from the received data (can be optionally bonded out)

NRZ Non return zero data from the Manchester encoder (can be optionally bonded out)

5. BRIEF FUNCTIONAL DESCRIPTION

5.1 Block diagram of the TACS/AMPS modem



5.2 AMPS/TACS modem registers

Intel mode register selection

Register to be addressed	A0	A1	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	$\overline{RES}$
Control register A	0	0	1	0	0	1
Control register B	1	0	1	0	0	1
Trasmitter register	0	1	1	0	0	1
BCH-register	1	1	1	0	0	1
Status register	0	x	0	1	0	1
Receiver register	1	x	0	1	0	1

Motorola mode register selection

Register to be addressed	A0	A1	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	$\overline{RES}$
Control register A	0	0	0	1	0	1
Control register B	1	0	0	1	0	1
Trasmitter register	0	1	0	1	0	1
BCH-register	1	1	0	1	0	1
Status register	0	x	1	1	0	1
Receiver register	1	x	1	1	0	1

Control register A

D7 STE Signaling tone enable

D6 SATE Supervisory audio tone loop-back enable

D5 LFS Loopfilter bandwidth select in the digital bit clock PLL. High = Narrow band, Low = Wide band.

D4 C/$\overline{V}$ Control signal for either control or voice channel signaling. Busy/Idle bits are removed from the received data stream on the control channel. When C/$\overline{V}$ = 1, B/$\overline{I}$ is selected in the status register; otherwise DS is selected.

D3	A/$\overline{B}$	Selects data stream A or data stream B on the control channel.
D2	CSR	Reset syndrome register in the BCH decoder with a low to high transition.
D1	CSF	Clear word sync flag with a low to high transition.
D0	CCF	Clear 10 ms timer interrupt flag with a low to high transition.

Control register B

D7	RINTE	Receiver interrupt enable
D6	TINTE	Transmitter interrupt enable
D5	CINTE	Timer interrupt enable. When CINTE is "Ø", then 10 ms timer is held in reset.
D4	SHM	Sets hunt mode, when "1" is written to SHM. After this a "Ø" must be written to SHM. Enables the "sync" signal to reset the receiver frame counter. Sets the loopfilter in the bitclock PLL to "wideband" and enables the pseudo bitclock in the PLL. When word sync has been found the sync signal is disabled and the PLL uses its own bitclock as a reference. During hunt mode-RFLAG is kept reset.
D3	LOOP	Output connected to the input
D2	S/$\overline{B}$	Selects either SØ, S1 from the SAT detector or WØ, W1 from the BCH decoder to the status register.
D1	SPS	SAT phase shift counter incremet bit. When "1" is written to SPS, SAT phase is shifted 6.75°.
D0	STBY	Sets the circuit in stand by mode (low power).

Status register

D7	B/$\overline{I}$ or DS	B/$\overline{I}$ signal is high when two of the last three Busy/Idle bits have been high. This applies only if C/$\overline{V}$ is high (receiving a message on the control channel). DS signal goes high 2 ±0.5 ms after a dotting sequence has started.
D6 D5	SØ/WØ S1/W1	The different combinations of SØ and S1 determines the received SAT signal

S1	SØ	
0	0	5970 Hz
0	1	6000 Hz
1	0	6030 Hz
1	1	No SAT received

The different combination of WØ and W1 determines frame errors as follows:

W1	WØ	
0	1	Errors detected in frame
1	0	Possible to correct one error
1	1	Correct frame
0	0	Impossible state

D4	TXE	Transmission is enabled
D3	RFLAG	This flag goes high every time the RX register contains a new 8 bit byte of data
D2	TFLAG	This flag goes high whenever the TX register is able to receive new data from the microprocessor
D1	CFLAG	This flag goes high every 10 ms after the timer has been started with CINTE. It has to be cleared with CCF before the next interrupt.
DØ	SFLAG	This flag goes high every time the word sync detector detects a correct word sync pattern. It is cleared with CSF. In the control channel SFLAG is cleared internally at the end of the frame.

5.3 Functional description of blocks

5.3.1 Oscillator and prescaler

Oscillator runs with a 4.8 MHz external crystal. Prescaler generates 19.2 kHz clock signal for external use and all internal clock signals.

5.3.2 Microprocessor interface

The function of the uP interface is to organize communication between the modem and the microprocessor. I/$\overline{M}$ seletcs suitable interface signals for different processors. Signals $\overline{CS}$, AØ, A1 and $\overline{WR}$ or $\overline{RD}$ are used to control the access to the different registers inside the modem chip (see tables on page 7). $\overline{INT}$ line is used to detect interrupts caused by the receiver, the transmitter or the timer. $\overline{RES}$ line is the master reset of the circuit.

Interface consist signals:

$\overline{WR}$ - write signal
$\overline{RD}$ - read signal
I/$\overline{M}$ - Intel/Motorola mode selection. Normally in Motorola mode, can be changed to Intel mode with an internal bonding.
$\overline{CS}$ - chip select
AØ,A1 - address lines
$\overline{RES}$ - master reset signal
$\overline{INT}$ - interrupt signal

Internal signals in the microprocessor interface:

CAE	Control register A enable
CBE	Control register B enable
TDE/CTF	Transmit data register enable/ clear transmitter flag
BDE	BCH decoder register enable
$\overline{S}$/D	Enables either status or data to the microprocessor bus
BE	Bus enable
STF	Set transmitter flag
CRF	Clear transmitter flag
RINTE	Receiver interrupts enabled (from CRB)
RFLAG	Receiver flag (from receiver timing)
TINTE	Transmitter interrupts enabled (from CRB)
TFLAG	Transmitter flag (from transmitter timing)
CINTE	Clock interrupts enabled
CFLAG	10 ms timer clock flag

Interrupts:

	Motorola mode operation $\overline{INT}$ =	Intel mode operation INT =
Receiver interrupt	RINTE and RFLAG	RINTE and RFLAG
Transmitter interrupt	TINTE and TFLAG	TINTE and TFLAG
Clock interrupt	CINTE and CFLAG	CINTE and CFLAG

5.3.3 Control register A

Control register A transfers data bits from the data bus to the desired modules.

CRA consists of

D7 STE — Signalling tone transmission enable. Data transmission is disabled.

D6 SATE — Supervisory audio tone transmission enable.

D5 LFS — Loopfilter bandwith select in the digital bit clock PLL.

LFS	bandwidth
Ø	wide
1	narrow

D4 C/$\overline{V}$ — Control or voice channel selection.

C/$\overline{V}$	selected status
Ø	DS
1	B/$\overline{I}$

D3 A/$\overline{B}$ — A or B data stream selection on the control channel.

D2 CSR — Clear the syndrome register in the BCH decoder with a low to high transition.
Note: After clearing the BCH decoder, it's not allowed to write to the BCH decoder before 10 microseconds.

D1 CSF — Clear the word sync flag with a low to high transition.

DØ CCF — Clear the 10 ms timer interrupt flag (CFLAG) with a low to high transition.

Note: Time period between two clearing operations of the syndrome register, the word sync flag or the 10 ms timer interrupt must be more than 20 microseconds.

5.3.4 Control register B

Control register transfers data bits from the data bus to the desired modules.

CRB consists of

D7	RINTE	Receiver interrupts enable
D6	TINTE	Transmitter interrupts enable
D5	CINTE	Clock interrupts enable
D4	SHM	Set hunt mode. Sets the loopfilter in the bitclock PLL to wideband. During hunt mode RFLAG is kept reset.
D3	Loop	Connects data output to the data input.
D2	S/$\overline{B}$	Selects either SAT, (SØ,S1) or BCH (WØ,W1) information to the status register.
D1	SPS	This signal is used as a clock for the phase shift register. The register state is a measure of phase shift on the SAT signal.
DØ	STBY	Sets the circuit in stand-by mode (low power).

5.3.5 BCH-decoder

The function of the BCH decoder is to decode the received BCH coded data. Received 40 bits data frame is clocked to the BCH decoder in serial form along data line DØ. The most significant bit is clocked first after reset by CSR in the CRA. After all 40 data bits and one extra zero have been clocked in, the output bits W1, WØ in the STR can be examined.

W1, WØ having the value 1,1 indicates that the frame is correct. W1, WØ having the value 0,1 that there are errors in the frame and the BCH is shifted by clocking zeroes in it until W1, WØ changes from 0,1 to 1,0. When this happens, the number of clocked zeroes indicates the position of the bit to be changed. If the status does not change from 0,1 to 1,0 after 40 zeroes have been clocked in, it is not possible to correct the frame. State 0,0 is impossible.

5.3.6 Serial to parallel register

The function of the S/P register is to change the received serial data to 8 bit wide data bytes.

5.3.7 Status and receiver register

The function of the STR and RX register is to transfer status or data bits to the data bus.

5.3.8 10 ms Timer

The function of this timer is to produce 10 ms clock for real time software system along the $\overline{INT}$ line. When CINTE in the CRB goes "high" it enables the timer. CFLAG in the STR goes "high" after every 10 ms and causes an interrupt. CFLAG is cleared with CCF in the CRA.

5.3.9 Transmitter register

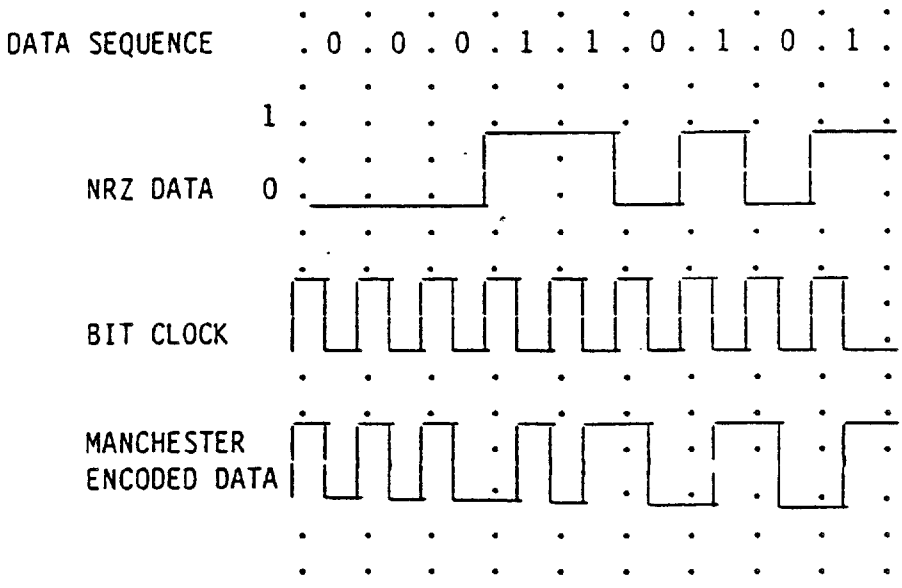
The transmitter register is a buffer for the data to be transmitted.

5.3.10 Parallel to serial register

The function of the P/S register is to change 8 bit data bytes to serial form. The data is moved out with a 8 or 10 kHz clock when STBY is "high".

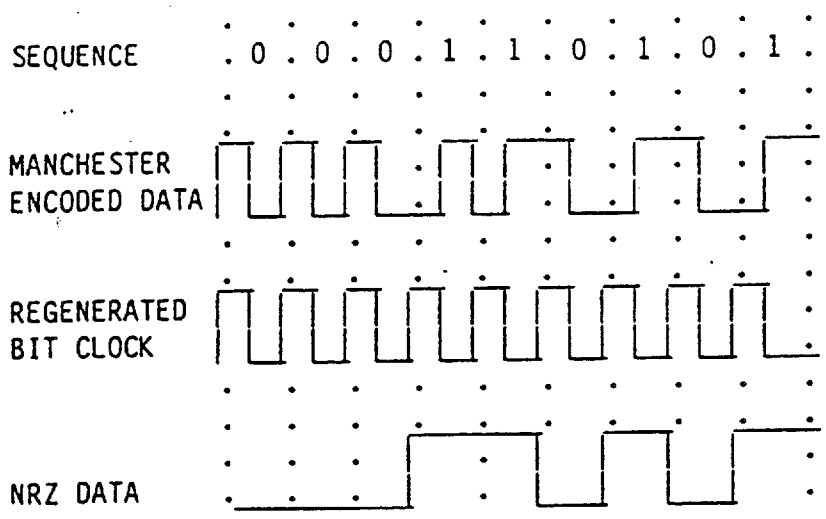
5.3.11 Manchester encoder

The function of the manchester encoder is to change the NRZ data to manchester code. NRZ binary one is transformed to zero-to-one transition and NRZ binary zero is transformed to one-to-zero transition.



5.3.12 Manchester decoder

The function of the manchester decoder is to decode the manchester coded data to NRZ data.



5.3.13 SAT phase shift register

The function of the sat phase shift register is to adjust phase difference between the incoming and the outgoing SAT. With 27 sps (SAT phase shift) pulses phase shift can be adjusted ±180° (6.75° per one sps).

5.3.14 Signalling tone generator

The function of the signalling tone generator is to produce two clock signals to the two bit D/A converter which output must be filtered to 8 kHz (TACS) or 10 kHz (AMPS) sine wave. When STE is high it enables signalling tone and disables TXD.

5.3.15 Dotting detector

The function of the dotting detector is to indicate the incoming data stream in the voice channel.

The received frame in the voice channel starts with a 101 bits long dotting sequence. After 2 ±0.5 ms beginning of the dotting sequency bit DS in STR should go high.

5.3.16 SAT detector

The function of the SAT detector is to indicate which SAT frequency is received. SAT detectors outputs S1, SØ are in STR. The SAT frequencies must be detected as in the table on next page.

	SAT	S1, SØ
F < F1	no valid SAT	1 , 1
	F1=5955 ± 5 Hz	
F1 ≤ F < F2	SAT=5970	0 , 0
	F2=5985 ± 5 Hz	
F2 ≤ F < F3	SAT=6000	0 , 1
	F3=6015 ± 5 Hz	
F3 ≤ F ≤ F4	SAT=6030	1, 0
	F4=6045 ± 5 Hz	
F4 ≤ F	no valid SAT	1 , 1
F4 ≤ F	no valid SAT	1 , 1

5.3.17 Digital phase locked loop

The function of the digital phase locked loop is to synchronize the phase of the receiver clock with the "pseudo-clock" recovered from the incoming data stream. The bandwidth of the DPLL can be set to narrow mode with LFS bit in the CRA. The digital phase locked loop tolerates less than ± 90° phase shift in the data i.e. ± 25 us in AMPS mode and ± 31 us in TACS mode.

5.3.18 Receiver timing

The function of the receiver timing is to mask out data bits for RX and Busy/Idle bits for Busy/Idle detector (see pictures on pages 20 and 21). The receiver timing is set to the right mode with the bits C/$\overline{V}$, A/$\overline{B}$ and SHM.

5.3.19 Word sync detector

The function of the word sync detector is to detect a 11 bit word synchronization sequence 11100010010. SFLAG in the STR goes "high" when this sequency is found.

5.3.20 The 8-bit data bus (DØ...D7)

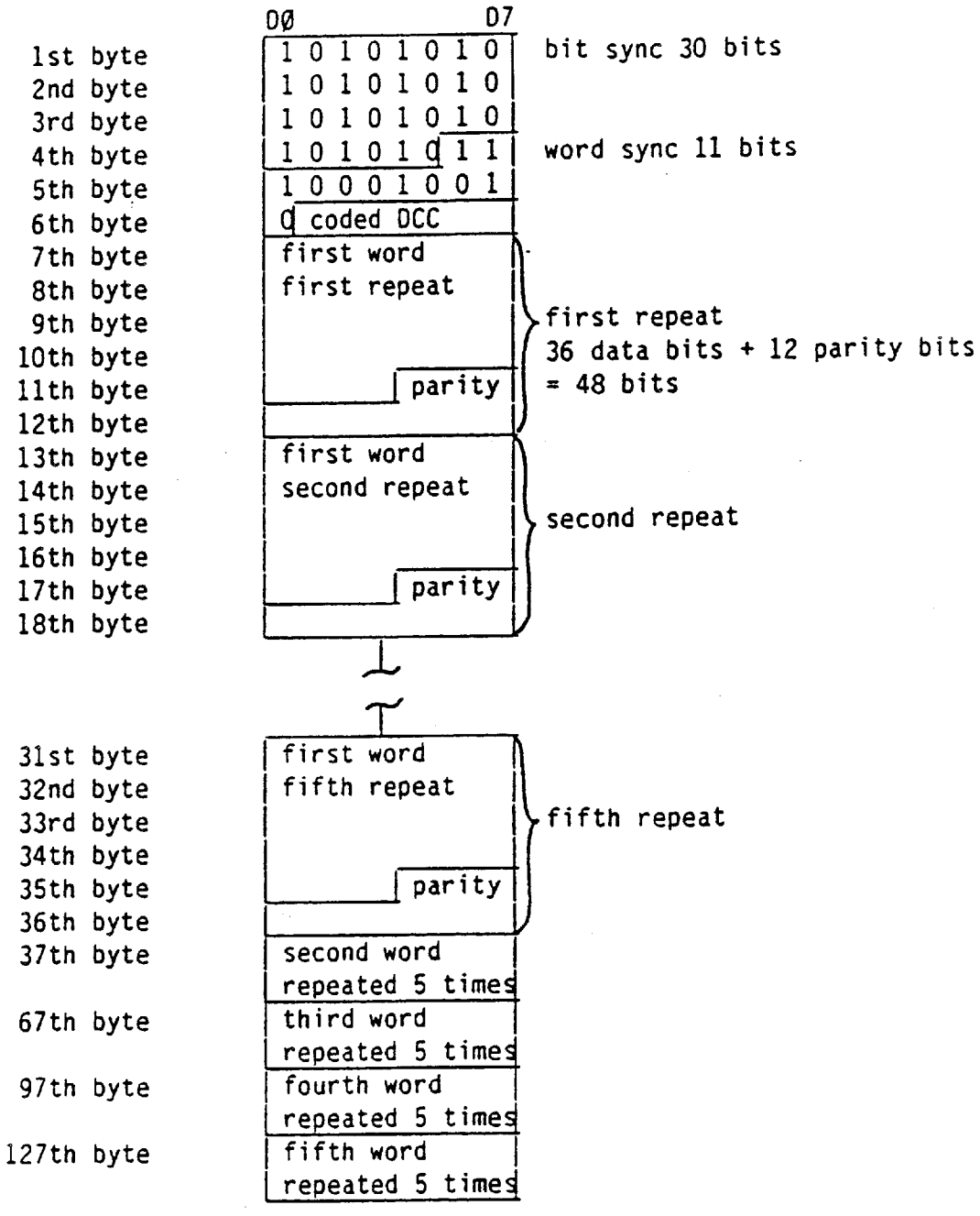
A bidirectional bus is used to write or read selected registers.

5.3.21 Transmit timing

When transmission is not being performed the transmit counter is disabled and the TFLAG is "high" and the TXE is "low". Transmission is started by writing TINTE high, which causes interrupt to the processor. The processor writes the first byte to the TX register and TFLAG goes "high" causing prosessor to write the next byte to the TX register. Transmission is ended when the processor stops writing.

5.5 Modem data transfer

5.5.1 Data transmission, reverse control channel



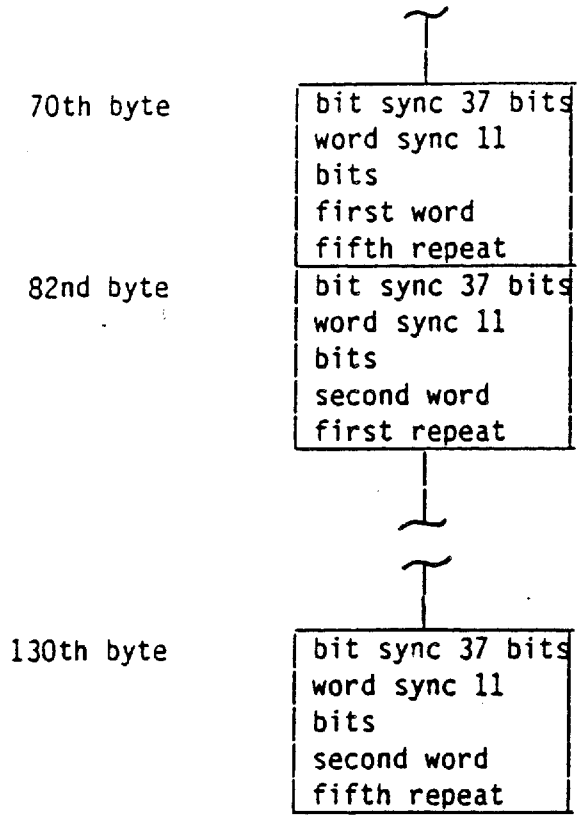
coded DCC received DCC	7-bit coded DCC
0 0	0 0 0 0 0 0 0
0 1	0 0 1 1 1 1 1
1 0	1 1 0 0 0 1 1
1 1	1 1 1 1 1 0 0

Message can consist of one to five (TACS) or seven (AMPS) words.

5.5.2 Data transmission, reverse voice channel

Data is transferred from the CPU to the modem in parallel form (8 bits data at time).

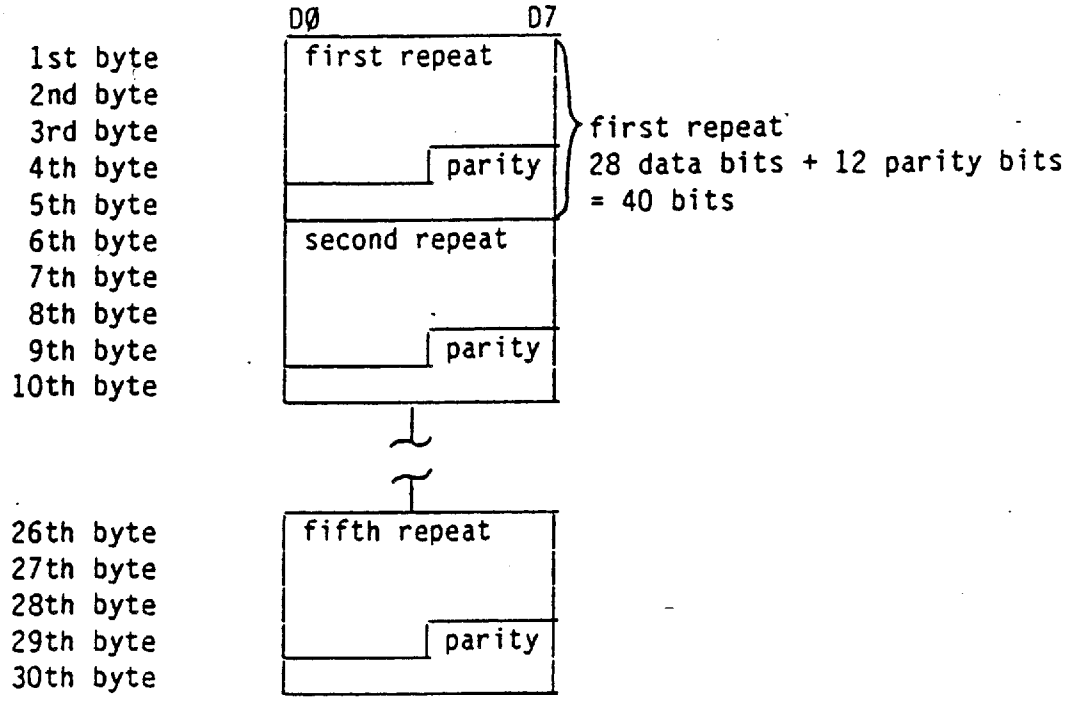
	D0 D7	
1st byte	1 0 1 0 1 0 1 0	bit sync 101 bits
2nd byte	1 0 1 0 1 0 1 0	
3rd byte	1 0 1 0 1 0 1 0	
4th byte	1 0 1 0 1 0 1 0	
5th byte	1 0 1 0 1 0 1 0	
6th byte	1 0 1 0 1 0 1 0	
7th byte	1 0 1 0 1 0 1 0	
8th byte	1 0 1 0 1 0 1 0	
9th byte	1 0 1 0 1 0 1 0	
10th byte	1 0 1 0 1 0 1 0	
11th byte	1 0 1 0 1 0 1 0	
12th byte	1 0 1 0 1 0 1 0	
13th byte	1 0 1 0 1 1 1 1	word sync 11 bits
14th byte	0 0 0 1 0 0 1 0	
15th byte	first word	first repeat
16th byte	first repeat	
17th byte		
18th byte		36 data bits + 12 parity bits
19th byte	parity	= 48 bits
20th byte		
21st byte	1 0 1 0 1 0 1 0	bit sync. 37 bits
22nd byte	1 0 1 0 1 0 1 0	
23rd byte	1 0 1 0 1 0 1 0	
24th byte	1 0 1 0 1 0 1 0	
25th byte	1 0 1 0 1 1 1 1	word sync 11 bits
26th byte	0 0 0 1 0 0 1 0	
27th byte	first word	second repeat
28th byte	second repeat	
29th byte		
30th byte		
31st byte	parity	
32nd byte		
33rd byte	1 0 1 0 1 0 1 0	bit sync 37 bits
34th byte	1 0 1 0 1 0 1 0	
35th byte	1 0 1 0 1 0 1 0	
36th byte	1 0 1 0 1 0 1 0	
37th byte	1 0 1 0 1 1 1 1	word sync 11 bits
38th byte	0 0 0 1 0 0 1 0	
39th byte	first word	
40th byte	third repeat	
41st byte		
42nd byte		
43rd byte	parity	
44th byte		

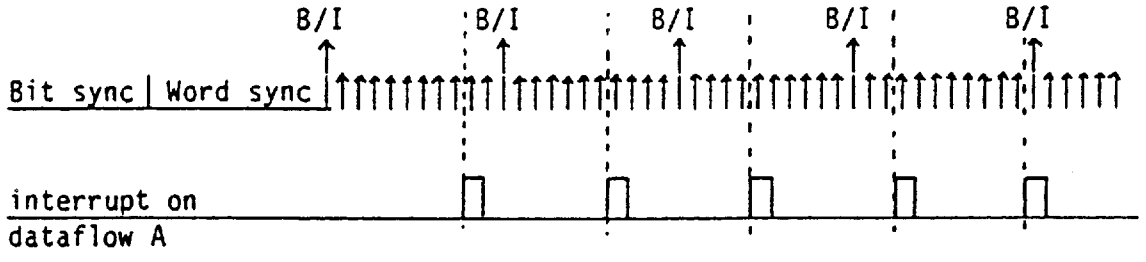


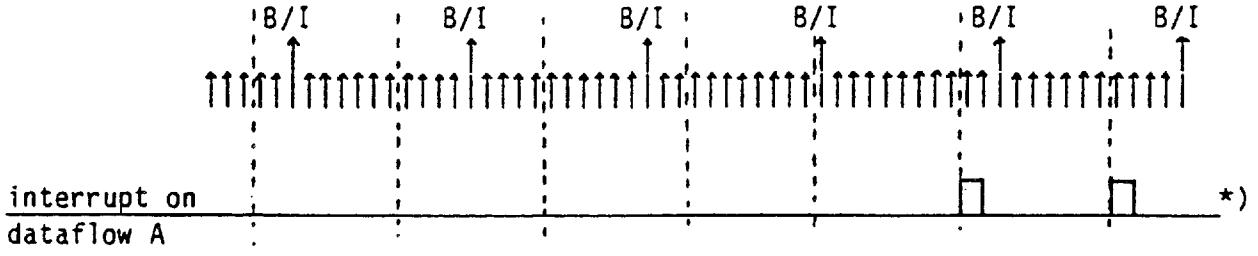
Message can consist of one or two (TACS) or four (AMPS) words.

5.5.3 Data reception, forward control channel

Reception is started by initiating "Hunt mode". When synchronization pattern is found the SFLAG signal goes high. After that, if RINTE enables, receiving interrupt occurs after every eight bits received either from data flow A or B choosed by the processor. Also every 10th bit in data (Busy/Idle) is masked away before transfering to the processor.







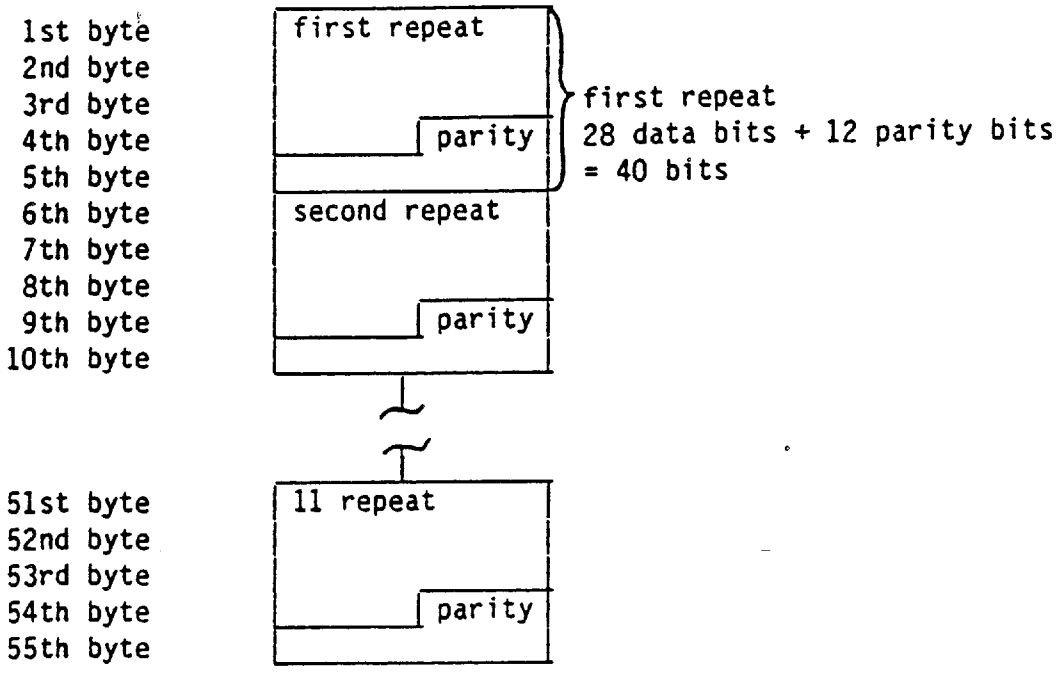
*) Interrupts are missing when dataflow B is received.

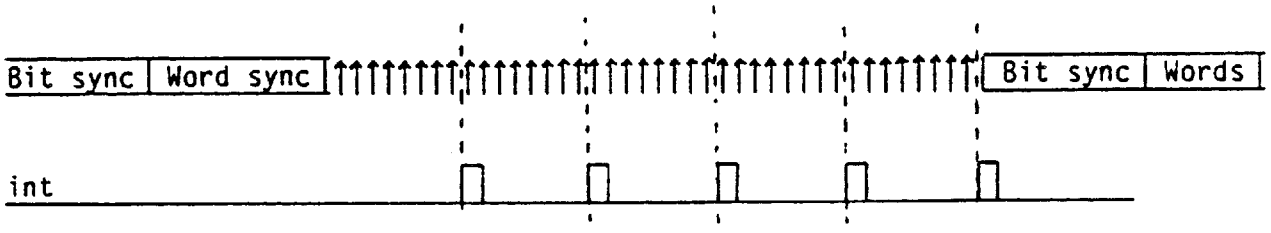
↑ = data bit

| = Busy/Idle bit

5.5.4 Data reception, forward voice channel

Reception is started by initiating "Hunt mode". When synchronization pattern is found the SYNC signal goes high. After that, if RINTE enables, receiving interrupt occurs after every eight bits received. "Hunt mode" must be initiated after every repeat of the word.





↑ = data bit

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute maximum ratings

Supply voltage	V_{DD}	6.5 V
Input voltage	V_{IN}	-0.5 V to V_{DD} +0.5 V
Operating temperature	T_A	-35°C to +85°C
Storage temperature	T_{stg}	-55°C to +125°C
Max. power dissipations	P_{max}	400 mW

6.2 DC characteristics V_{DD} = 5 V, T_A = -35°C to +85°C, unless otherwise noted

Monolithic circuit characteristics	Symbol	Limits			Unit
		Min	Typ	Max	
Supply current	I_{DD}		5	12	mA
Supply current in stand-by mode operation				5	mA
Supply voltage	V_{DD}	4.75	5	5.25	V
Output low voltage INT, 19K2, STBY I_{OL} = 0.8 mA DØ - D7 I_{OL} = 1.6 mA NRZ, RXC, PLL1 I_{OL} = 0.3 mA	V_{OL}			0.4	V
Output high voltage INT, 19K2, STBY, NRZ, RXC, PLL1 I_{OH} = 0.2 mA DØ - D7 I_{OH} = 0.6 mA	V_{OH}	4.6			V
Short-circuit sink current INT, 19K2, STBY DØ - D7 NRZ, RXC, PLL1	 I_{OLS} I_{OLS} I_{OLS}			 35 65 15	 mA mA mA
Short-circuit source current INT, 19K2, STBY, NRZ, RXC, PLL1 DØ - D7	 I_{OHS} I_{OHS}			 10 30	 mA mA
Input low voltage	V_{IL}		2.1	0.8	V
Input high voltage	V_{IH}	3.5	2.1		V
Input current for digital signals	I_{IN}			±100	uA
Input capacitance	C_{IN}		3		pF
At DI analog input Input impedance at 6 kHz	Z_{IN}	250	400	550	k
Analog output load impedance DO	 Z_L			10 50	k pF

6.3 AC characterics of logical signals

V_{DD} = 5 V, T_A = -35°C to +85°C

R_L = 10 kohm, C_L = 50 pF (in parallel)

Intel mode (I/$\overline{M}$ = high)

Input low level	V_{IL} = 0.5 V
Input high level	V_{IH} = 2.5 V
Output low level	V_{OL} = 0.8 V
Output high level	V_{OH} = 2.0 V

Intel mode

Characterics	Symbol	Limits			Unit
		Min	Typ	Max	
$\overline{WR}$ pulse width	t_{WW}	80			ns
Data valid to trailing edge of $\overline{WR}$	t_{DW}	100			ns
Data valid after trailing edge of $\overline{WR}$	t_{WD}	40			ns
Address and chip select stabile before $\overline{WR}$	t_{AW}	30			ns
Address and chip select stabile after $\overline{WR}$	t_{WA}	20			ns
Read access time	t_{RD}			100	ns
Chip selects access time	t_{SD}			85	ns
Address access time	t_{CD}			130	ns
$\overline{RD}$ pulse width	t_{RR}	110			ns
Address and chip select hold time for $\overline{RD}$	t_{RA}	0			ns
Read to data hold	t_{DF}	0		100	ns
$\overline{RES}$ pulse width	t_{RES}	500			ns

Motorola mode ($I/\overline{M}$ = low)

Input low level	V_{IL} < 2.5 V
Input high level	V_{IH} > 2.5 V
Output low level	V_{OL} < 2.5 V
Output high level	V_{OH} > 2.5 V

Motorola mode

Characterics	Symbol	Limits			Unit
		Min	Typ	Max	
WR pulse width	t_{WW}	80			ns
Data valid to trailing edge of WR	t_{DW}	100			ns
Data valid after trailing edge of WR	t_{WD}	40			ns
Address stabile before WR	t_{AW}	30			ns
Address and chip select stabile after WR	t_{WA}	20			ns
Read access time	t_{RD}	200			ns
Read stabile after WR	t_{WR}	10			ns
Chip selects access time	t_{SD}			85	ns
Address access time	t_{CD}			130	ns
Read to trailing edge of CS	t_{RC}	10			ns
RD pulse width	t_{RR}	110			ns
Address and chip select hold time for RD	t_{RA}	0			ns
Read to data hold	t_{DF}	0		100	ns
$\overline{RES}$ pulse width	t_{RES}	500			ns

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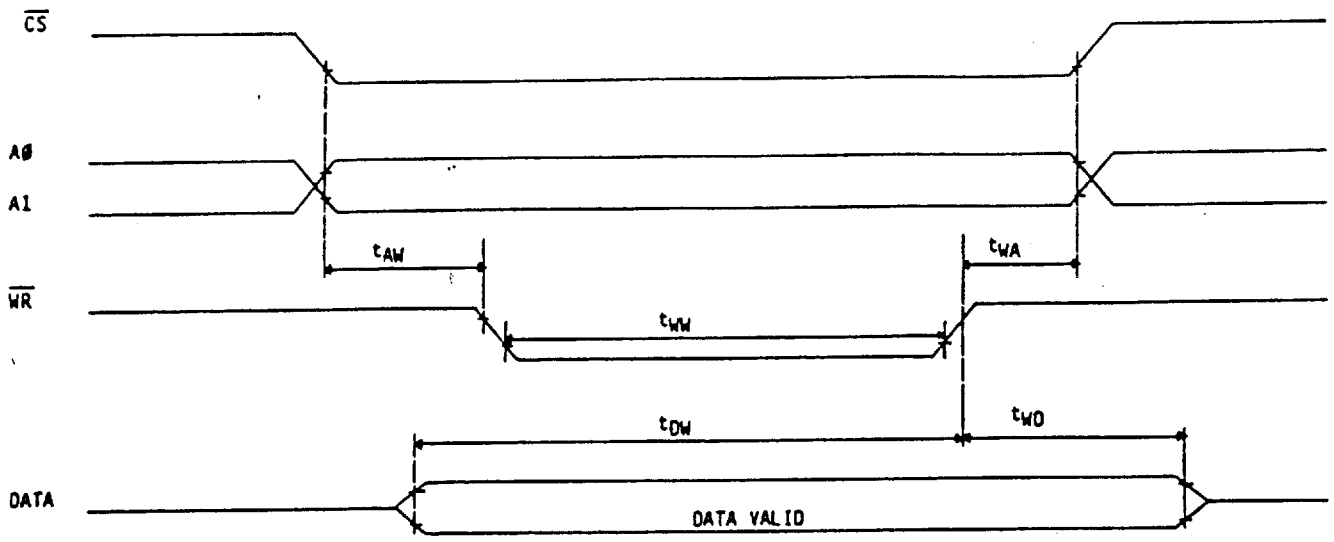
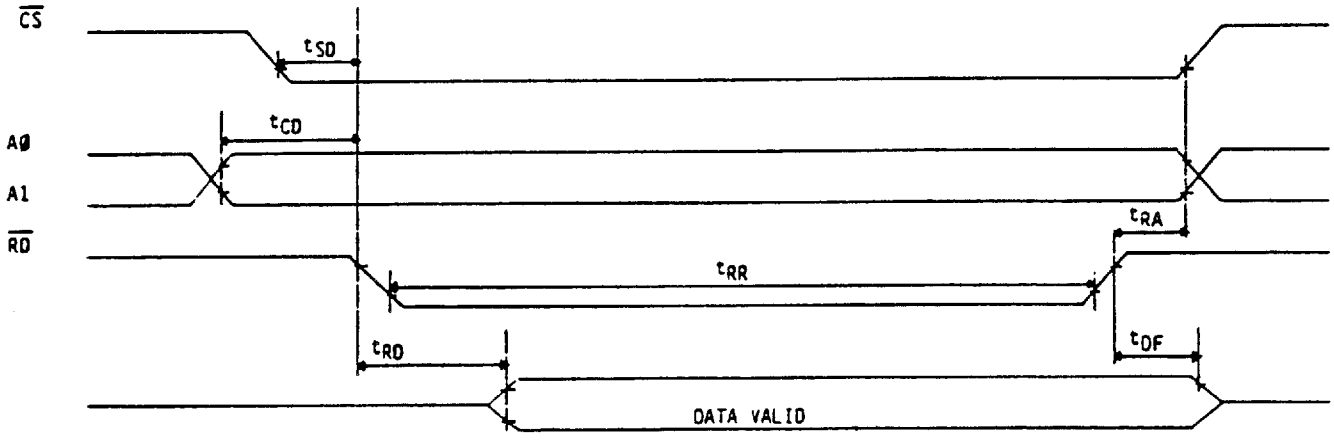
WRITE CYCLE IN INTEL MODE

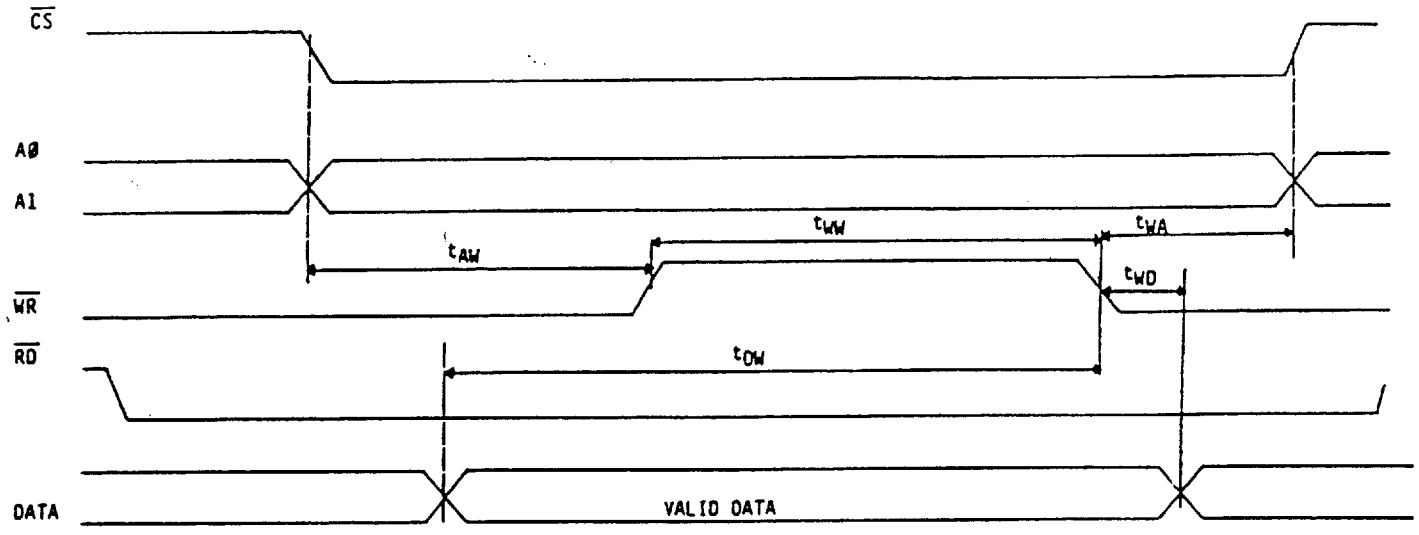


READ CYCLE IN INTEL MODE

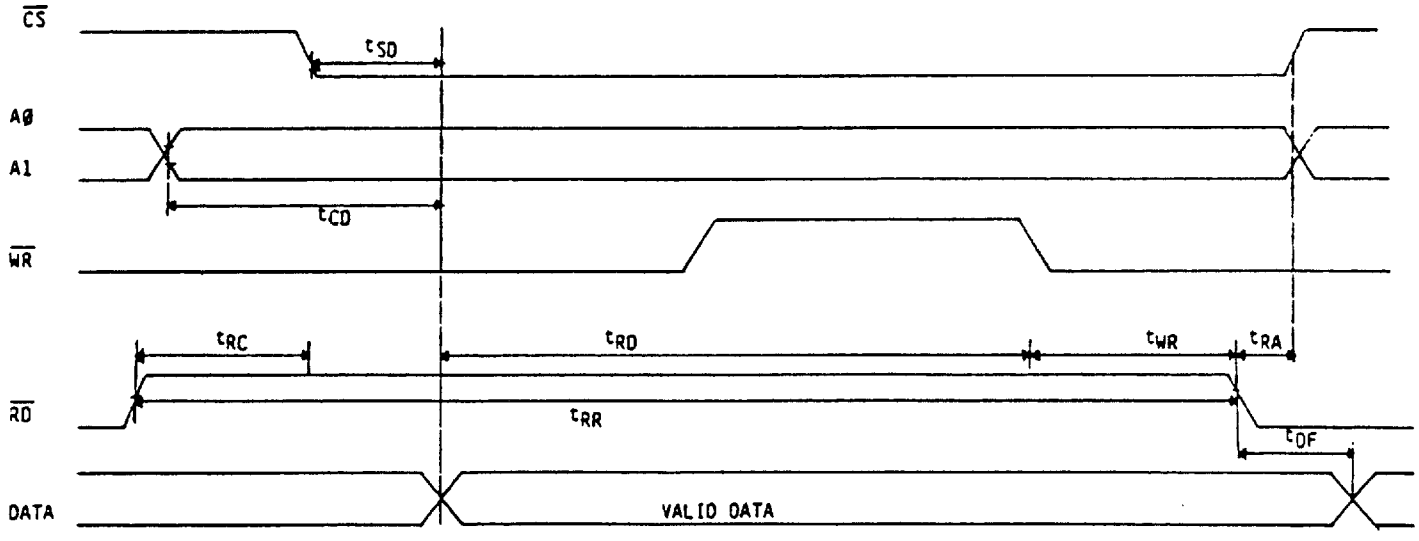


MICRONAS

WRITE CYCLE IN MOTOROLA MODE



READ CYCLE IN MOTOROLA MODE



6.4 Modem input levels (in pin DI), Z_{in} = 400 k ± 150 k at 6 kHz.

Modem input level: DATA (and dotting, see 5.3.15)

Vin, max = 566 mVpp
Vin, nom = 396 mVpp
Vin, min = 283 mVpp

Modem input level: SAT

Vin, max = 150 mVpp
Vin, nom = 105 mVpp
Vin, min = 70 mVpp

6.5 Modem output levels (in pin DO)

Nominal conditions: Tnom = +25°C
V_{DD}, nom = 4.8...5.2 V

Operating conditions: T = -35°C...+75°C
V_{DD}, nom ± 1 %

Output levels in operating conditions

ST: Vout = 2.3 Vpp ± 15 %

ratio in TACS and AMPS	STnom/ST = 1 ± 5 %	*
ratio in TACS and AMPS	STnom/WBD= 1 ± 5 %	*
ratio in TACS	STnom/SAT= 3.77 ± 5 %	*
ratio in AMPS	STnom/SAT= 4.00 ± 5 %	*

Note:
* Measured from peak to peak values in frequency range 0 - 50 kHz (first order low pass filter). In data signal peak to peak value is affected by the harmonics.

- Total noise and harmonic distortion (100 Hz...100 kHz) for ST at least 35 dB below fundamental.

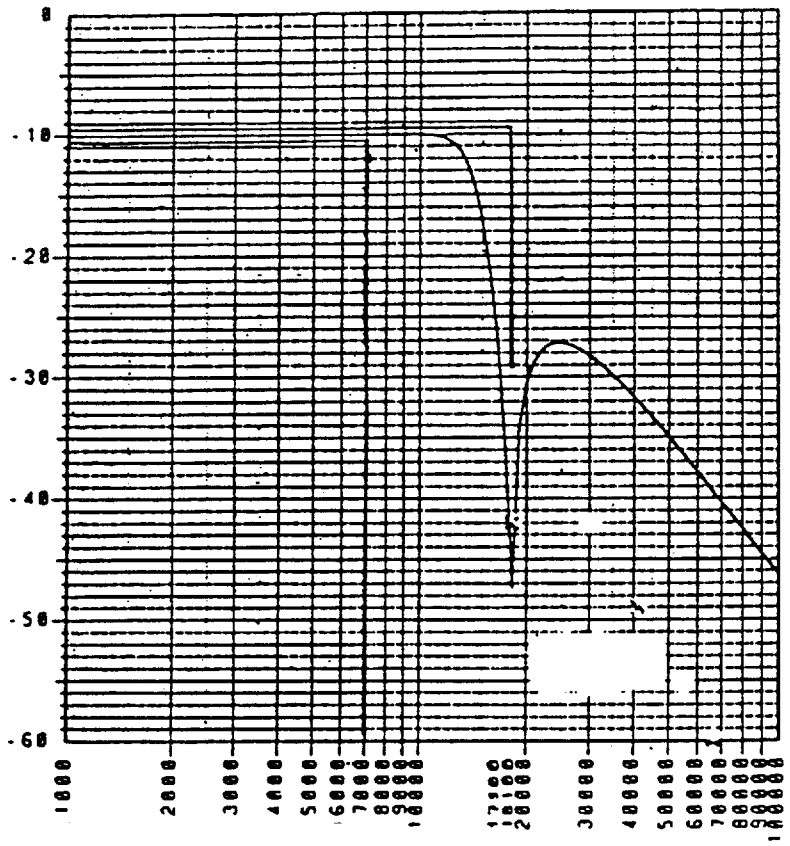
- Total noise and harmonic distortion (100 Hz...100kHz) for SAT at least 23 dB below fundamental.

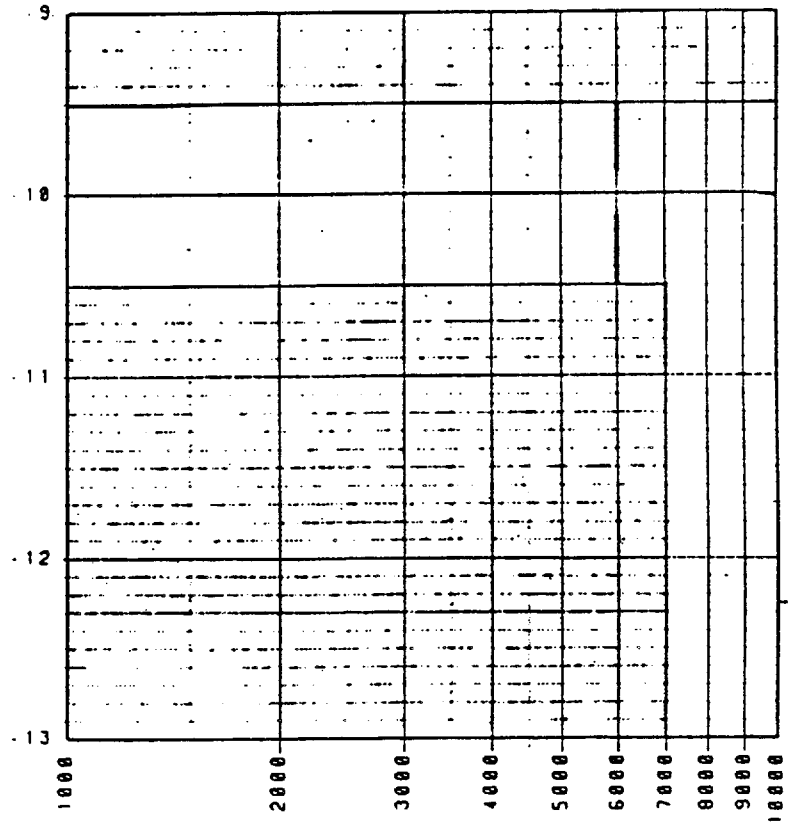
- Signalling tone (ST) frequency 8/10 kHz ± 1 Hz (TACS/AMPS).

- Wideband data rate 8/10 kHz (TACS/AMPS).

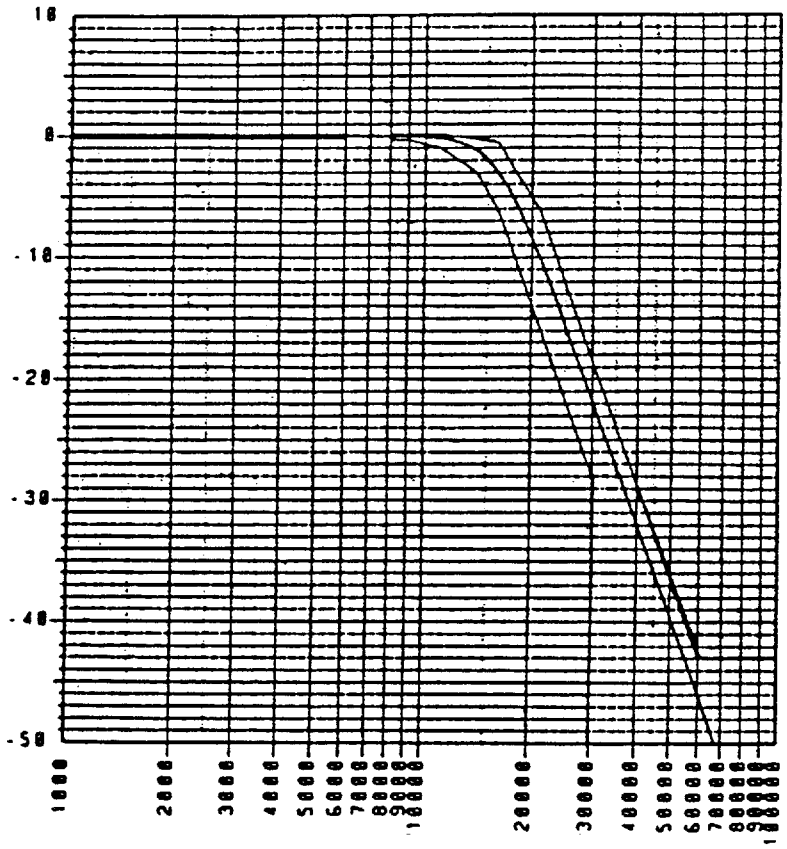
6.6 Filter characteristics

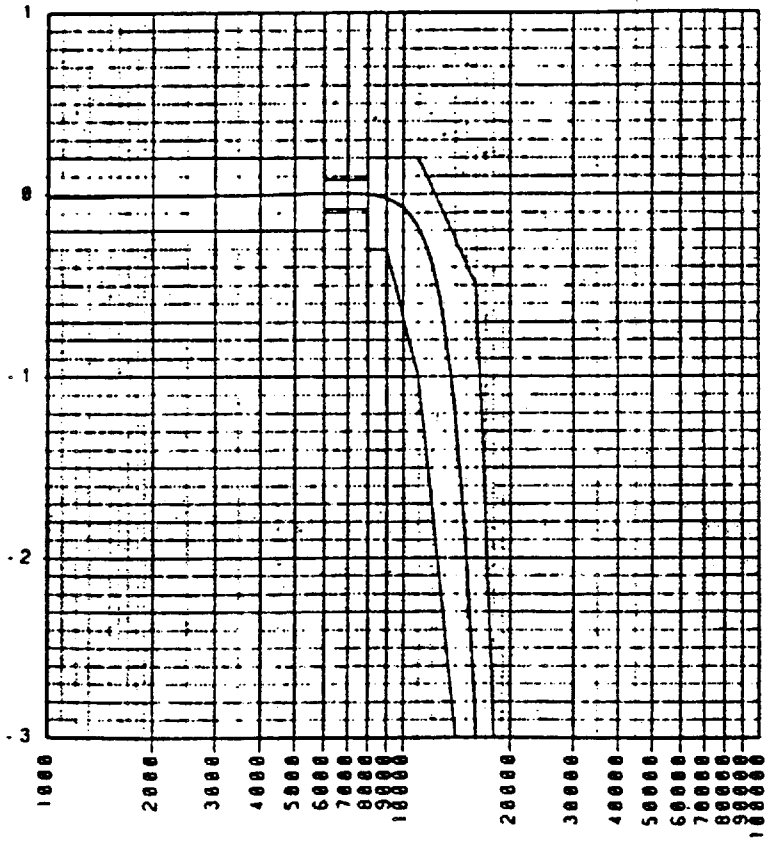
7.6.1 SAT-out filter characteristics



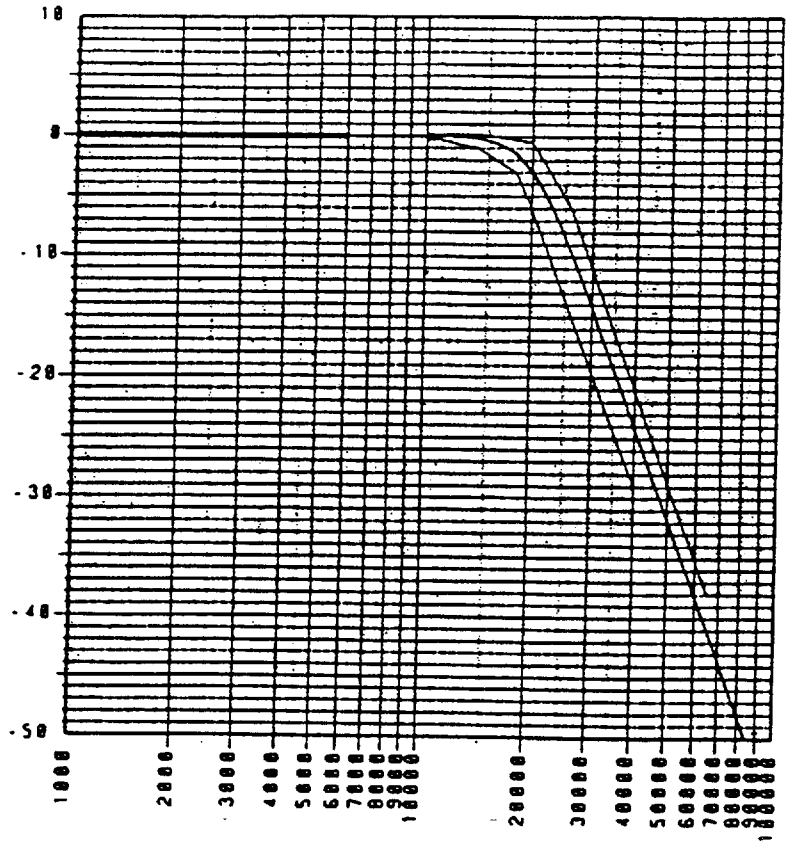


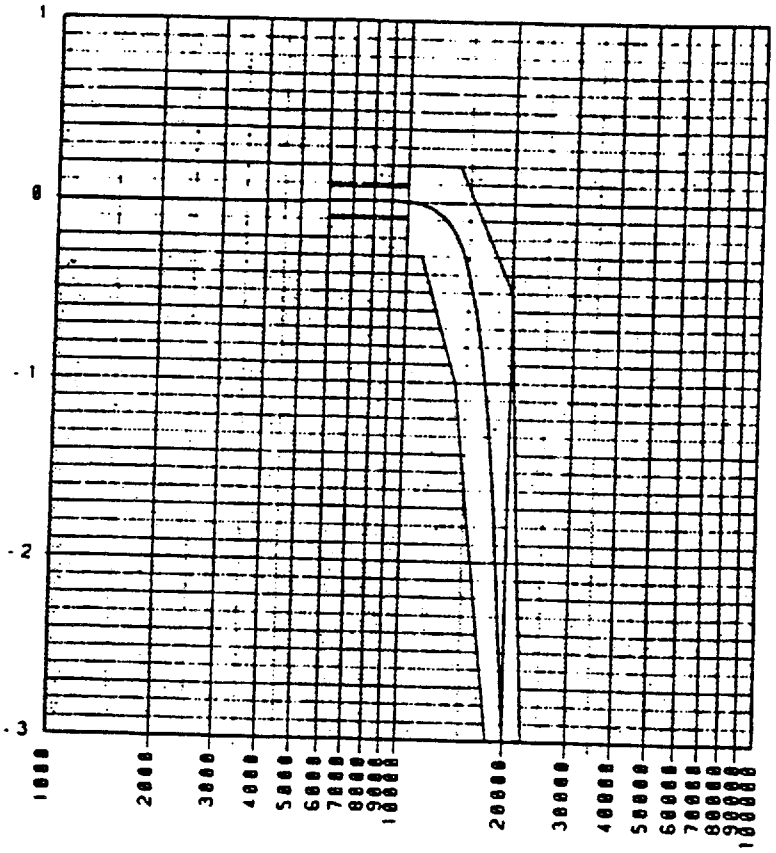
7.6.2 TACS DATA-out filter characteristics



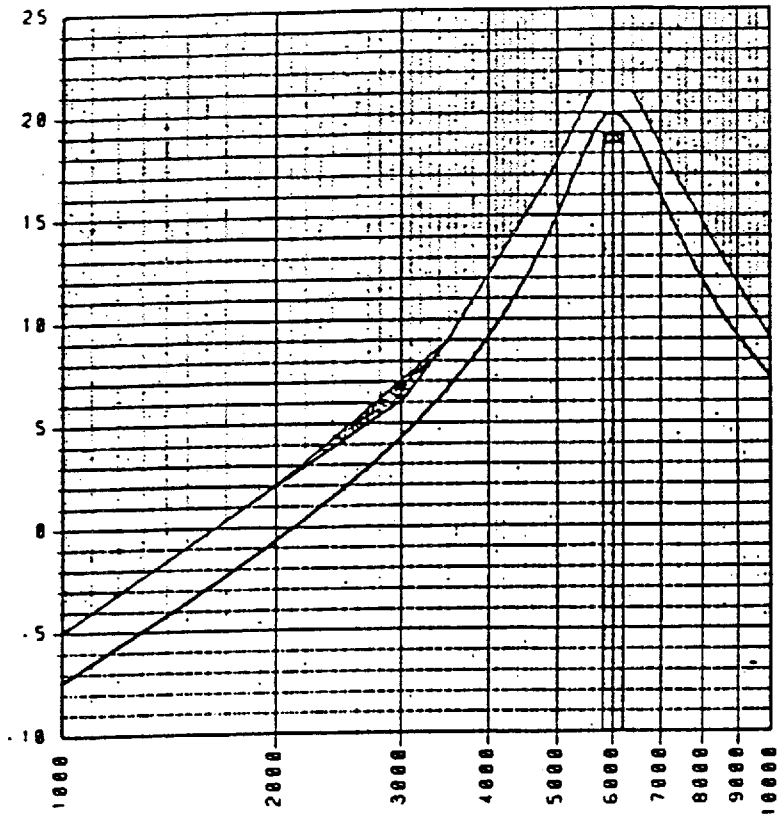


7.6.3 AMPS DATA-out filter characteristics

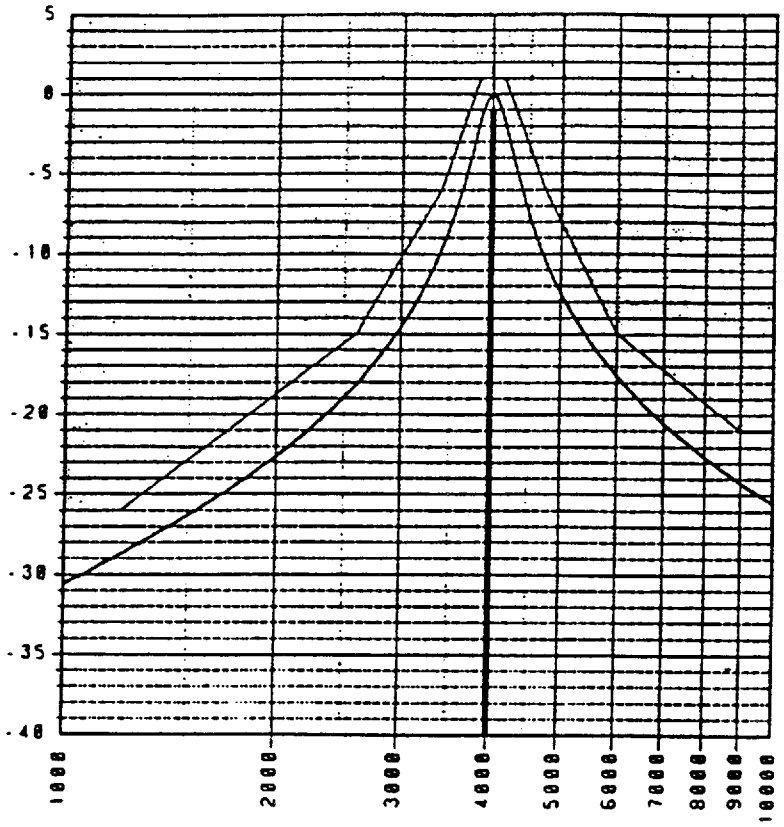




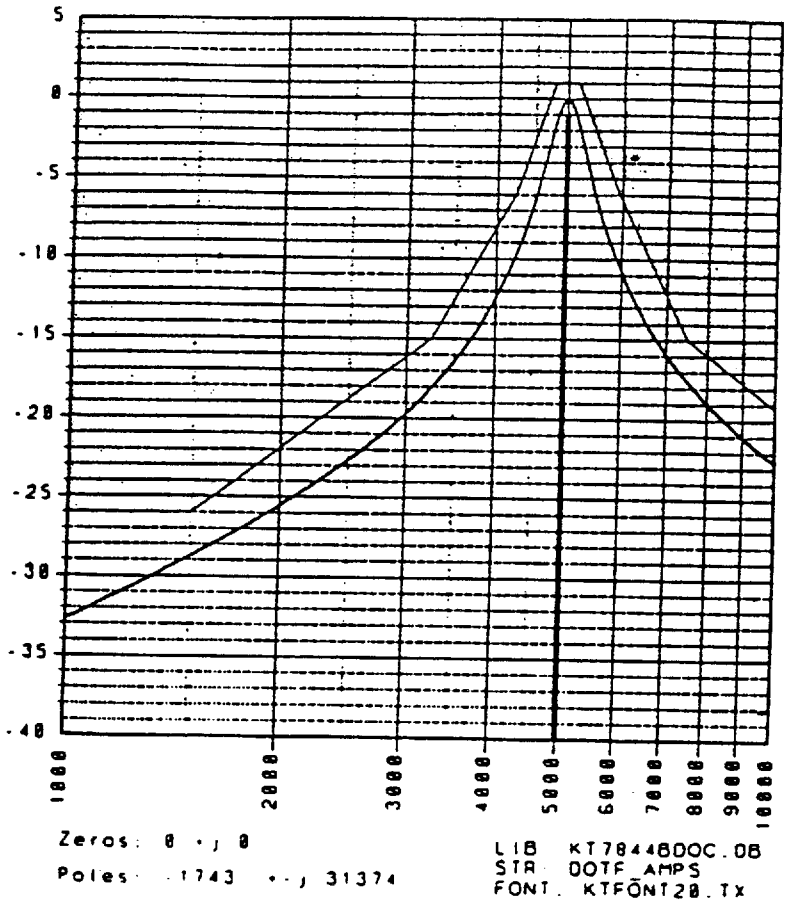
7.6.4 SAT-in filter characteristics



7.6.5 TACS DOTTING filter characteristics



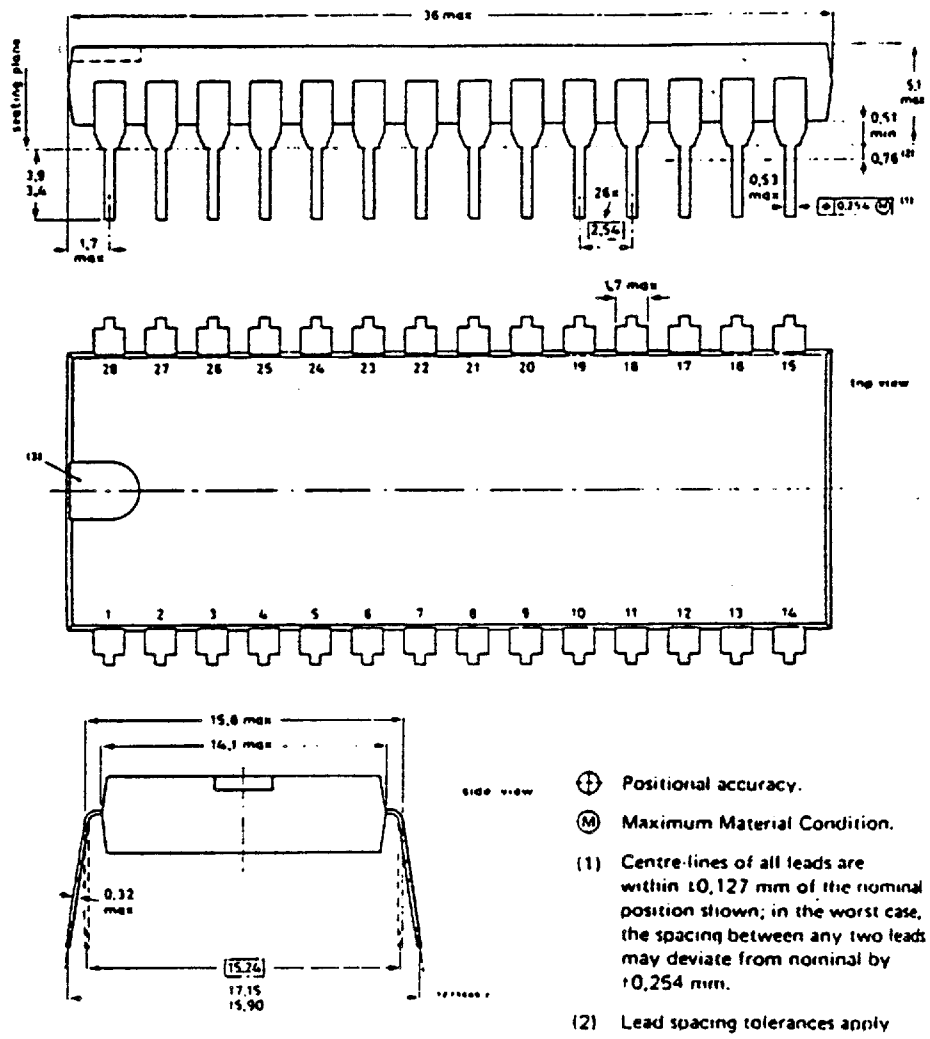
7.6.6 AMPS DOTTING filter characteristics



7. MECHANICAL DATA OF THE MODEM PACKAGE

7.1 28-pin DIL-package

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

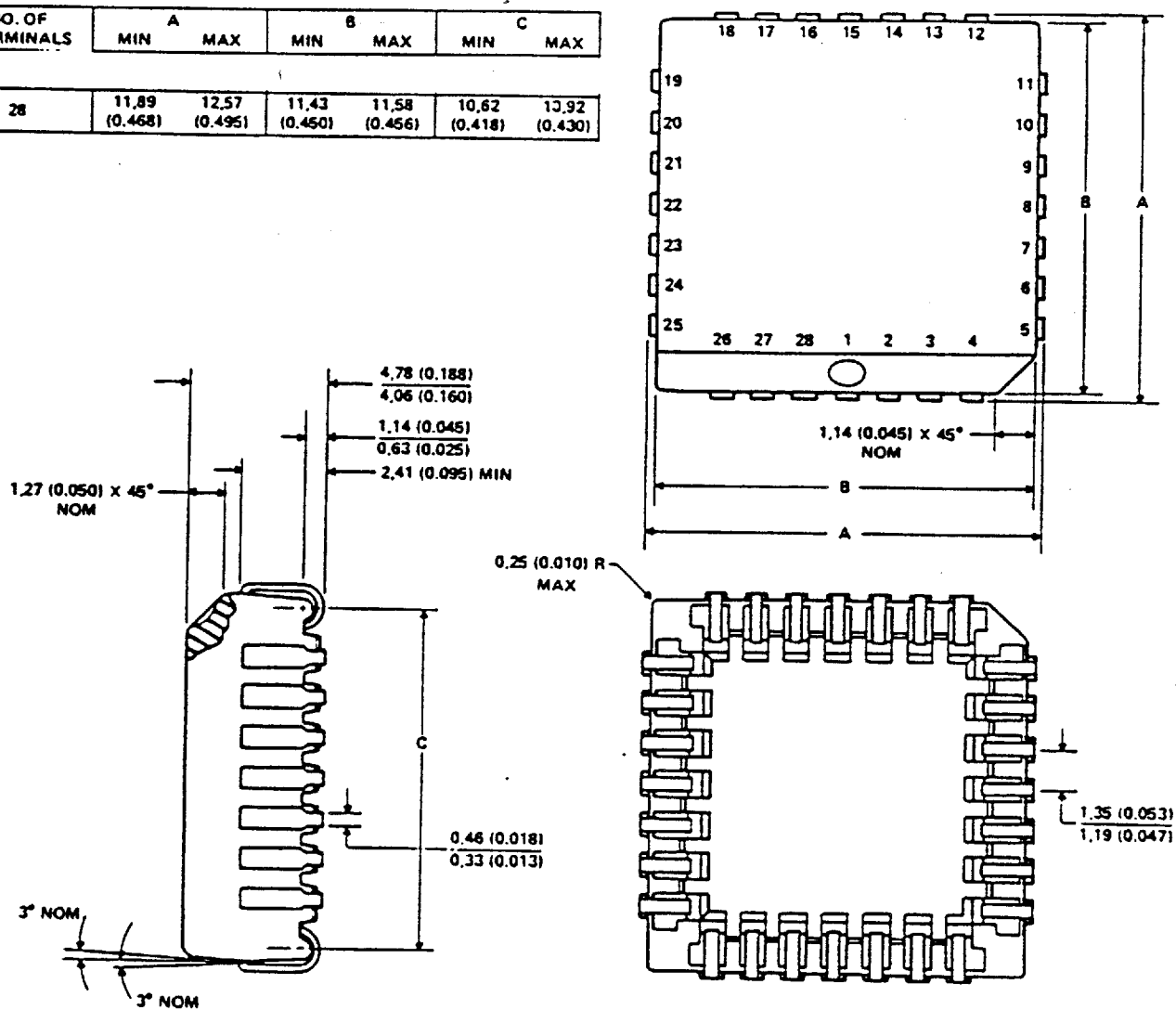
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

7.2 28-pin PLCC28-package (JEDEC), leg type J

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	11,89 (0.468)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

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8. TECHNICAL PERFORMANCE

The graph, figure 8.1., shows maximum bit error rate versus signal to noise ratio in TACS/AMPS modem.

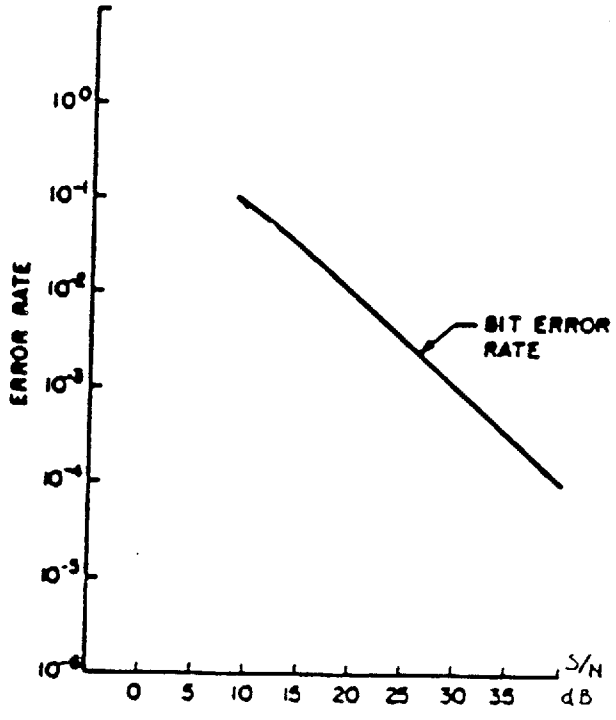

Figure 8.1. TACS/AMPS modems maximum bit error rate versus signal to noise ratio.