SiT5711 PRELIMINARY

1 to 60 MHz Emerald Platform™ Stratum 3E OCXO

Description

The SiT5711 is the industry's smallest Stratum 3E OCXO (9 mm x 7 mm) with ±5 ppb over-temp stability and ±0.04 ppb/°C typical frequency slope (dF/dT). Leveraging SiTime's unique DualMEMS™ and TurboCompensation™ temperature sensing technology, it delivers excellent stability in the presence of environmental stressors – airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The SiT5711's environmental robustness enables unmatched ease-of-use and reduces system manufacturing overhead:

- Highly flexible placement on the PCB
- No mechanical lid or shielding for thermal isolation
- No external regulators

SiT5711 can be factory-programmed to any frequency between 1 MHz and 60 MHz. The SiT5711 is supported by the SiT6731 evaluation board.

Features

- Any frequency between 1 MHz and 60 MHz, in 1 Hz steps
- ±0.04 ppb/°C frequency slope typical dF/dT
- ±5 ppb frequency stability over temperature
- Up to 85°C operating temperature range
- 1.5E-11 ADEV at 10 second averaging time
- Exceptional dynamic stability under airflow and rapid temperature changes
- Excellent Holdover over a wide range of conditions
- Integrated regulators for on-chip power-supply noise filtering and excellent PSNR
- GR-1244 Stratum 3E compliant
- Resistant to shock, vibration and board bending
- 3.3 V supply voltage
- LVCMOS and Clipped Sinewave outputs

Applications

- 4G/5G radio
- Base Stations
- Digital Switching
- Time and Frequency Measurement
- IEEE 1588
- Test and measurement

9 mm x 7 mm Package

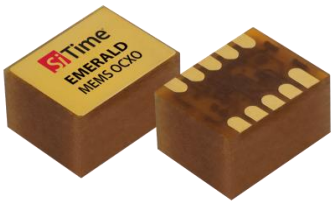


Figure 1. Top and bottom view

Package Pinout

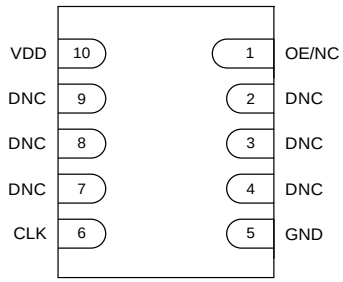
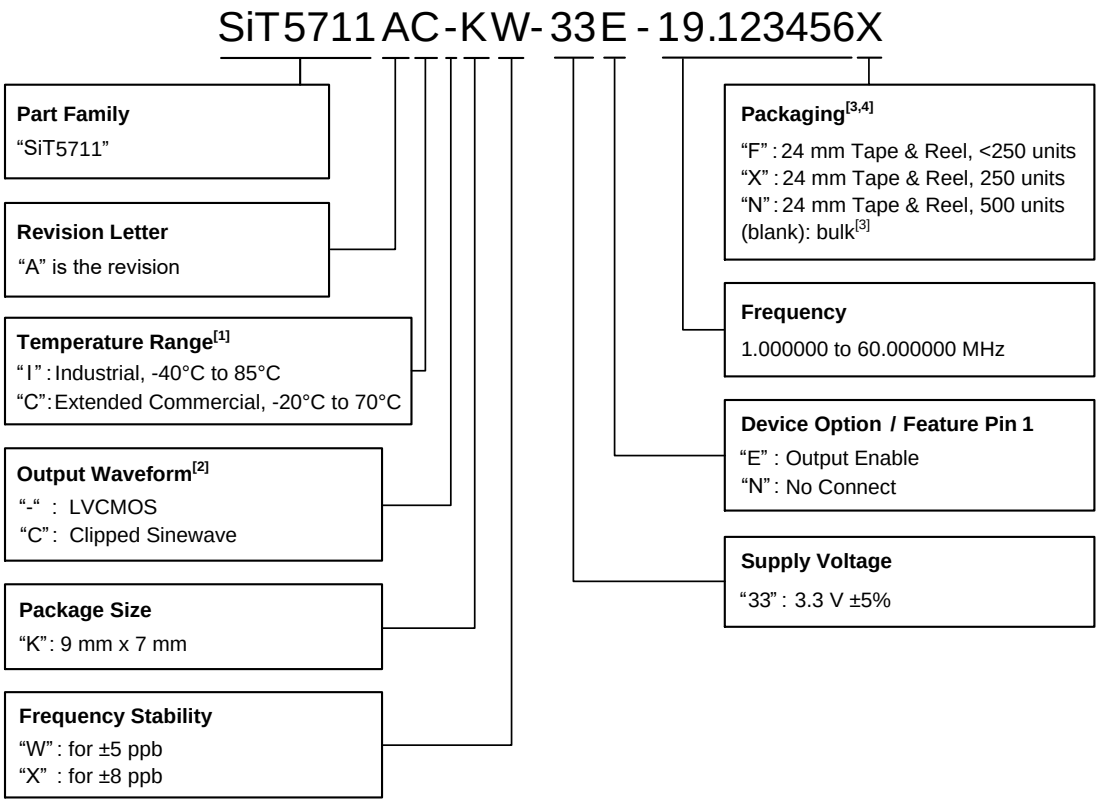


Figure 2. Pin Assignments (Bottom view)

Ordering Information



Notes:

1. Contact SiTime for other temperature range options.
2. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 2 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI.
3. Bulk is available for sampling only.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size	24 mm T&R (<250 units) [4]	24 mm T&R (250 units)	24 mm T&R (500 units)
9 mm x 7 mm	F	X	N

Notes:

4. Contact SiTime for minimum order quantities for <250 units.

Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage. Typical values are at 25°C and 3.3 V VDD. All measurements are specified with 15 pF load unless otherwise stated.

Table 2. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Output Frequency Range	F	1	–	60	MHz	
Frequency Stability						
Frequency Stability over Temperature	F_stab	-5	–	+5	ppb	Referenced to (fmax + fmin)/2 over the specified temperature range. Contact SiTime for ±3 ppb or tighter frequency stability.
		-8	–	+8	ppb	
Frequency vs. Temperature Slope	dF/dT	-0.12	±0.04	+0.12	ppb/°C	Steady airflow ≤4 m/s, 1°C/min ramp rate
Dynamic Frequency Change to Temperature Ramp	F_dynamic	-0.002	±0.0007	+0.002	ppb/s	Steady airflow ≤4 m/s, 1°C/min ramp rate
Initial Tolerance	F_init	-500	–	+500	ppb	Initial frequency offset at 48 hours after 2 reflows, measured at 25°C
Hysteresis Over Temperature	F_Hys	-0.8	±0.11	+0.8	ppb	Over -40 to 85°C, measured as maximum frequency deviation from center of hysteresis eye, 1°C/min ramp rate
One-day Aging	F_1d	–	±0.6	–	ppb	After 30-days operation, 50°C
One-month Aging	F_1m	–	±7	–	ppb	After 30-days operation, 50°C
One-year Aging	F_1y	–	±35	–	ppb	After 30-days operation, 50°C
Ten-year Aging	F_10y	–	±70	–	ppb	After 30-days operation, 50°C
Total Stability – 20 years	F_20y_stab	-1	–	+1	ppm	Better than Stratum 3E stability of ±4.6 ppm over 20 years per GR-1244-CORE. Inclusive of initial tolerance, frequency stability over temperature, 20-year Aging, and variations to supply voltage and output load. Typically called free running accuracy
Supply Voltage Sensitivity	F_vdd	–	±0.3	–	ppb	V_{DD} ±5%
Output Load Sensitivity	F_load	–	±0.2	–	ppb	LVCMOS output
		–	±0.2	–	ppb	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Start-up Characteristics						
Start-up Time	T_start	–	2.5	3.5	ms	Time to first pulse
OE Time	OE_Tstart	–		680	ns	Time to first pulse after OE pin reaches 70% of V_{DD}, 10 MHz
Warm-up Time	T_warmup	–	19.8	183	s	Time to within ±10 ppb of final frequency. Final frequency measured at one hour. 24 hours off prior to measurement.
		–	–	45	ms	Time to within ±200 ppb of final frequency. Final frequency measured at one hour. 24 hours off prior to measurement.
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	tr, tf	–	2.4	3	ns	10% - 90% VDD
Output Voltage High	V_{OH}	90%	–	–	V_{DD}	I_{OH} = ±3 mA, (V_{DD} = 3.3 V)
Output Voltage Low	V_{OL}	–	–	10%	V_{DD}	I_{OL} = ±3 mA, (V_{DD} = 3.3 V)
Clipped Sinewave Output Characteristics						
Output Voltage Level	V_{OUT}	0.8	–	1.2	V	Measured peak-to-peak swing at any V_{DD} – 10 kΩ || 10 pF ±10%
Rise/Fall Time	tr, tf	–	4.2	4.6	ns	20%–80% V_{OUT}

Table 3. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	V_{DD}	3.14	3.3	3.47	V	Contact SiTime for other voltage options
Power Consumption						
Power Consumption – Warm-up	Pwr_warmup	–	–	2.3	W	Max power may be configurable lower, higher max gives shorter time
Power Consumption – Steady State	Pwr_steady	–	0.95	1.1	W	At +25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial
		-40	–	+85	°C	Industrial. Contact SiTime for -55°C and 95°C support

Table 4. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	–	kΩ	Internal pull up to V_{DD}
Input High Voltage	VIH	70	–	–	%	
Input Low Voltage	VIL	–	–	30	%	

Table 5. Jitter & Phase Noise

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Period Jitter	T_jitt	–	1	–	ps	F = 10 MHz, population 10 k
RMS Phase Jitter (random)	T_phj	–	0.38	–	ps	F = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
Allan Deviation						
$\tau = 1\ second$	AD_1s	–	2E-11	–		
$\tau = 10\ seconds$	AD_10s	–	1.5E-11	–		
$\tau = 100\ seconds$	AD_100s	–	1.5E-11	–		
Phase Noise						
1 Hz offset		–	-80	-76	dBc/Hz	Reference f = 10.3 MHz
10 Hz offset		–	-109	-105	dBc/Hz	
100 Hz offset		–	-129	-126	dBc/Hz	
1 kHz offset		–	-148	-145	dBc/Hz	
10 kHz offset		–	-153	-151	dBc/Hz	
100 kHz offset		–	-153	-150	dBc/Hz	
1 MHz offset		–	-165	-161	dBc/Hz	
5 MHz offset		–	-166	-160	dBc/Hz	

Table 6. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	–	°C
V_{DD}	-0.5	4	V
Soldering Temperature (follow standard Pb-free soldering guidelines)	–	260	°C

Table 7. Environmental Compliance[5]

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method2002**
Mechanical Vibration	**MIL-STD-883F, Method2007, Condition A** **JEDEC JESD22-B103, Condition 1**
Temperature Cycle	**JESD22, MethodA104**
Solderability	**MIL-STD-883F, Method2003**
Moisture Sensitivity Level	**TBD**
Washability	**MSL3**

Note:
5. This device is RoHS and REACH compliant Pb-free and is Halogen-free and Antimony-free.

Pin-out Bottom View

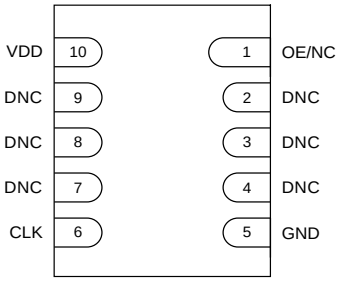


Figure 3. Size 9 mm x 7 mm

Table 8. Pin Assignments

Package Size	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
9 mm x 7 mm	OE/NC	DNC	DNC	DNC	GND	CLK	DNC	DNC	DNC	VDD

Table 9. Pin Description

Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
OE/NC	OE – Input	100 kΩ Pull-Up	H[6]: specified frequency output L: output is high impedance. Only output driver is disabled
	NC – No Connect	-	H or L or Open: No effect on output frequency or other device functions
DNC	Do Not Connect	DNC	Solder to pads, Do Not Connect
GND	Power	-	Connect to ground[7]
CLK	Output	-	LVCMOS, or clipped sinewave oscillator output
VDD	Power	-	Connect to VDD

Notes:

6. In OE mode, a pull-up resistor of 100 kΩ or less is recommended if Pin 1 is not externally driven. If Pin 1 needs to be left floating, use the NC option.
7. 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND.

Typical Performance Plots

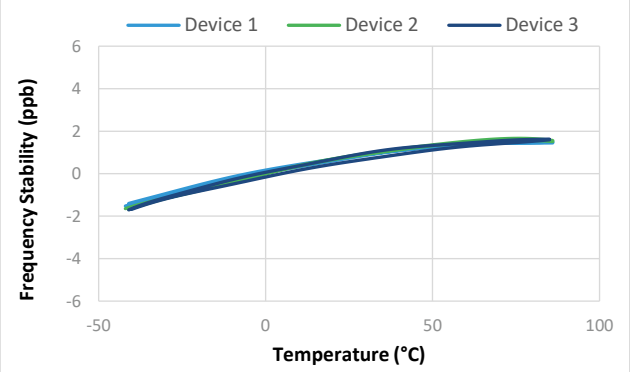


Figure 4. Frequency Stability

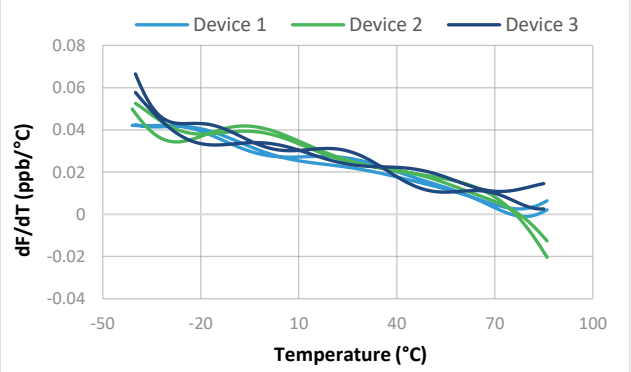


Figure 5. Frequency Slope

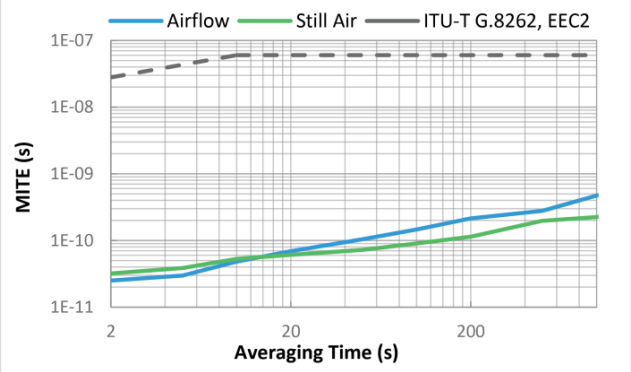


Figure 6. MTIE

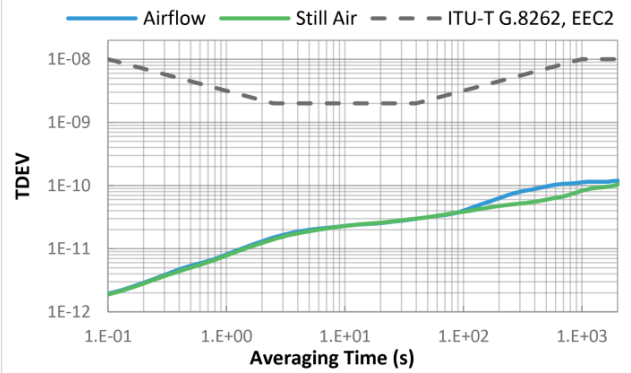
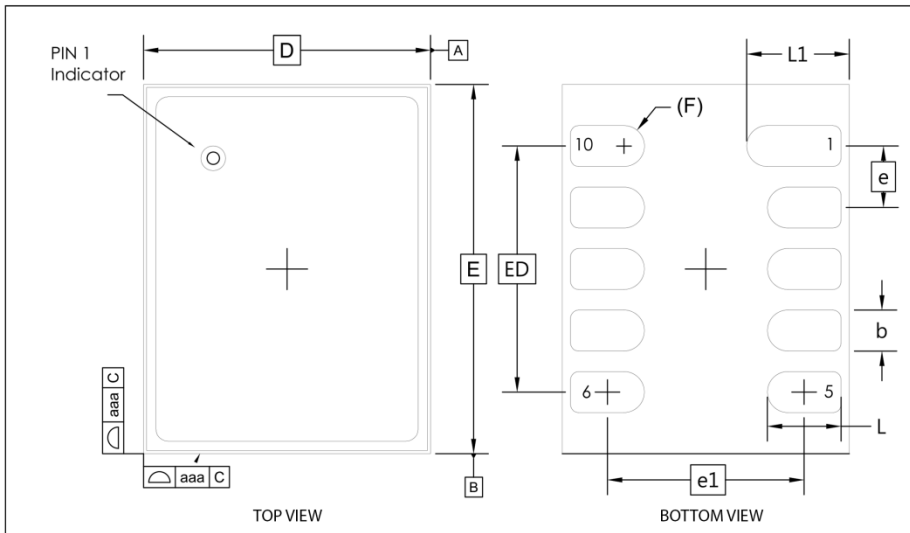


Figure 7. TDEV

Dimensions and Patterns — 9 mm x 7 mm package

Package Size – Dimensions (Unit: mm)



		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	5.010	5.600	6.190
BODY SIZE	X	D		7.000 BSC	
	Y	E		9.000 BSC	
LEAD WIDTH		b	0.950	1.000	1.050
LEAD LENGTH		L	1.750	1.800	1.850
LEAD PITCH		e		1.500 BSC	
		e1		4.800 BSC	
RADIUS		F		0.500 REF	
EDGE LEAD TO LEAD		ED		6.000 BSC	
PACKAGE TOLERANCE		aaa		0.15	
COPLANRITY		ccc		0.05	

Notes
1. All dimensions are in millimeters

Package Outline	
POD-051-PCBA-010-X0	10L PCBA
9.00x7.00x5.6 mm	
REV D00 2020/02/10	

Layout Guidelines

- SiT5711 uses internal regulators to minimize the impact of the power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1 µF and 10 µF). Place the bypass capacitors as close to the VDD pin as possible, typically within 1 to 2 mm. Ensure 0.1 uF cap is placed closest to the device VDD and GND power pins.
- No metal cover. Unlike legacy quartz OCXOs, SiT5711 is engineered to operate reliably without performance degradation, in the presence of ambient disturbers such as airflow and sudden temperature changes. Therefore, the use of a metal cover typical of quartz OCXOs is not needed.
- It is recommended to connect all NC pins to the ground plane and place multiple vias under the GND pin for maximum heat dissipation.
- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the SiT5711 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- After the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, it is recommended to use “no clean” flux. Do not subject SiT5711 to liquid based cleaning processes.
- Reflow profile, per JESD22-A113D
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes

Table 10. Additional Information

Document	Description
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.
SiT6731 EVB	Evaluation board, contact SiTime
Time Machine II	MEMS oscillator programmer
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info
Qualification Reports	RoHS report, Reliability reports, Composition reports
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies
Termination Techniques	Termination design recommendations
Layout Techniques	Layout recommendations
Other Quality Documents	ISO certificate, materials declarations, environmental policy, warranty on date code

Table 11. Revision History

Version	Release Date	Change Summary
0.1	07/17/2018	First release, advanced information
0.11	07/27/2018	Changed Pin 2 and Pin 7 to Rsvd (reserved)
0.12	08/08/2018	Added 9x7 mm package option in the ordering code Added 9x7 mm package pad layout recommendation Misc. corrections
0.13	08/09/2018	Removed 10 mm x 10 mm package Misc. formatting changes
0.14	08/27/2018	Added ±3 ppb support Added 14.0 x 9.0 mm, 20.0 x 13.0 mm, 25.0 x 22.0 mm packages Updated Table 2 and Ordering information Added Package Drawing section
0.8	11/01/2018	Update frequency slope to ±0.15 ppb°/C Misc. corrections
0.81	02/15/2019	Updated Ordering information Added Typical Performance Plots section Rearranged sections Added Pin Outs for 14x9 mm, 20x13 mm and 25x22 mm Updated Layout Guidelines Added T&R options Added factory option note to the Typical Plots Labeled package Top Views Other minor corrections
0.82	03/15/2019	Updated drawings for 14x9, 20x13 and 25x22 mm packages
0.83	10/10/2019	Updated Phase Noise *(typical)* in Table 5 Updated Packages Pinout, added Washability and additional information
0.84	12/03/2019	Changed Rise/Fall time condition for Clipped Sinewave Output Characteristics
0.85	03/02/2020	Package Drawings edits
0.91	04/20/2020	Updated various specifications and conditions after characterization Updated package drawings and pinouts view
0.92	06/05/2020	Updated Typical Performance Plots Cycle to Cycle Jitter Removed Hysteresis Specification Updated Manufacturing Notes Updated

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