ISO²-CMOS MT9196 C-Phone

Advance Information

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Features

- Programmable μ-Law/A-Law CODEC and Filters
- Programmable CCITT (G.711)/sign-magnitude coding
- Programmable transmit, receive and side-tone gains
- Digital DTMF and single tone generation
- Fully differential interface to handset transducers
- Auxiliary analog interface
- Flexible digital interface including ST-BUS
- Serial microport control
- Single 5 volt supply, low power operation
- Anti-howl circuit for group listening applications

Applications

- Digital telephone sets
- Cellular radio sets
- Local area communications stations

Ordering Information

MT9196AE	28 Pin Plastic DIP
MT9196AC	28 Pin Ceramic DIP
MT9196AP	28 Pin Plastic LCC

-40°C to +85°C

Description

The MT9196 C-Phone is an integrated circuit designed for use in digital phone products. The device incorporates a built-in Filter/Codec, digital gain pads, DTMF generator and tone ringer. Complete telephony interfaces are provided for connecting to handset and speakerphone transducers. Internal register access is provided through a serial microport compatible with various industry standard micro-controllers.

The device is fabricated in Mitel's ISO²-CMOS technology ensuring low power consumption and high reliability.

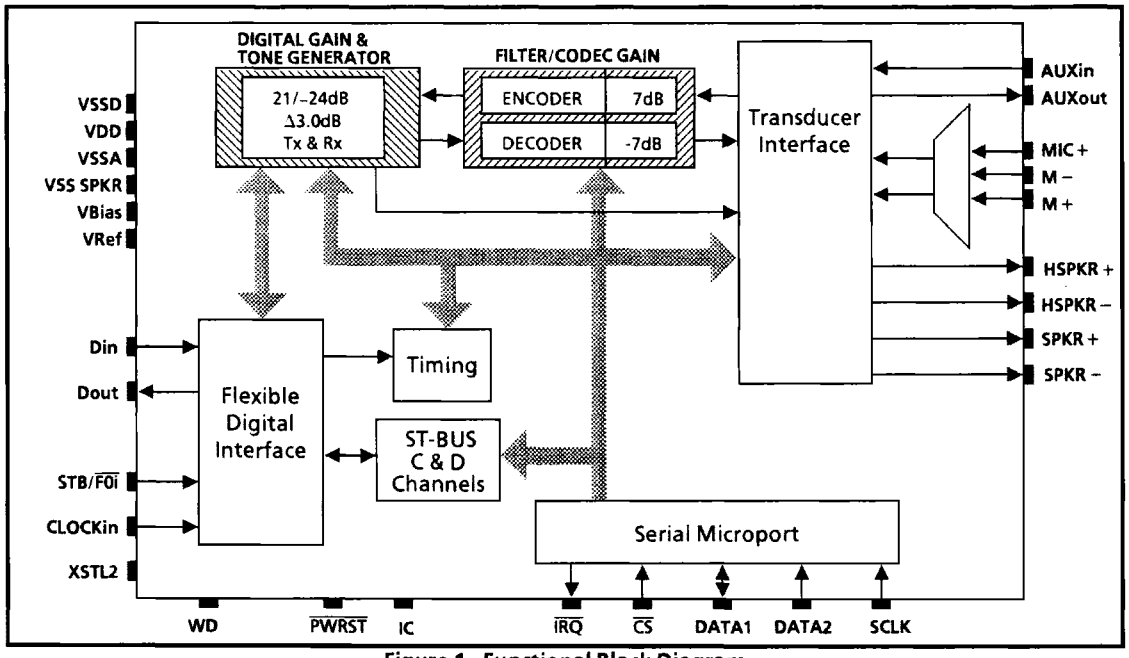

Figure 1 - Functional Block Diagram

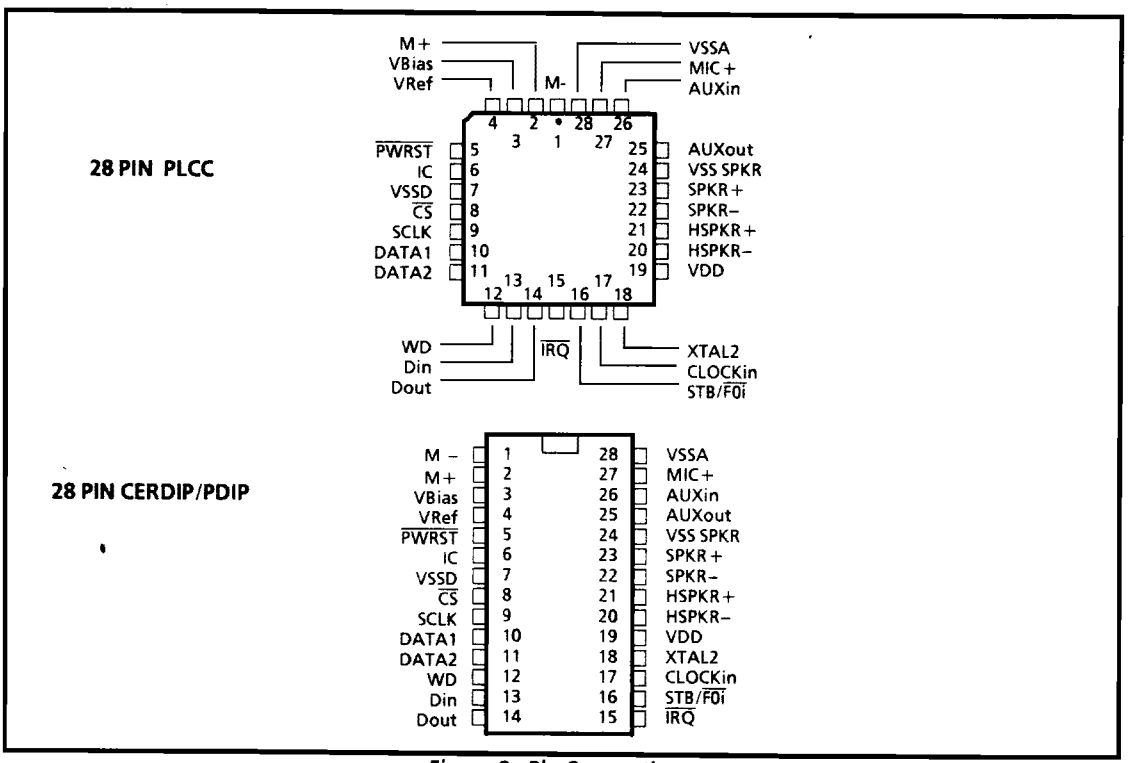

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	M–	**Inverting Microphone (Input).** Inverting input to microphone amplifier from the handset microphone.
2	M+	**Non-Inverting Microphone (Input).** Non-inverting input to microphone amplifier from the handset microphone.
3	V_{Bias}	**Bias Voltage (Output).** ($V_{DD}/2$) volts is available at this pin for biasing external amplifiers. Connect 0.1 µF capacitor to V_{SSA}.
4	V_{Ref}	**Reference voltage for codec (Output).** Nominally [($V_{DD}/2$)–1.5] volts. Used internally. Connect 0.1 µF capacitor to V_{SSA}.
5	$\overline{PWRST}$	**Power-up Reset (Input).** CMOS compatible input with Schmitt Trigger (active low).
6	IC	**Internal Connection.** Tie externally to V_{SS} for normal operation.
7	V_{SSD}	**Digital Ground .** Nominally 0 volts.
8	$\overline{CS}$	**Chip Select (Input).** This input signal is used to select the device for microport data transfers. Active low. TTL level compatible.
9	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for microport. TTL level compatible.
10	DATA 1	**Bidirectional Serial Data.** Port for microprocessor serial data transfer. In Motorola/National mode of operation , this pin becomes the data transmit pin only and data receive is performed on the DATA 2 pin. TTL level compatible input levels.
11	DATA 2	**Serial Data Receive.** In certain modes of operation, this pin is used for data receive to the C-Phone. In Intel mode, serial data transmit and receive are performed on the DATA 1 pin and DATA 2 is disconnected. Input level TTL compatible.
12	WD	**Watchdog (Output).** Watchdog timer output. Active high.

Pin Description

Pin #	Name	Description
13	D_{in}	**Data Input.** A digital input for 8 bit wide channel data received from the Layer 1 device. Data is sampled on the falling edge of BCL during the timeslot defined by STB, or according to standard ST-BUS timing. Input level is CMOS compatible.
14	D_{out}	**Data Output.** A selectable tri-state/open drain digital output for 8 bit wide channel data being sent to the Layer 1 device. Data is shifted out via this pin concurrent with the rising edge of BCL during the timeslot defined by STB, or according to standard ST-BUS timing.
15	$\overline{IRQ}$	**Interrupt Request (Open Drain Output).** Low true interrupt output to microcontroller.
16	STB/$\overline{F0i}$	**Data Strobe/Frame Pulse (Input).** For SSI mode this input determines the 8 bit timeslot used by the device for both transmit and receive data. This active high signal has a repetition rate of 8 kHz. Standard frame pulse definitions apply in ST-BUS mode. CMOS level compatible input.
17	CLOCKin	**Clock (Input).** The clock provided to this input is used by the internal phone functions.
18	XSTL2	**Crystal Input (4.096 MHz).** Used in conjunction with the MCL/$\overline{C4i}$/XSTL1 pin to provide the master clock signal via external crystal.
19	V_{DD}	**Positive Power Supply (Input).** Nominally 5 volts.
20	HSPKR –	**Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
21	HSPKR+	**Non-Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
22	SPKR –	**Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
23	SPKR +	**Non-Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
24	V_{SS}SPKR	**Power Supply Rail for Speaker Driver.** Nominally 0 Volts.
25	AUX_{out}	**Auxilary Port (Output).** Access point to the D/A (analog) signals of the receive path as well as to the various analog inputs.
26	AUX_{in}	**Auxiliary Port (Input).** An analog signal may be fed to the filter/codec transmit section and various loopback paths via this pin. No external anti-aliasing is required.
27	MIC +	**Non-inverting on-hook answer back Microphone (Input).** Microphone amplifier non-inverting input pin.
28	V_{SSA}	**Analog Ground (Input).** Nominally 0 V.

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