

## MEMORY

## CMOS

## 4 M × 4 BIT

## FAST PAGE MODE DYNAMIC RAM

## MB81V17400A-60/-70/-60L/-70L

## CMOS 4,194,304 × 4 Bit Fast Page Mode Dynamic RAM

## ■ DESCRIPTION

The Fujitsu MB81V17400A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 4-bit increments. The MB81V17400A features a "fast page" mode of operation whereby high-speed random access of up to 1,024 bits of data within the same row can be selected. The MB81V17400A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V17400A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V17400A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V17400A are not critical and all inputs are LVTTTL compatible.

## ■ PRODUCT LINE &amp; FEATURES

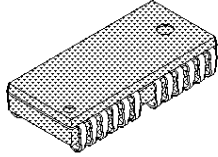
Parameter		MB81V17400A				
		-60	-60L	-70	-70L	
RAS Access Time		60 ns max.	60 ns max.	70 ns max.	70 ns max.	
Random Cycle Time		110 ns min.	110 ns min.	130 ns min.	130 ns min.	
Address Access Time		30 ns max.	30 ns max.	35 ns max.	35 ns max.	
CAS Access Time		15 ns max.	15 ns max.	17 ns max.	17 ns max.	
Fast Page Mode Cycle Time		40 ns min.	40 ns min.	45 ns min.	45 ns min.	
Low Power Dissipation	Operating Current	396 mW max.	396 mW max.	342 mW max.	342 mW max.	
	Standby Current	LVTTTL level	7.2 mW max.	3.6 mW max.	7.2 mW max.	3.6 mW max.
		CMOS level	3.6 mW max.	0.54 mW max.	3.6 mW max.	0.54 mW max.

- 4,194,304 words × 4 bit organization
- Silicon gate, CMOS, Advanced Capacitor Cell
- All input and output are LVTTTL compatible
- 2048 refresh cycles every 32.8 ms
- Self refresh function
- Standard and low power versions
- Early Write or  $\overline{OE}$  controlled write capability
- RAS only, CAS-before-RAS, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

# MB81V17400A-60/-70/-60L/-70L

## ■ PACKAGE

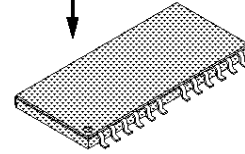
Plastic SOJ Package



(LCC-26P-M09)

Plastic TSOP(II) Package

Marking side



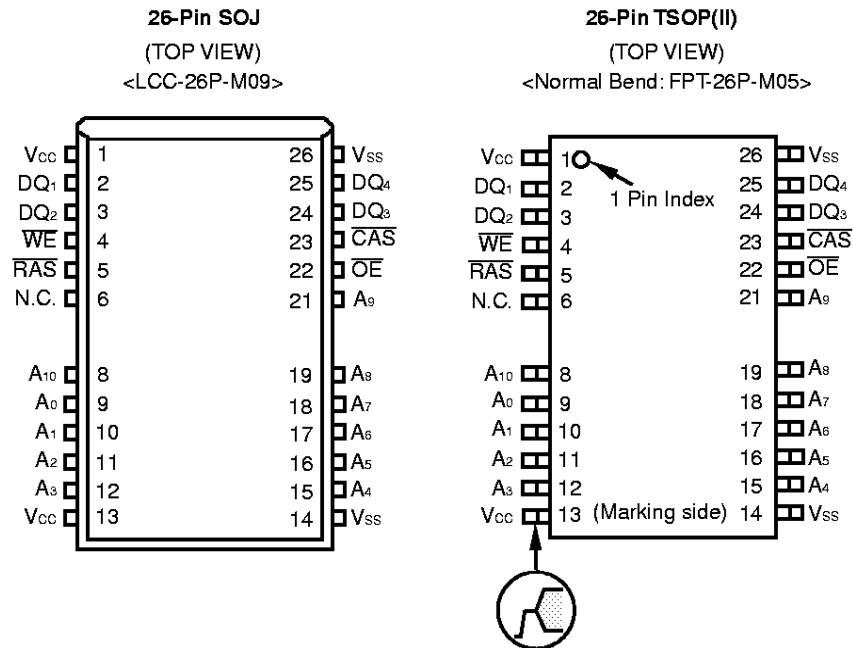
(FPT-26P-M05)  
(Normal Bend)

### Package and Ordering Information

- 26-pin plastic (300mil) SOJ, order as MB81V17400A-xxPJ
- 26-pin plastic (300mil) TSOP-II with normal bend leads, order as MB81V17400A-xxPFTN and MB81V17400A-xxLPFTN (Low Power)

# MB81V17400A-60/-70-60L/-70L

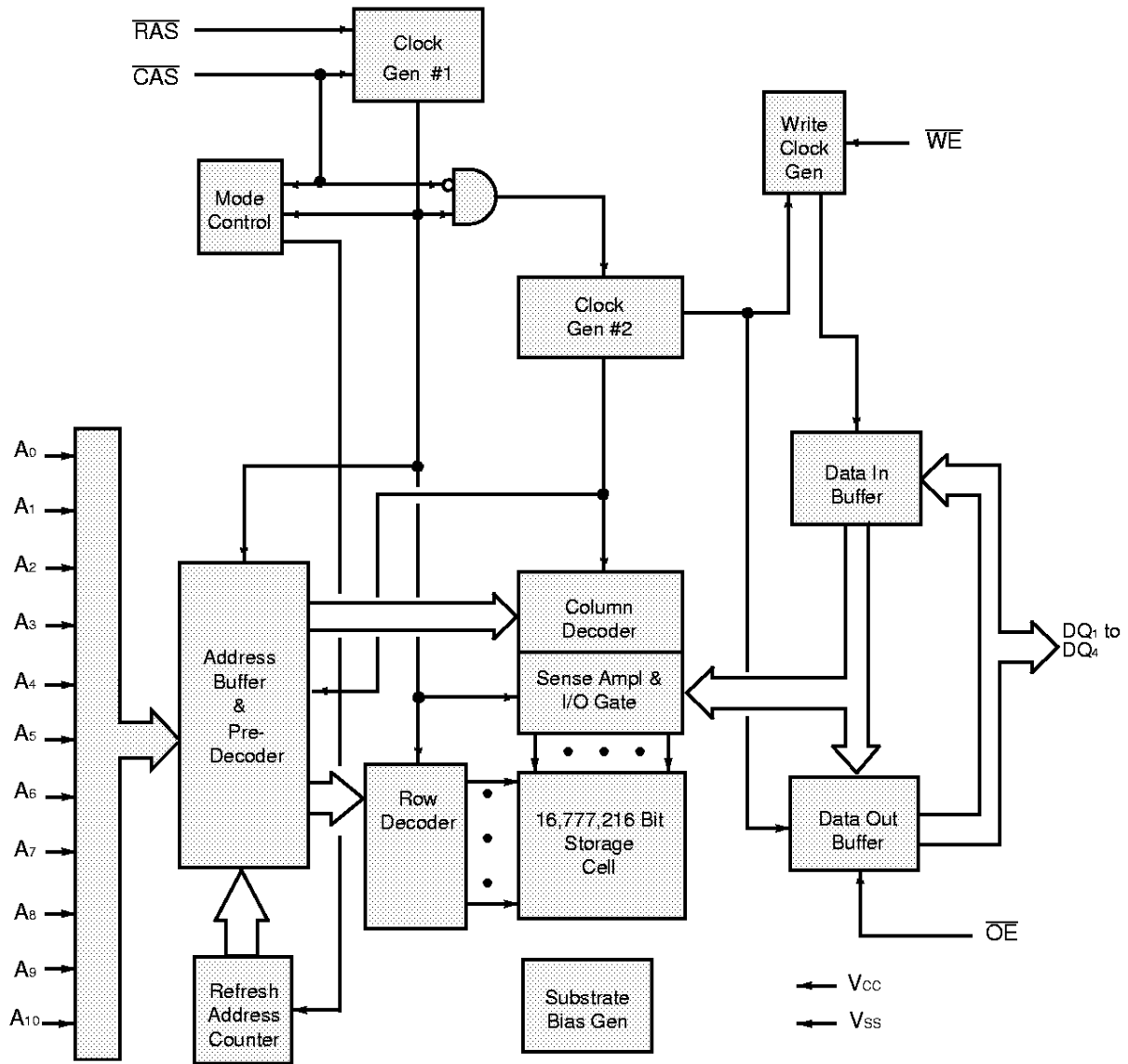
## ■ PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
DQ <sub>1</sub> to DQ <sub>4</sub>	Data input/output
$\overline{WE}$	Write enable
$\overline{RAS}$	Row address strobe
A <sub>0</sub> to A <sub>10</sub>	Address inputs
V <sub>CC</sub>	+3.3 volt power supply
$\overline{OE}$	Output enable
$\overline{CAS}$	Column address strobe
V <sub>SS</sub>	Circuit ground
N.C.	No connection

# MB81V17400A-60/-70/-60L/-70L

Fig. 1 - MB81V17400A DYNAMIC RAM - BLOCK DIAGRAM



# MB81V17400A-60/-70-60L/-70L

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to +4.6	V
Voltage of V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to +4.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Short Circuit Output Current	I <sub>OUT</sub>	-50 to +50	mA
Operating Temperature	T <sub>OP</sub>	0 to +70	°C
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	*1	V <sub>CC</sub>	3.0	3.3	3.6	V	0°C to +70°C
		V <sub>SS</sub>	0	0	0		
Input High Voltage, All Inputs	*1	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.3	V	
Input Low Voltage, All Inputs/ outputs *	*1	V <sub>IL</sub>	-0.3	—	0.8	V	

\* : Undershoots of up to -1.2 volts with a pulse width not exceeding 20 ns are acceptable.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

(T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A <sub>0</sub> to A <sub>10</sub>	C <sub>IN1</sub>	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	C <sub>IN2</sub>	—	5	pF
Input/Output Capacitance, DQ <sub>1</sub> to DQ <sub>4</sub>	C <sub>DQ</sub>	—	7	pF

# MB81V17400A-60/-70/-60L/-70L

## FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address Input		Input Data		Refresh	Note
	RAS	CAS	WE	OE	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}(\text{min})$
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes *	$t_{WCS} \geq t_{WCS}(\text{min})$
Read-Modify- Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
RAS-only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
CAS-before- RAS Refresh Cycle	L	L	H	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}(\text{min})$
Hidden Refresh Cycle	H→L	L	H→X	L	—	—	—	Valid	Yes	Previous data is kept.

X: "H" or "L"

\*: It is impossible in Fast Page Mode

## FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty-two input bits are required to decode any four of 16,777,216 cell addresses in the memory matrix. Since only eleven address bits ( $A_0$  to  $A_{10}$ ) are available, the row and column inputs are separately strobed by RAS and CAS as shown in Figure 1. First, eleven row address bits are input on pins  $A_0$ -through- $A_{10}$  and latched with the row address strobe (RAS) then, ten column address bits are input and latched with the column address strobe (CAS). Both row and column addresses must be stable on or before the falling edge of RAS and CAS, respectively. The address latches are of the flow-through type; thus, address information appearing after  $t_{RAH}(\text{min.}) + t_r$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of WE. When WE is active Low, a write cycle is initiated; when WE is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUTS

Input data is written into memory in either of three basic ways: an early write cycle, an OE (delayed) write cycle, and a read-modify-write cycle. The falling edge of WE or CAS, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data ( $DQ_1$  to  $DQ_4$ ) is strobed by CAS and the setup/hold times are referenced to CAS because WE goes Low before CAS. In a delayed write or a read-modify-write cycle, WE goes Low after CAS; thus, input data is strobed by WE and all setup/hold times are referenced to the write-enable signal.

# MB81V17400A-60/-70-60L/-70L

## DATA OUTPUTS

The three-state buffers are LVTTTL compatible with a fanout of one TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- $t_{RAC}$  : from the falling edge of  $\overline{RAS}$  when  $t_{RCD}$  (max) is satisfied.
- $t_{CAC}$  : from the falling edge of  $\overline{CAS}$  when  $t_{RCD}$  is greater than  $t_{RCD}$  (max).
- $t_{AA}$  : from column address input when  $t_{RAD}$  is greater than  $t_{RAD}$  (max).
- $t_{OEA}$  : from the falling edge of  $\overline{OE}$  when  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$ .

The data remains valid after either  $\overline{CAS}$  or  $\overline{OE}$  returns to High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

## FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions,  $\overline{RAS}$  is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024 bits can be accessed and, when multiple MB81V17400As are used,  $\overline{CAS}$  is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

# MB81V17400A-60/-70/-60L/-70L

## ■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note 3

Parameter	Notes	Symbol	Condition	Value				Unit
				Min.	Typ.	Max.		
						Std power	Low power	
Output High Voltage		$V_{OH}$	$I_{OH} = -2.0 \text{ mA}$	2.4	—	—	—	V
Output Low Voltage		$V_{OL}$	$I_{OL} = +2.0 \text{ mA}$	—	—	0.4	0.4	
Input Leakage Current (Any Input)		$I_{(L)}$	$0 \text{ V} \leq V_{IN} \leq V_{CC}$ ; $3.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ ; $V_{SS} = 0 \text{ V}$ ; All other pins under test = 0 V	-10	—	10	10	$\mu\text{A}$
Output Leakage Current		$I_{O(L)}$	$0 \text{ V} \leq V_{OUT} \leq V_{CC}$ ; Data out disabled	-10	—	10	10	
Operating Current (Average Power Supply Current)	MB81V17400A -60/-60L	$I_{CC1}$	$\overline{RAS}$ & $\overline{CAS}$ cycling; $t_{RC} = \text{min}$	—	—	110	110	mA
	MB81V17400A -70/-70L					95	95	
Standby Current (Power Supply Current)	LVTTL Level	$I_{CC2}$	$\overline{RAS} = \overline{CAS} = V_{IH}$	—	—	2.0	1.0	mA
	CMOS Level		$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$			1000	150	
Refresh Current#1 (Average Power Supply Current)	MB81V17400A -60/-60L	$I_{CC3}$	$\overline{CAS} = V_{IH}$ , $\overline{RAS}$ cycling; $t_{RC} = \text{min}$	—	—	110	110	mA
	MB81V17400A -70/-70L					95	95	
Fast Page Mode Current	MB81V17400A -60/-60L	$I_{CC4}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling; $t_{HPC} = \text{min}$	—	—	70	70	mA
	MB81V17400A -70/-70L					60	60	
Refresh Current#2 (Average Power Supply Current)	MB81V17400A -60/-60L	$I_{CC5}$	$\overline{RAS}$ cycling; $\overline{CAS}$ -before- $\overline{RAS}$ ; $t_{RC} = \text{min}$	—	—	110	110	mA
	MB81V17400A -70/-70L					95	95	
Battery backup Current (Average Power Supply Current)	MB81V17400A -60L/-70L	$I_{CC6}$	$\overline{RAS}$ cycling; $\overline{CAS}$ -before- $\overline{RAS}$ ; $t_{RC} = 64 \mu\text{s}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$	—	—	—	300	$\mu\text{A}$
Refresh Current#3 (Average Power Supply Current)	MB81V17400A -60L/-70L	$I_{CC9}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS} = V_{IL}$ Self Refresh;	—	—	—	250	$\mu\text{A}$

# MB81V17400A-60/-70-60L/-70L

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V17400A -60/-60L		MB81V17400A -70/-70L		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh	Std power	t <sub>REF</sub>	—	32.8	—	32.8	ms
		Low power		—	128	—	128	ms
2	Random Read/Write Cycle Time		t <sub>RC</sub>	110	—	130	—	ns
3	Read-Modify-Write Cycle Time		t <sub>RWC</sub>	150	—	174	—	ns
4	Access Time from $\overline{\text{RAS}}$	*6,9	t <sub>RAC</sub>	—	60	—	70	ns
5	Access Time from $\overline{\text{CAS}}$	*7,9	t <sub>CAC</sub>	—	15	—	17	ns
6	Column Address Access Time	*8,9	t <sub>AA</sub>	—	30	—	35	ns
7	Output Hold Time		t <sub>OH</sub>	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t <sub>ON</sub>	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	*10	t <sub>OFF</sub>	—	15	—	17	ns
10	Transition Time		t <sub>T</sub>	3	50	3	50	ns
11	$\overline{\text{RAS}}$ Precharge Time		t <sub>RP</sub>	40	—	50	—	ns
12	$\overline{\text{RAS}}$ Pulse Width		t <sub>RAS</sub>	60	100000	70	100000	ns
13	$\overline{\text{RAS}}$ Hold Time		t <sub>RSH</sub>	15	—	17	—	ns
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t <sub>CRP</sub>	0	—	0	—	ns
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	*11,12	t <sub>RCD</sub>	20	45	20	53	ns
16	$\overline{\text{CAS}}$ Pulse Width		t <sub>CAS</sub>	15	—	17	—	ns
17	$\overline{\text{CAS}}$ Hold Time		t <sub>CSH</sub>	60	—	70	—	ns
18	$\overline{\text{CAS}}$ Precharge Time (Normal)	*19	t <sub>CPN</sub>	10	—	10	—	ns
19	Row Address Setup Time		t <sub>ASR</sub>	0	—	0	—	ns
20	Row Address Hold Time		t <sub>RAH</sub>	10	—	10	—	ns
21	Column Address Setup Time		t <sub>ASC</sub>	0	—	0	—	ns
22	Column Address Hold Time		t <sub>CAH</sub>	15	—	15	—	ns
23	Column Address Hold Time from $\overline{\text{RAS}}$		t <sub>AR</sub>	35	—	35	—	ns
24	$\overline{\text{RAS}}$ to Column Address Delay Time	*13	t <sub>RAD</sub>	15	30	15	35	ns
25	Column Address to $\overline{\text{RAS}}$ Lead Time		t <sub>RAL</sub>	30	—	35	—	ns
26	Column Address to $\overline{\text{CAS}}$ Lead Time		t <sub>CAL</sub>	30	—	35	—	ns
27	Read Command Setup Time		t <sub>RCS</sub>	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	*14	t <sub>RRH</sub>	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	*14	t <sub>RCH</sub>	0	—	0	—	ns
30	Write Command Setup Time	*15,20	t <sub>WCS</sub>	0	—	0	—	ns

(Continued)

# MB81V17400A-60/-70/-60L/-70L

(Continued)

No.	Parameter	Notes	Symbol	MB81V17400A -60/-60L		MB81V17400A -70/-70L		Unit
				Min.	Max.	Min.	Max.	
31	Write Command Hold Time		t <sub>WCH</sub>	15	—	15	—	ns
32	Write Hold Time from $\overline{\text{RAS}}$		t <sub>WCR</sub>	35	—	35	—	ns
33	$\overline{\text{WE}}$ Pulse Width		t <sub>WP</sub>	15	—	15	—	ns
34	Write Command to $\overline{\text{RAS}}$ Lead Time		t <sub>RWL</sub>	15	—	17	—	ns
35	Write Command to $\overline{\text{CAS}}$ Lead Time		t <sub>CWL</sub>	15	—	17	—	ns
36	DIN Setup Time		t <sub>DS</sub>	0	—	0	—	ns
37	DIN Hold Time		t <sub>DH</sub>	15	—	15	—	ns
38	Data Hold Time from $\overline{\text{RAS}}$		t <sub>DHR</sub>	35	—	35	—	ns
39	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	*20	t <sub>RWD</sub>	80	—	92	—	ns
40	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	*20	t <sub>CWD</sub>	35	—	39	—	ns
41	Column Address to $\overline{\text{WE}}$ Delay Time	*20	t <sub>AWD</sub>	50	—	57	—	ns
42	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh cycles)		t <sub>RPC</sub>	5	—	5	—	ns
43	$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t <sub>CSR</sub>	0	—	0	—	ns
44	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t <sub>CHR</sub>	10	—	12	—	ns
45	$\overline{\text{WE}}$ Setup Time from $\overline{\text{RAS}}$		t <sub>WSR</sub>	0	—	0	—	ns
46	$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$		t <sub>WHR</sub>	10	—	10	—	ns
47	Access Time from $\overline{\text{OE}}$	*9	t <sub>OEA</sub>	—	15	—	17	ns
48	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	*10	t <sub>OEZ</sub>	—	15	—	17	ns
49	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data		t <sub>OEL</sub>	5	—	7	—	ns
50	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	*16	t <sub>OEH</sub>	5	—	5	—	ns
51	$\overline{\text{OE}}$ to Data in Delay Time		t <sub>OED</sub>	15	—	17	—	ns
52	$\overline{\text{CAS}}$ to Data in Delay Time		t <sub>CDD</sub>	—	—	—	—	ns
53	DIN to $\overline{\text{CAS}}$ Delay Time	*17	t <sub>DZC</sub>	0	—	0	—	ns
54	DIN to $\overline{\text{OE}}$ Delay Time	*17	t <sub>DZO</sub>	0	—	0	—	ns
55	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width		t <sub>RASP</sub>	—	100000	—	100000	ns
56	Fast Page Mode Read/Write Cycle Time		t <sub>PC</sub>	40	—	45	—	ns
57	Fast Page Mode Read-Modify-Write Cycle Time		t <sub>PRWC</sub>	80	—	89	—	ns
58	Access Time from $\overline{\text{CAS}}$ Precharge	*9,18	t <sub>CPA</sub>	—	35	—	40	ns

(Continued)

# MB81V17400A-60/-70-60L/-70L

(Continued)

No.	Parameter	Notes	Symbol	MB81V17400A -60/-60L		MB81V17400A -70/-70L		Unit
				Min.	Max.	Min.	Max.	
59	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time		$t_{CP}$	10	—	10	—	ns
60	Fast Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		$t_{RHCP}$	35	—	40	—	ns
61	Fast Page Mode $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	*20	$t_{CPWD}$	55	—	62	—	ns

# MB81V17400A-60/-70/-60L/-70L

- Notes:**
- \*1. Referenced to  $V_{SS}$ .
  - \*2.  $I_{CC}$  depends on the output load conditions and cycle rates; the specified values are obtained with the output open.  $I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$ ,  $\overline{CAS} = V_{IH}$  and  $V_{IL} > -0.3V$ .  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  $I_{CC2}$  is specified during  $\overline{RAS} = V_{IH}$  and  $V_{IL} > -0.3V$ .  $I_{CC6}$  is measured on condition that all address signals are fixed steady state.
  - \*3. An initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200  $\mu s$  is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
  - \*4. AC characteristics assume  $t_r = 5$  ns.
  - \*5. Input voltage levels are 0V and 3V, and input reference levels are  $V_{IH}$  (min) and  $V_{IL}$  (max) for measuring timings of input signals. Also, the transition time ( $t_r$ ) is measured between  $V_{IH}$  (min) and  $V_{IL}$  (max). The output reference levels are  $V_{OH} = 2.0V$  and  $V_{OL} = 0.8V$ .
  - \*6. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$ ,  $t_{RAD} \leq t_{RAD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig. 2 and 3.
  - \*7. If  $t_{RCD} \geq t_{RCD}(\max)$ ,  $t_{RAD} \geq t_{RAD}(\max)$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_r$ , access time is  $t_{CAC}$ .
  - \*8. If  $t_{RAD} \geq t_{RAD}(\max)$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_r$ , access time is  $t_{AA}$ .
  - \*9. Measured with a load equivalent to one TTL loads and 100 pF.
  - \*10.  $t_{OFF}$  and  $t_{OEZ}$  is specified that output buffer change to high-impedance state.
  - \*11. Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*12.  $t_{RCD}(\min) = t_{RAH}(\min) + 2t_r + t_{ASC}(\min)$ .
  - \*13. Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
  - \*15.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS}(\min)$  the data output pin will remain High-Z state through entire cycle.
  - \*16. Assumes that  $t_{WCS} < t_{WCS}(\min)$ .
  - \*17. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
  - \*18.  $t_{CPA}$  is access time from the selection of a new column address (that is caused by changing  $\overline{CAS}$  from "L" to "H"). Therefore, if  $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA}(\max)$ .
  - \*19. Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh.
  - \*20.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If  $t_{WCS} > t_{WCS}(\min)$ , the cycle is an early write cycle and DQ pin will maintain high-impedance state throughout the entire cycle. If  $t_{CWD} > t_{CWD}(\min)$ ,  $t_{RWD} > t_{RWD}(\min)$ ,  $t_{AWD} > t_{AWD}(\min)$ , and  $t_{CPWD} > t_{CPWD}(\min)$ , the cycle is a read modify-write cycle and data from the selected cell will appear at the DQ pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the DQ pin, and write operation can be executed by satisfying  $t_{RWL}$ ,  $t_{CWL}$ , and  $t_{RAL}$  specifications.

# MB81V17400A-60/-70-60L/-70L

Fig. 2 -  $t_{RAC}$  vs.  $t_{RCD}$

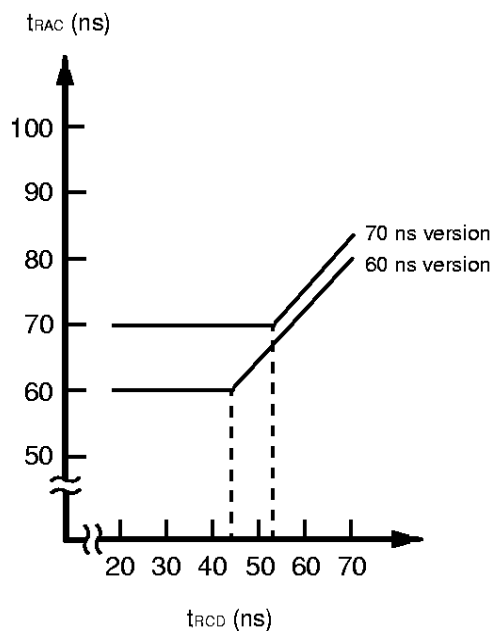
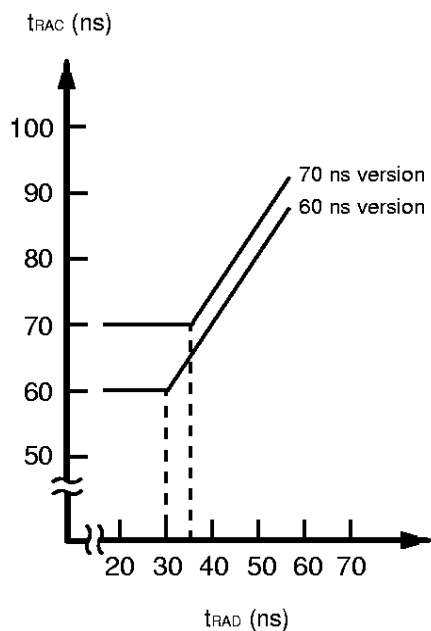
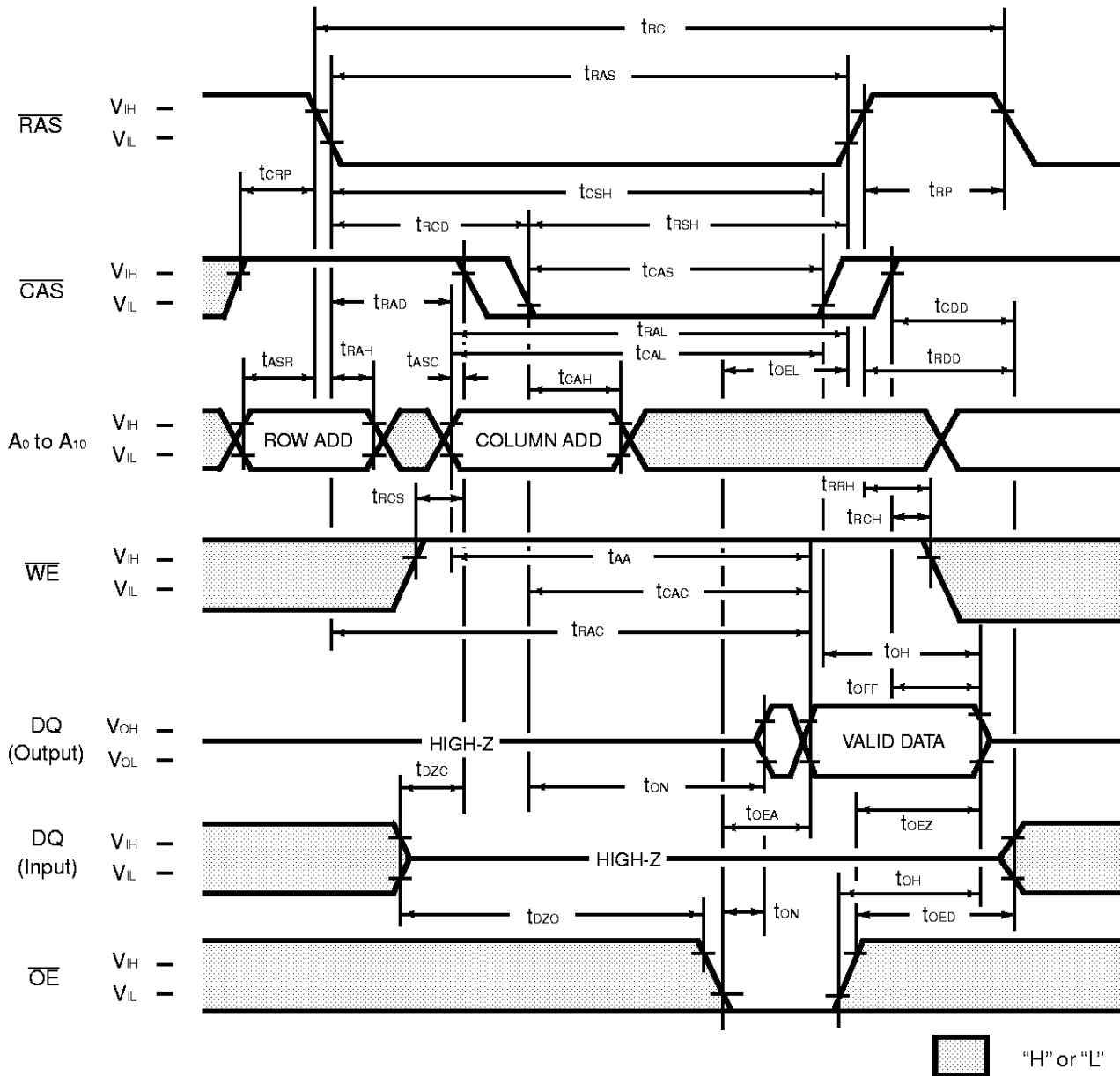


Fig. 3 -  $t_{RAC}$  vs.  $t_{RAD}$



# MB81V17400A-60/-70/-60L/-70L

Fig. 4 – READ CYCLE



## DESCRIPTION

To implement a read operation, a valid address is latched in by the  $\overline{RAS}$  and  $\overline{CAS}$  address strobes and with  $\overline{WE}$  set to a High level and  $\overline{OE}$  set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by  $RAS(t_{RAC})$ ,  $CAS(t_{CAC})$ ,  $\overline{OE}$  ( $t_{OEA}$ ) or column addresses ( $t_{AA}$ ) under the following conditions:

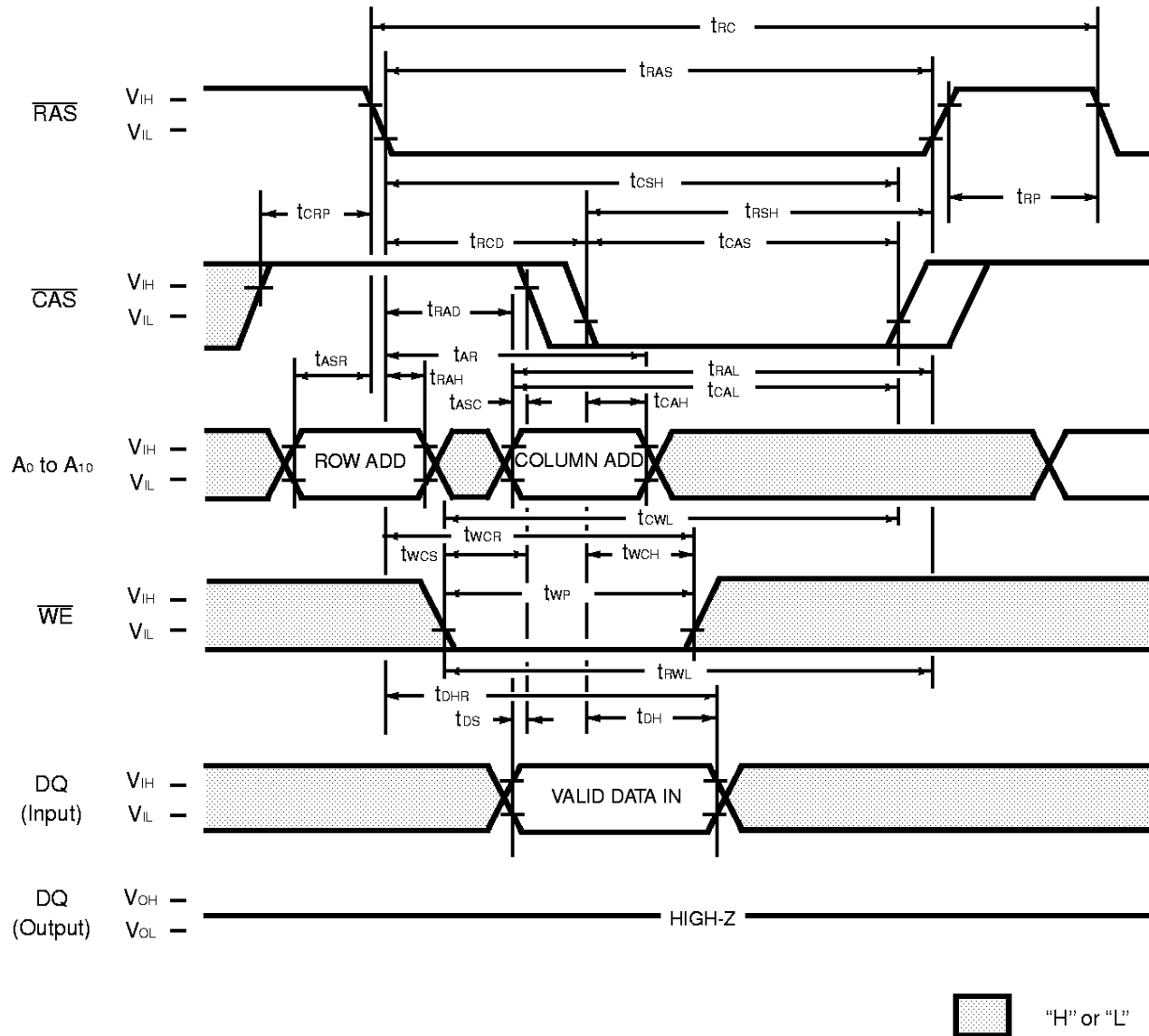
If  $t_{RCD} > t_{RCD}(\max)$ , access time =  $t_{CAC}$ .

If  $t_{RAD} > t_{RAD}(\max)$ , access time =  $t_{AA}$ .

If  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$  (whichever occurs later), access time =  $t_{OEA}$ .

However, if either  $\overline{CAS}$  or  $\overline{OE}$  goes High, the output returns to a high-impedance state after  $t_{OH}$  is satisfied.

## MB81V17400A-60/-70-60L/-70L

Fig. 5 – EARLY WRITE CYCLE ( $\overline{OE}$  = "H" or "L")**DESCRIPTION**

A write cycle is similar to a read cycle except  $\overline{WE}$  is set to a Low state and  $\overline{OE}$  is a "H" or "L" signal. A write cycle can be implemented in either of three ways – early write,  $\overline{OE}$  write (delayed write), or read-modify-write. During all write cycles, timing parameters  $t_{RWL}$ ,  $t_{CWL}$  and  $t_{RAL}$  must be satisfied. In the early write cycle shown above  $t_{WCS}$  satisfied, data on the DQ pin is latched with the falling edge of  $\overline{CAS}$  and written into memory.







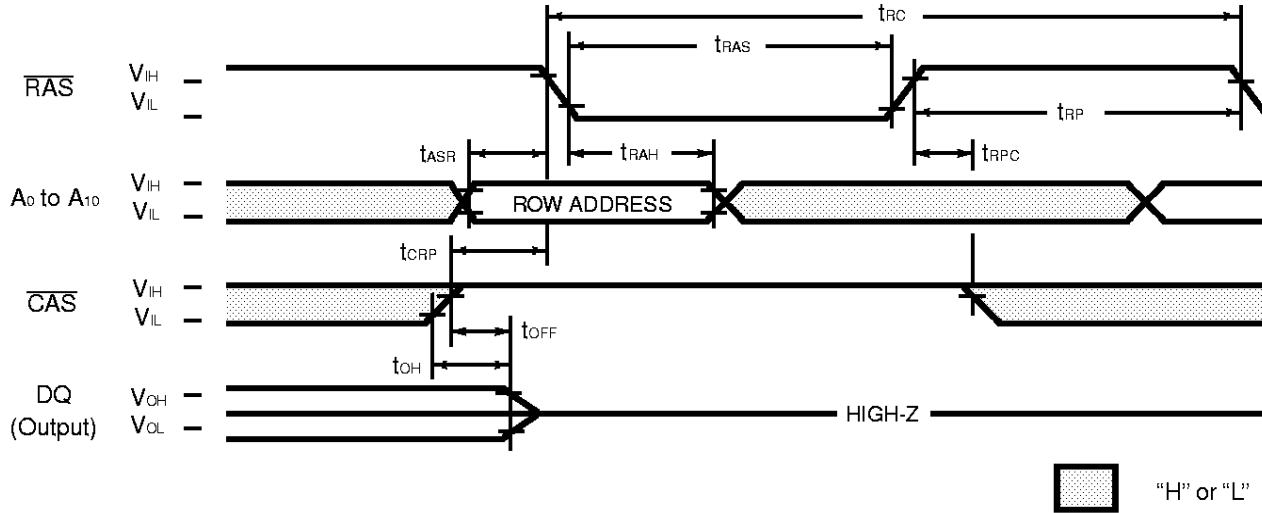






# MB81V17400A-60/-70/-60L/-70L

Fig. 12 – RAS-ONLY REFRESH ( $\overline{WE} = \overline{OE} = \text{"H"} \text{ or } \text{"L"}\text{"}$ )

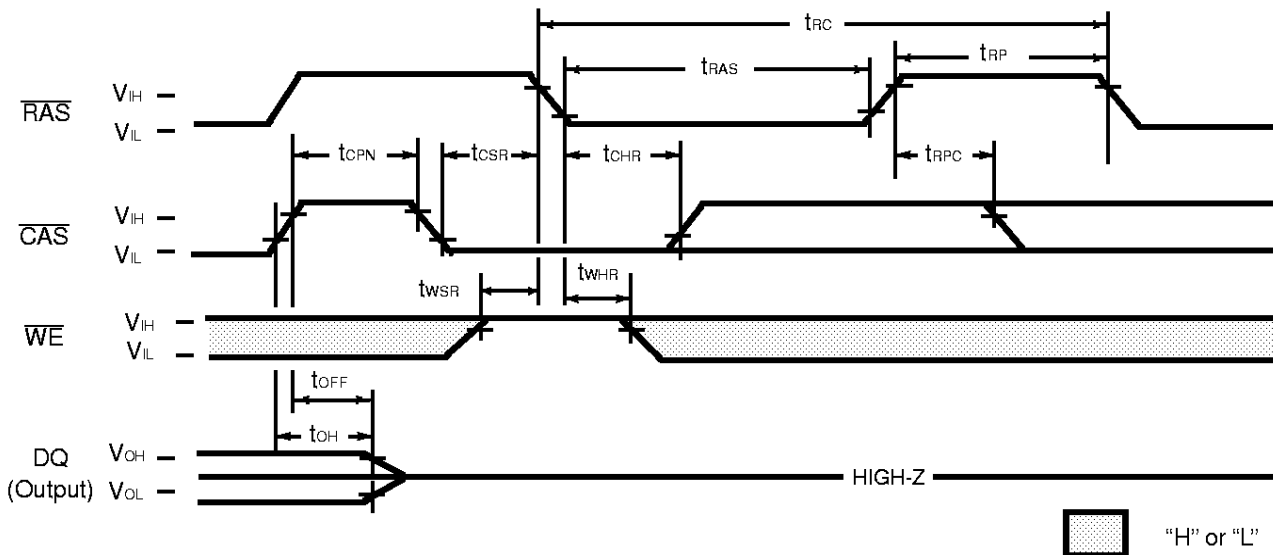


**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 2048 row addresses every 32-milliseconds. Three refresh modes are available: RAS-only refresh, CAS-before-RAS refresh, and hidden refresh.

RAS-only refresh is performed by keeping  $\overline{RAS}$  Low and  $\overline{CAS}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{RAS}$ . During RAS-only refresh, DQ pin is kept in a high-impedance state.

Fig. 13 – CAS-BEFORE-RAS REFRESH (ADDRESSES =  $\overline{OE} = \text{"H"} \text{ or } \text{"L"}\text{"}$ )

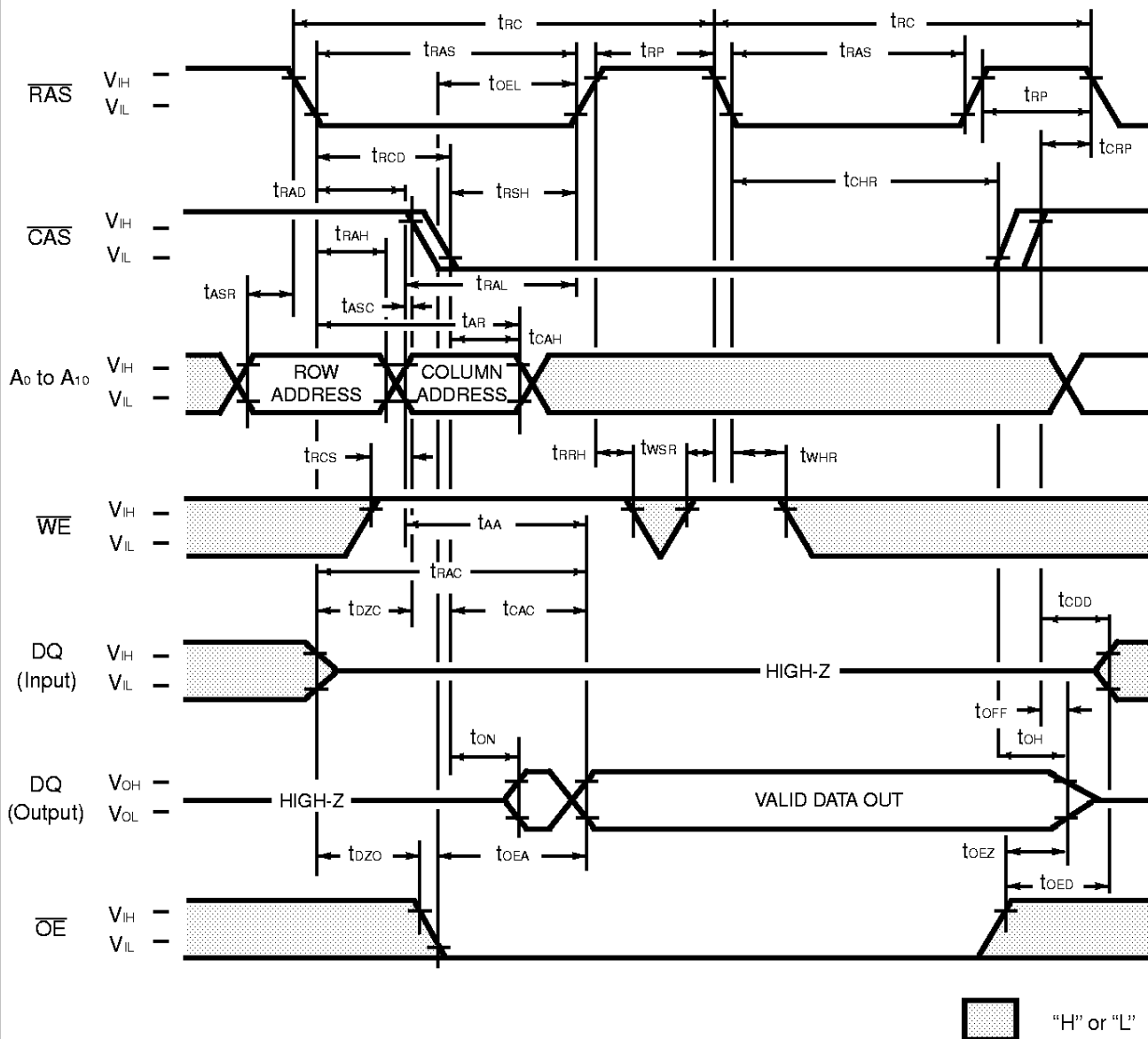


**DESCRIPTION**

CAS-before-RAS refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{CAS}$  is held Low for the specified setup time ( $t_{CSR}$ ) before  $\overline{RAS}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next CAS-before-RAS refresh operation.

# MB81V17400A-60/-70-60L/-70L

Fig. 14 – HIDDEN REFRESH CYCLE

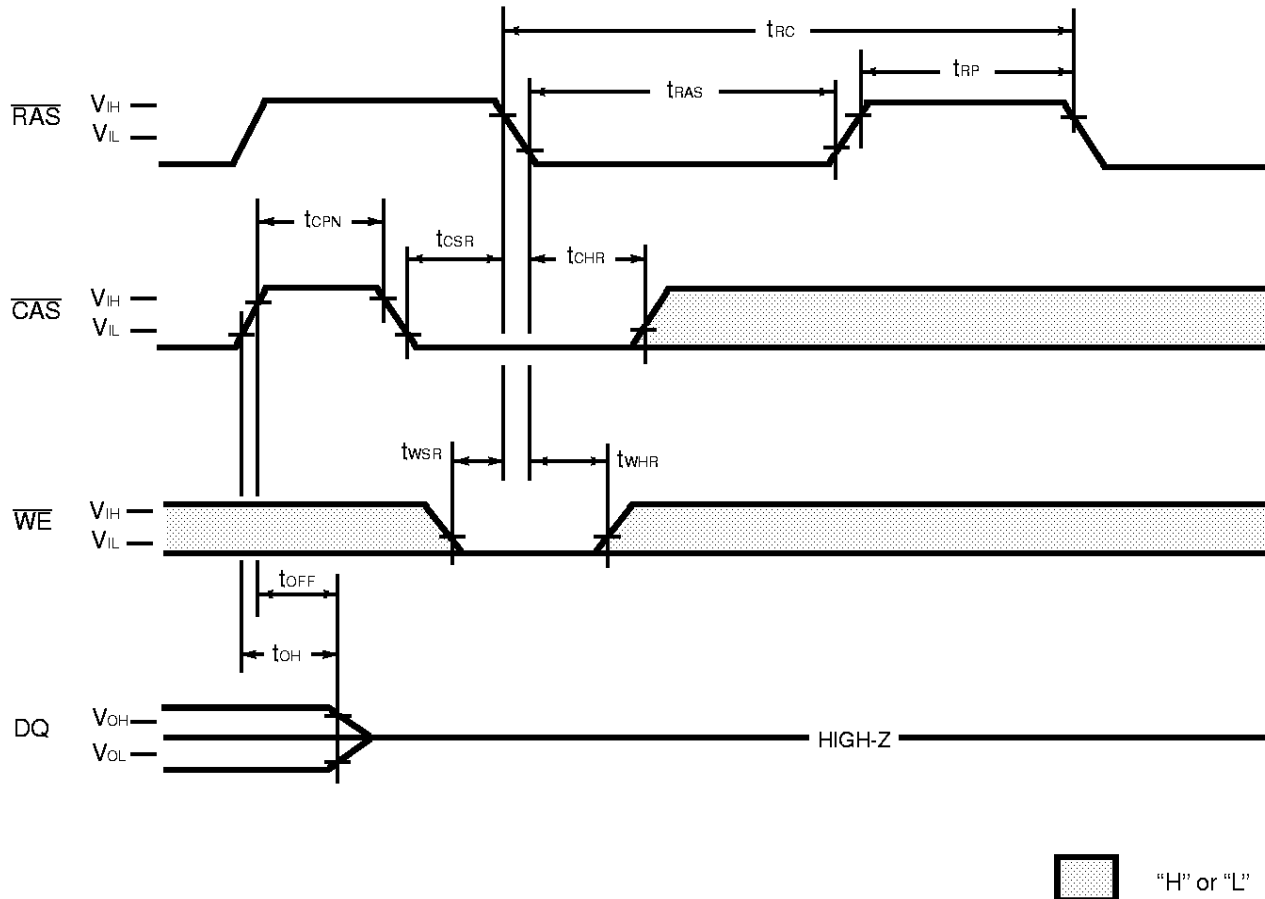


## DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{\text{CAS}}$  and cycling  $\overline{\text{RAS}}$ . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability.

# MB81V17400A-60/-70/-60L/-70L

Fig. 15 – TEST MODE SET CYCLE ( $A_0$  to  $A_{10}$ ,  $\overline{OE}$  = "H" or "L")



## DESCRIPTION

Test Mode ;

The purpose of this test mode is to reduce device test time to one sixteenth of that required to test the device conventionally. The test mode function is entered by performing a  $\overline{WE}$  and  $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) refresh for the entry cycle. In the test mode, read and write operations are executed in units of sixteenth bits which are selected by the address combination of  $\overline{CA0}$  and  $\overline{CA1}$ . In the write mode, data is written into sixteenth cells simultaneously. But the data must be input from DQ1 only. In the read mode, the data of sixteenth cells at the selected addresses are read out from DQ and checked in the following manner.

When the sixteenth bits are all "L" or all "H", a "H" level is output.

When the sixteenth bits show a combination of "L" and "H", a "L" level is output.

The test mode function is exited by performing a  $\overline{RAS}$ -only refresh or a  $\overline{CAS}$ -before- $\overline{RAS}$  refresh for the exit cycle.

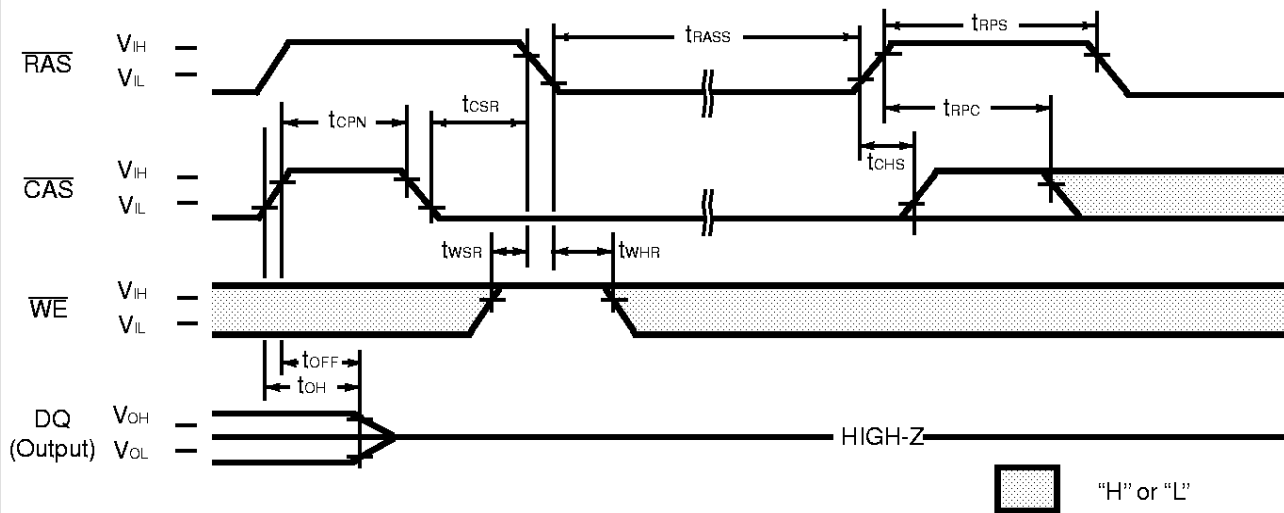
In test mode operation, the following parameters are delayed approximately 10 ns from the specified value in the data sheet.

$t_{RC}$ ,  $t_{RWC}$ ,  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{RAS}$ ,  $t_{RSH}$ ,  $t_{CAS}$ ,  $t_{CSH}$ ,  $t_{RAL}$ ,  $t_{CAL}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$ ,  $t_{CPWD}$ ,  $t_{RHCP}$ .



# MB81V17400A-60/-70/-60L/-70L

Fig. 17 – SELF REFRESH CYCLE ( $A_0$  to  $A_{10} = \overline{WE} = \overline{OE} = \text{“H” or “L”}$ )



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V17400A-60L		MB81V17400A-70L		Unit
			Min.	Max.	Min.	Max.	
100	$\overline{CAS}$ Pulse Width	$t_{RASS}$	100	—	100	—	$\mu s$
101	$\overline{RAS}$ Precharge Time	$t_{RPS}$	110	—	130	—	ns
102	$\overline{CAS}$ Hold Time	$t_{CHS}$	-50	—	-50	—	ns

Note: Assumes Self Refresh cycle only.

## DESCRIPTION

The Self Refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the Self Refresh cycle and refresh operation can be automatically executed using internal refresh address counter and generator.

If  $\overline{CAS}$  goes to "L" before  $\overline{RAS}$  goes to "L" (CBR) and the condition of  $\overline{CAS}$  "L" and  $\overline{RAS}$  "L" is kept for term of  $t_{RASS}$  (more than 100  $\mu s$ ), the device can enter the Self Refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during " $\overline{RAS} = L$ " and " $\overline{CAS} = L$ ".

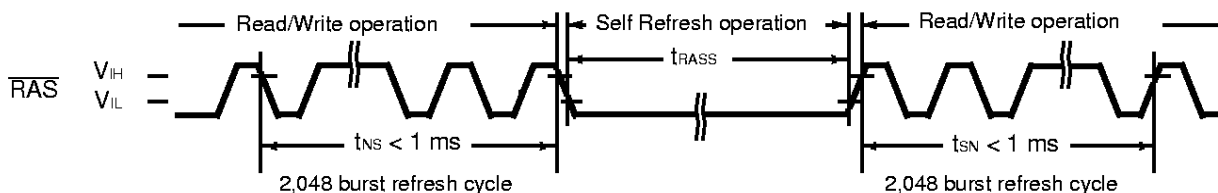
Exit from Self Refresh cycle is performed by toggling of  $\overline{RAS}$  and  $\overline{CAS}$  to "H" with specifying  $t_{CHS}$  min. In this time,  $\overline{RAS}$  must be kept "H" with specified  $t_{RPS}$  min.

Using self refresh mode, data can be retained without external  $\overline{CAS}$  signal during system is in standby.

Restriction for Self Refresh operation ;

For self refresh operation, the notice below must be considered.

- 1) In the case that distributed CBR refresh are operated in read/write cycles  
Self Refresh cycles can be executed without special rule if 2,048 cycles of distribute CBR refresh are executed within  $t_{REF}$  max.
- 2) In the case that burst CBR refresh or  $\overline{RAS}$  only refresh are operated in Read/Write cycles  
2,048 times of burst CBR refresh or 2,048 times of burst  $\overline{RAS}$  only refresh must be executed before and after Self Refresh cycles.



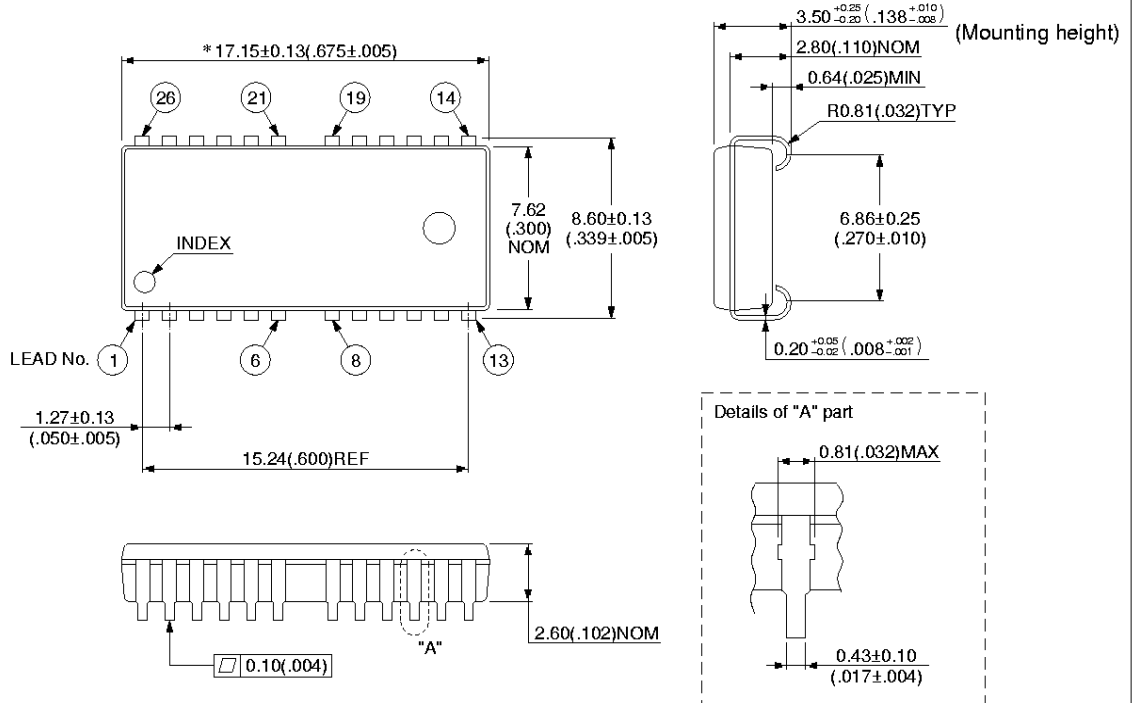
\* Read/Write operation can be performed non refresh time within  $t_{NS}$  or  $t_{SN}$ .

# MB81V17400A-60/-70-60L/-70L

## ■ PACKAGE DIMENSIONS

26-pin plastic SOJ  
(LCC-26P-M09)

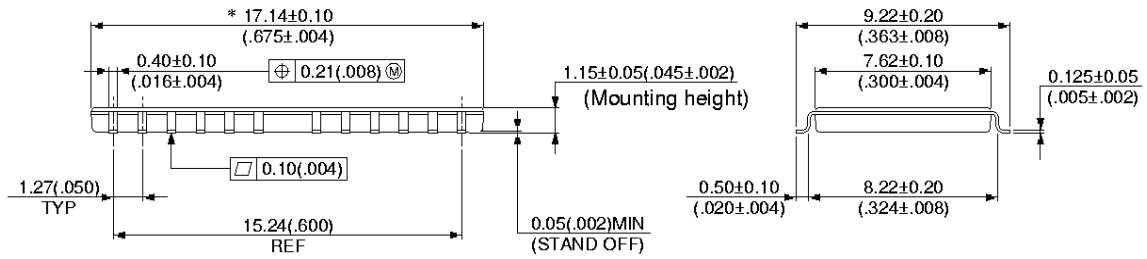
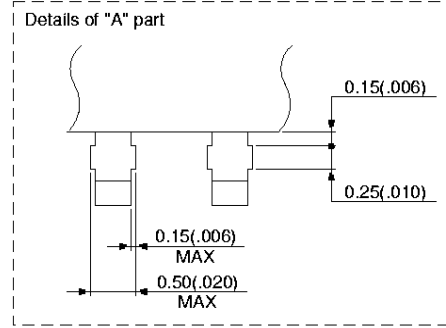
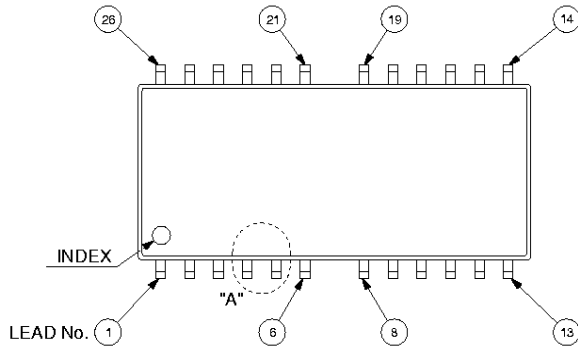
\*: Resin protrusion. (Each side: 0.15 (.006) max.)



# MB81V17400A-60/-70/-60L/-70L

26-pin plastic TSOP(II)  
(FPT-26P-M05)

\*: Resin protrusion. (Each side: 0.15 (.006) max.)



©1994 FUJITSU LIMITED F26005S-2C-1

Dimensions in mm (inches)

# MB81V17400A-60/-70-60L/-70L

## FUJITSU LIMITED

*For further information please contact:*

### Japan

FUJITSU LIMITED  
Corporate Global Business Support Division  
Electronic Devices  
KAWASAKI PLANT, 4-1-1, Kamikodanaka  
Nakahara-ku, Kawasaki-shi  
Kanagawa 211-88, Japan  
Tel: (044) 754-3763  
Fax: (044) 754-3329

<http://www.fujitsu.co.jp/>

### North and South America

FUJITSU MICROELECTRONICS, INC.  
Semiconductor Division  
3545 North First Street  
San Jose, CA 95134-1804, U.S.A.  
Tel: (408) 922-9000  
Fax: (408) 922-9179

Customer Response Center  
*Mon. - Fri.: 7 am - 5 pm (PST)*  
Tel: (800) 866-8608  
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

### Europe

FUJITSU MIKROELEKTRONIK GmbH  
Am Siebenstein 6-10  
D-63303 Dreieich-Buchsschlag  
Germany  
Tel: (06103) 690-0  
Fax: (06103) 690-122

<http://www.fujitsu-edc.com/>

### Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD  
#05-08, 151 Lorong Chuan  
New Tech Park  
Singapore 556741  
Tel: (65) 281-0770  
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

F9708

© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

#### CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.