

## FEATURES

- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards and IEEE 802.3z Gigabit Ethernet Applications
- Transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- Receiver PLL configured for clock and data recovery
- 1250 and 1062 Mb/s operation
- 8-bit parallel TTL compatible interface
- 1.6W typical power dissipation
- +3.3V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- 64 PQFP/TEP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- Drives 30m of Twinax cable directly

- Proprietary extended backplanes
- RAID drives
- Mass storage devices

## GENERAL DESCRIPTION

The S2061 transmitter and receiver chip is designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification. The chip runs at 1250.0, and 1062.5 Mbit/s data rates with associated 10-bit data word.

The chip performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The transmitter's on-chip PLL synthesizes the high-speed clock from a low-speed reference. The receiver's on-chip PLL synchronizes directly to incoming digital signal to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback mode is provided for system diagnostics.

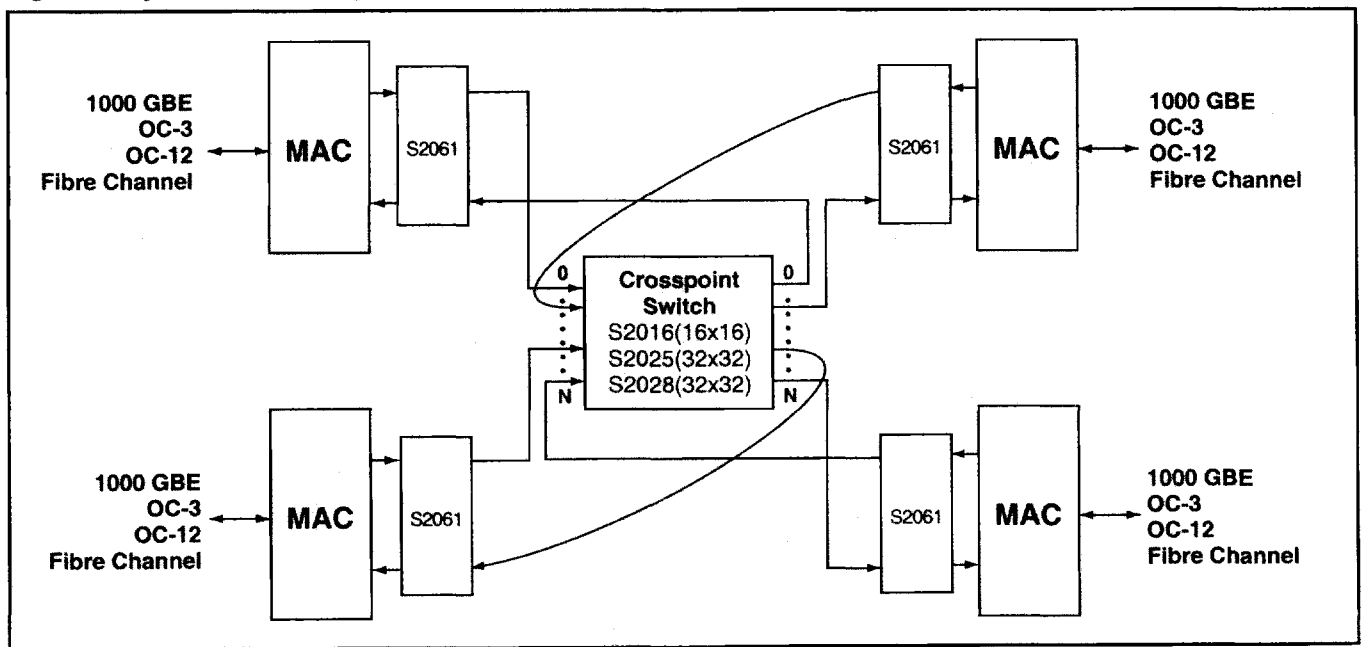
Figure 1 shows a typical configuration incorporating the chip, which is compatible with AMCC's Crosspoint switch products.

## APPLICATIONS

High-speed data communications

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments

Figure 1. System Block Diagram



### 8B/10B Coding

The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. It uses the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into a 10-bit transmission character. Information received is recovered 10 bits at a time and those transmission characters used for data ("D"-type) are decoded into one of the correct 256 8-bit combinations.

Refer to Reference (1) for the complete listing of valid data characters. Some of the remaining transmission characters ("K"-type) are used for functions associated with control signals related to protocol management. Codes detected at the receiver that are not D- or K-type are flagged as errors.

The characters defined by this transmission code ensure that short run lengths and enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of data.

### S2061 OVERVIEW

The S2061 transceiver performs encoding/decoding parallel to serial/serial to parallel conversion and framing functions to implement a Serial Backplane interface. Operation of the S2061 chip is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

#### Transmitter

1. 8-bit parallel input
2. 8B/10B encoding
3. Parallel-to-serial conversion
4. Serial output

#### Receiver

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10B/8B decoding
5. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 6, 7, 8.

A lock detect feature is provided for the receive PLL. The LOCKDET output indicates that the PLL is locked to the data stream.

### Loopback Modes

Local loopback mode is supported by the chip. Local loopback provides capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics. (See the section Other Operating Modes.)

### S2061 TRANSMITTER DESCRIPTION

#### Parallel Inputs

Data is input to the S2061 using eight LVTTTL (5V tolerant) signals. Data is latched into an input register on the rising edge of the input reference clock.

#### 8B/10B Encoder

The encoder accepts byte-wide data from the input register. Performs the 8B/10B encoding function, and converts from a parallel to serial bit stream. The S2061 generates the special characters required for Interframe and Transmit error functions. As a result from the extra overhead of the 8B/10B encoding, this data is transmitted at 1250 Mbit/s.

#### Frequency Synthesizer (PLL)

The S2061 lock detect function indicates the state of the phase-locked loop (PLL) clock synthesis unit. The S2061 will obtain phase and frequency lock after the start of receiving data inputs. Upon acquisition and maintaining of lock, the LOCKDET output will go high. If lock is lost then LOCKDET will go low.

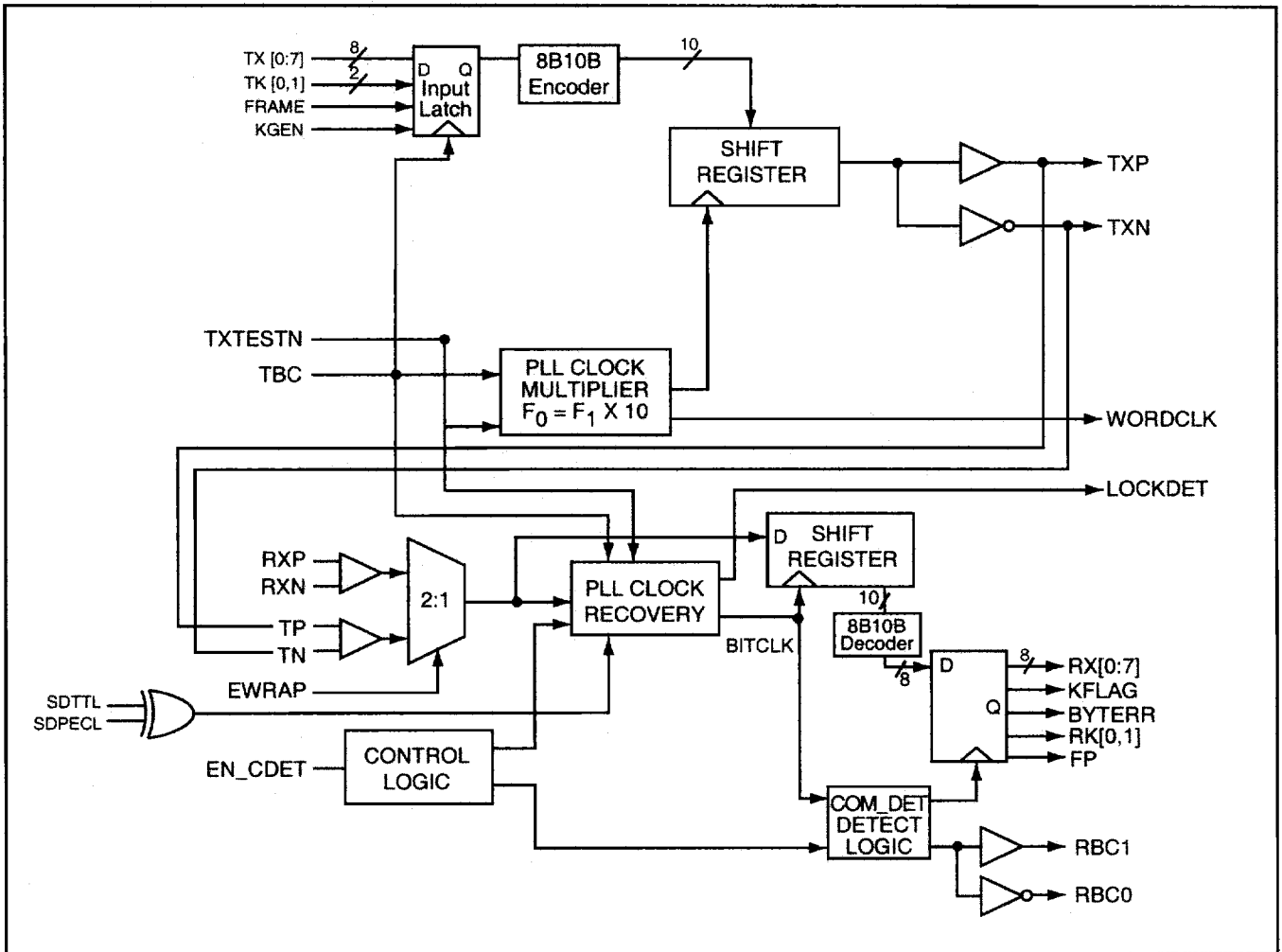
#### Test Functions

The S2061 has a testability input to aid in functional testing of the device. The TXTESTN input allows the internal voltage-controlled oscillator (VCO) to be bypassed and the reference clock substituted. This allows full functional testing of the digital portion of the chip or bypassing the internal synthesized clock with an external clock source. (See the section Other Operating Modes.)

#### Reference Clock Input

The reference clock input must be supplied with a crystal clock source with 100 PPM tolerance.

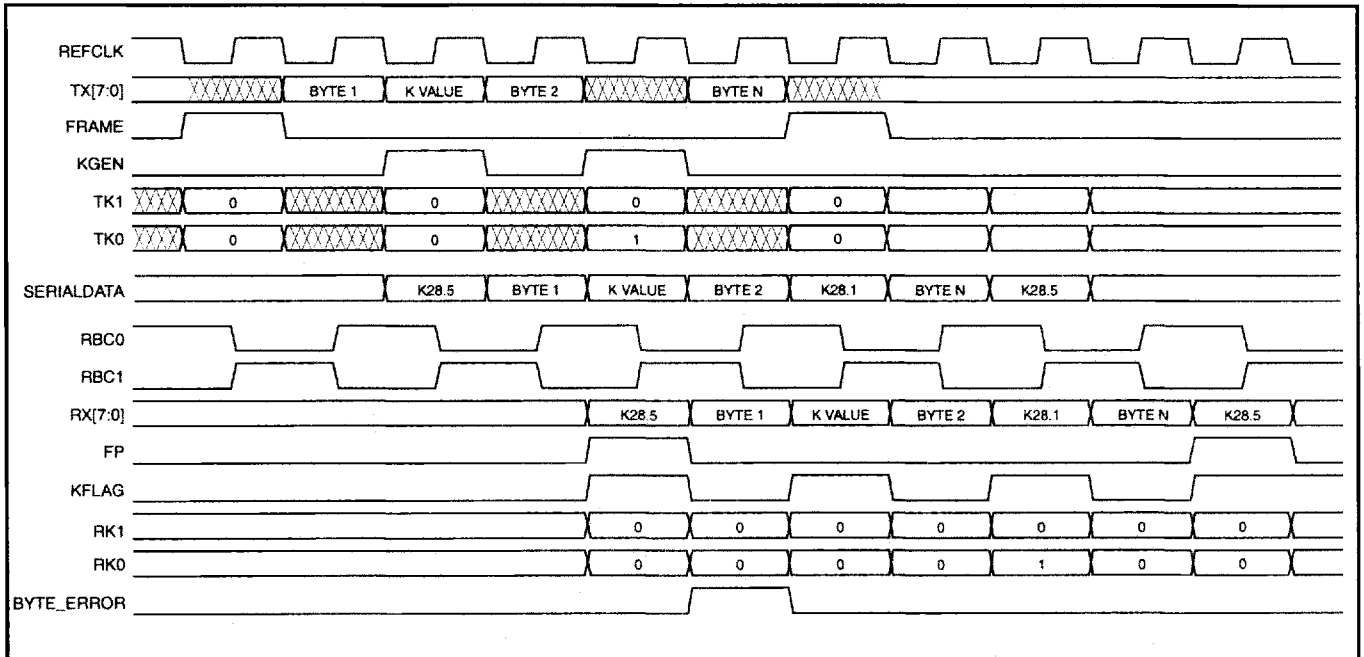
Figure 2. Functional Block Diagram



**Table 1. Character Generation**

FRAME	TK1	TK0	KGEN	TX[7:0]	STATE
1	0	0	0	X	K28.5 Running disparity generated.
0	0	0	1	K Character Value	K character of running disparity generated value on D[0:7].
0	0	1	1	X	K28.1 of running disparity generated.
0	1	0	1	X	K28.3 of running disparity generated.
0	1	1	1	X	K28.7 of running disparity generated.
0	X	X	0	Data	D character generated.

**Figure 3. Functional Waveform (1250 and 1062.5 Mbit/sec)**



1. A.X. Widmer and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC 9391, May 1982.

**RECEIVER DESCRIPTION**

**Architecture/Functional Description**

The receiver is designed to implement a Serial Backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 2.

The receiver accepts serial encoded data from a fiber optic or coaxial interface. Clock recovery is performed on-chip, with the output data presented as 8-bit parallel data.

Whenever a signal is present, the receiver attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. When bit synchronization is achieved, it is indicated by the LOCKDET signal. Word synchronization is achieved by monitoring the incoming serial data stream for the comma character with negative disparity (0011111XXX). All K28.5 characters, with the correct byte alignment, of either disparity will be indicated by FP. Additional K characters are also decoded per Table 2. When word synchronization is achieved, the receiver provides the valid decoded data on its parallel outputs.

**Decoder**

The decoder accepts a serial bit stream, does serial to byte-wide parallel conversion, and performs the 10B/8B decoding function. The framer recognizes the negative disparity K28.5 to correctly frame the data.

**Byte Synchronization and Framing**

The Receiver section performs byte synchronization on the incoming data stream. Byte synchronization is performed on only the negative disparity Fibre Channel comma character (0011111XXX). The FP signal will be active whenever a K28.5 character of either disparity is detected. This allows the FRAME input of the transmitter and the FP output on the receiver to be used to 'envelope' the data packet.

**Table 2. Character Detection<sup>1</sup>**

FP	RK1	RK0	KFLAG	STATE
1	0	0	1	K28.5 detected.
0	0	0	1	K character detected value on TX[0:7].
0	0	1	1	K28.1 detected.
0	1	0	1	K28.3 detected.
0	1	1	1	K28.7 detected.
0	0	0	0	D character.

1. K characters are detected with either positive or negative disparity.

**Lock Detect**

The S2061 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the received serial data fails the run length or frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the RBC1/0 output under loss of signal or loss of lock conditions. If the serial data inputs have a run length of 80 bit times with no transitions, the PLL will be declared out of lock. In addition, if the recovered clock frequency deviates from the local reference clock frequency by more than approximately 600 ppm, the PLL will also be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within approximately 300 ppm and the run length check indicates valid data, the PLL will be declared in lock and the lock detect output will go active.

In any transfer of PLL control from the serial data to the reference clock, the RBC1/0 output remains phase continuous and glitch free assuring the integrity of downstream clocking.

**Reference Clock Input**

The reference clock input must be supplied with a crystal clock source with 100 PPM tolerance.

**OTHER OPERATING MODES**

**Loopback**

When local loopback is enabled, serial data from the transmitter is internally routed to the receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

**Operating Frequency Range**

The S2061 is optimized for operation at 1250 and 1062 Mbit/s. Operation at other rates is possible if the rate falls between the nominal rates. TBC must be selected to be within 100 ppm of the desired byte or word clock rate.

**Table 3. S2061 Transmitter Pin Assignment and Descriptions**

Pin Name	Level	I/O	Pin #	Description
TX7 TX6 TX5 TX4 TX3 TX2 TX1 TX0	TTL	I	38 40 41 42 43 45 46 47	Transmit data. Parallel data on this bus is clocked in on the rising edge of TBC. TX0 is transmitted first.
TBC	TTL	I	27	Reference clock and transmit byte clock, a crystal-controlled reference clock for the PLL clock multiplier. The frequency of TBC is the bit rate divided by 10.
TXTESTN	TTL	I	39	When toggled 0V/1.5V, TXTESTN replaces internal test input. Tie High for normal operation.
TXP TXN	Diff. PECL	O	51 52	Differential PECL outputs that send out the serial transmitter data and drive 75Ω or 50Ω termination to Vcc-2V. TXP is the positive output, and TXN is the negative output.
TK0 TK1	LVTTTL	I	37 36	Transmit K character. Active High. These inputs allow additional K characters to be automatically generated by the encoder. (See Table 1.)
KGEN	LVTTTL	I	33	K Char Gen. Used to specify data (D) or control (K) for parallel data bits 0-7.
FRAME	LVTTTL	I	32	Active High. If KGEN is 0, the FRAME input controls the transmission of data or K28.5 characters. When active, a K28.5 character with correct running disparity will be generated by the transmit encoder. When inactive, the data byte present on DATAIN<7:0> will be encoded with the correct running disparity.
WORDCLK	LVTTTL	O	44	Word clock for encoder. The encoder operates synchronously to this clock. The frequency of the WORDCLK is the bit rate divided by 20.

**Table 4. S2061 Receiver Pin Assignment and Descriptions**

Pin Name	Level	I/O	Pin #	Description
RX7 RX6 RX5 RX4 RX3 RX2 RX1 RX0	TTL	O	13 11 10 9 8 6 5 4	Receive data outputs. Parallel data on this bus is valid on the rising edge of RBC0 and RBC1. RX0 is the first bit received.
RBC1 RBC0	Diff. TTL	O	19 18	Receive clock. Parallel data is valid on the rising edge of RBC0 and RBC1 (see timing diagram in Figure 8). After a sync word is detected, the period of the current RBC1 and RBC0 is stretched to align with the word boundary.

**Table 4. S2061 Receiver Pin Assignment and Descriptions (Continued)**

Pin Name	Level	I/O	Pin #	Description
EN_CDET	TTL	I	25	Enable comma detect. When High, enables sync detection. Detection of the 7-bit comma + character sync pattern, RX(0-9) = (K28.5:0011111XXX), will enable the word boundary for the data to follow. When Low, data is treated as unframed data.
RXP RXN	Diff. LVPECL	I	59 61	(Externally capacitively coupled.) Differential LVPECL received serial data inputs. RXP is the positive input, and RXN is the negative input. Internally biased.
FP	TTL	O	2	Frame Pulse. Active High. When active FP indicates that a K28.5 character of either disparity has been detected and is present on RX<0:7>. Note: Byte alignment is performed on the 7 bit comma character with negative disparity (0011111XXX), not the full K28.5.
LOCKDET	LVTTTL	O	64	Lock Detect. Active High. Indicates that the receiver has achieved bit synchronization (PLL lock).
KFLAG	LVTTTL	O	16	K Character Flag. Active High. Indicates the decoded data byte is a special character (K byte). Control information is indicated whenever KFLAG is high; a low indicates data.
BYTERR	LVTTTL	O	1	Byte Error Flag. Active High. Indicates the received byte contained a character or disparity error.
SDTTL	LVTTTL	I	22	Signal Detect. Active High when SDPECL is unconnected (logic 0). Active Low when SDPECL is held at logic 1. A single-ended LVTTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDTTL is inactive, the data on the RXP/N pins will be internally forced to a constant zero. When SDTTL is active, data on the RXP/N pins will be processed normally.
SDPECL	LVPECL	I	21	Signal Detect. LVPECL with internal 1 k pull-down. Active High when SDTTL is held at logic 0. A single-ended 10K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDPECL is inactive, the data on the Serial Data In (RXP/N) pins will be internally forced to a constant zero. When SDPECL is active, data on the RXP/N pins will be processed normally. When SDTTL is to be connected to the optical receiver module instead of SDPECL, then SDPECL should be tied High to implement an active low Signal Detect, or left unconnected to implement an active high Signal Detect.
RK0 RK1	LVTTTL	O	14 15	Receive K Character. Active High. These outputs indicate reception of the K28.1, K28.3, and K28.7 K characters. (See Table 2.)

**Table 5. S2061 Common Pin Assignment and Descriptions**

Pin Name	Level	I/O	Pin #	Description
EWRAP	TTL	I	30	Enable Wrap input. When High, selects the transmitter serial output data to be routed to the receiver. When Low, selects RXP and RXN (normal operation). TXP, TXN are static when EWRAP is High.
RST	TTL	I	23	Active Low. Used to initialize the chip for factory test.
RATESEL	TTL	I	56	Used for factory test. Tie High for normal operation.
ECLVCC	-	-	29 26 53 58	Core +3.3V
ECLVEE	-	-	24 28 35 48 57	Core Ground
TTLGND			3 17	TTL Ground
TTLVCC			7 12	TTL +3.3V
ECLIOVCC			50	PECL I/O +3.3V
ECLIOVEE			55 49	PECL I/O Ground
AVCC			31 63	Analog +3.3V
AVEE			34 62	Analog Ground
NC	-	-	20 54 60	No Connection

**Figure 4. Pin Description and Assignment**

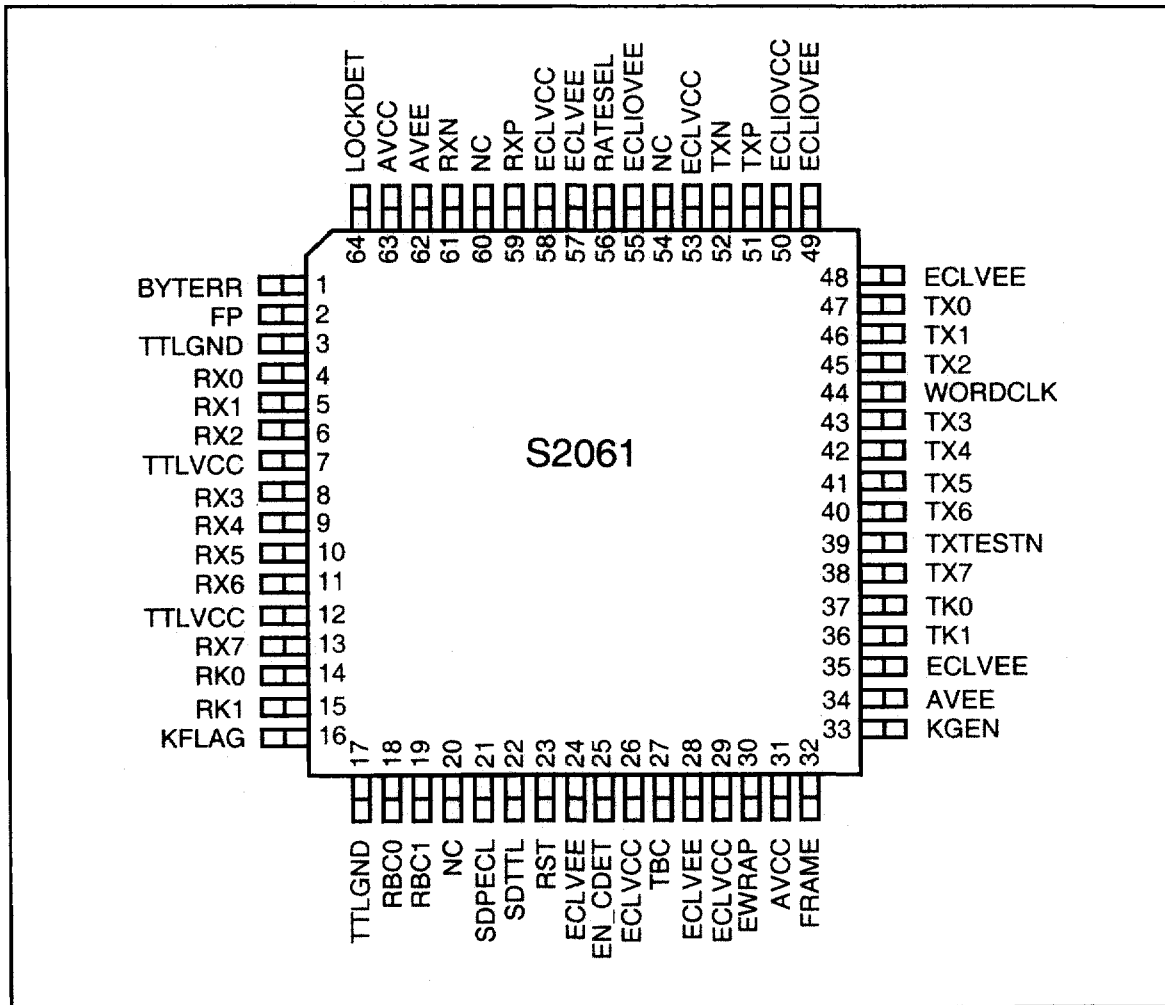
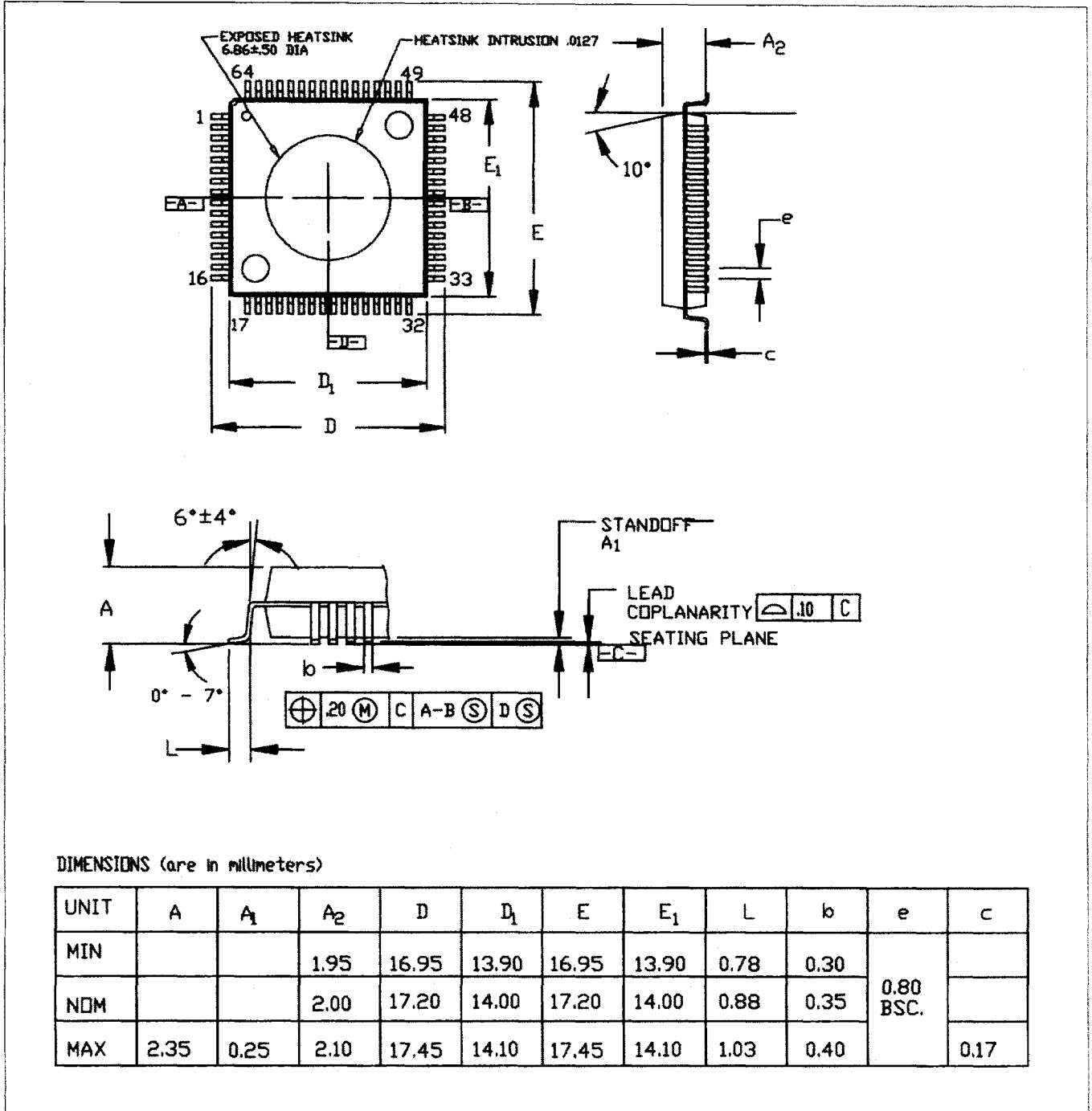


Figure 5. 64 PQFP/TEP (14mm x 14mm) Package



**Thermal Management**

Device	Power	θ <sub>ja</sub>	θ <sub>jc</sub>
S2061	2.0W Max	30°C/W	2.5°C/W

**Table 6. Absolute Maximum Ratings**

PARAMETER	MIN	TYP	MAX	UNIT
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin except Tx [0:7]	-0.5		3.47	V
Voltage on TTL input pin TX [0:7]			+5.5	V
Voltage on any PECL Input Pin	0		VCC	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

**Table 7. Recommended Operating Conditions**

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias			130	°C
Voltage on TTLVCC, ECLVCC, ECLIOVCC, and AVCC with respect to GND/VEE	3.13	3.3	3.47	V
Voltage on TTL Input Pin except TX [0:7]	0		3.47	V
Voltage on any PECL Input Pin	VCC -2.0		VCC	V
Voltage on TTL data TX [0:7]	0		5.0	

**Table 8. Reference Clock Requirements**

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	—
TD <sub>1-2</sub>	Symmetry	40	60	%	Duty Cycle at 50% pt.
T <sub>RCR</sub> , T <sub>RCF</sub>	REFCLK Rise and Fall Time	—	2	ns	20 – 80%
—	Random Jitter		100	ps	Peak-to-Peak

**Table 9. S2061 DC Characteristics**

Parameters	Description	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage (TTL)	2.2	2.5	$V_{CC}$	V	$V_{CC} = \text{min}, I_{OH} = -400 \mu\text{A}$
$V_{OL}$	Output LOW Voltage (TTL)	GND	.025	0.5	V	$V_{CC} = \text{max}, I_{OL} = 1 \text{ mA}$
$V_{IH}$	Input HIGH Voltage (TTL)	2.0	—	—	V	$I_H \leq 1 \text{ mA}$ at $V_{IH} = 5.5 \text{ V}$
$V_{IL}$	Input LOW Voltage (TTL)	GND	—	0.8	V	—
$I_{IH}$	Input HIGH Current (TTL)	—	—	40	$\mu\text{A}$	$V_{IN} = 2.4 \text{ V}, V_{CC} = \text{max}$
$I_{IL}$	Input LOW Current (TTL)	—	—	600	$\mu\text{A}$	$V_{IN} = 0.4 \text{ V}, V_{CC} = \text{max}$
$I_{CC}$	Supply Current		485	577	mA	Outputs open, $V_{CC} = V_{CC} \text{ max}$ SQ pattern
$P_D$	Power Dissipation		1.6	2.0	W	Outputs open, $V_{CC} = V_{CC} \text{ max}$ SQ pattern
$V_{DIFF}$	Min. differential input voltage swing for differential PECL inputs	100		1300	mV	
$\Delta V_{OUT}$	Serial Output Voltage Swing	600	—	1600	mV	$50\Omega$ to $V_{CC} - 2.0 \text{ V}$
$C_{in}$	Input capacitance	—		4	PF	

**Table 10. S2061 Performance Summary**

Parameter	S2061		Units
Operating Frequency *	1250	1062.5	Mbit/s
Serial clock period	.800	.941	ns
Byte clock period	8.00	9.41	ns
Acquisition Time	250	250	ns
Reference clock	125.0	106.25	MHz
Word width	10	10	Bits

\* ±10% lock range, nominal frequency is per FC-PH standard.

**Table 11. S2061 Transmitter Timing**

Parameters	Description	Min	Max	Units	Conditions
$T_1$	Data setup w.r.t. $\uparrow$ REFCLK	2	—	ns	See note.
$T_2$	Data hold w.r.t. $\uparrow$ REFCLK	1.0	—	ns	—
$T_{SDR}, T_{SDF}$	Serial data rise and fall	—	300	ps	20% to 80%, tested on a sample basis.
<b>Transmitter Output Jitter Allocation</b>					
$T_{J,RMS}$	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis. Measured with 1010 pattern.
$T_{DJ}$	Serial data output deterministic jitter (p-p)	—	80	ps	Peak-to-peak, tested on a sample basis. Measured with K28.5± @ 1.25 GHz pattern.

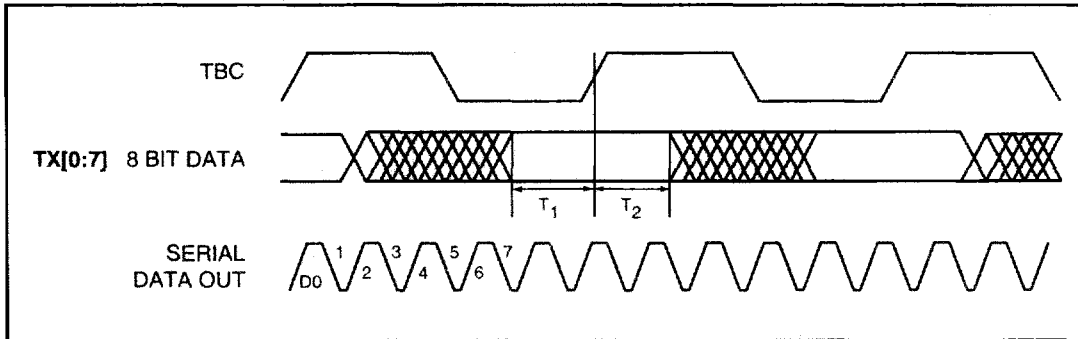
Note: All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

**Table 12. S2061 Receiver Timing**

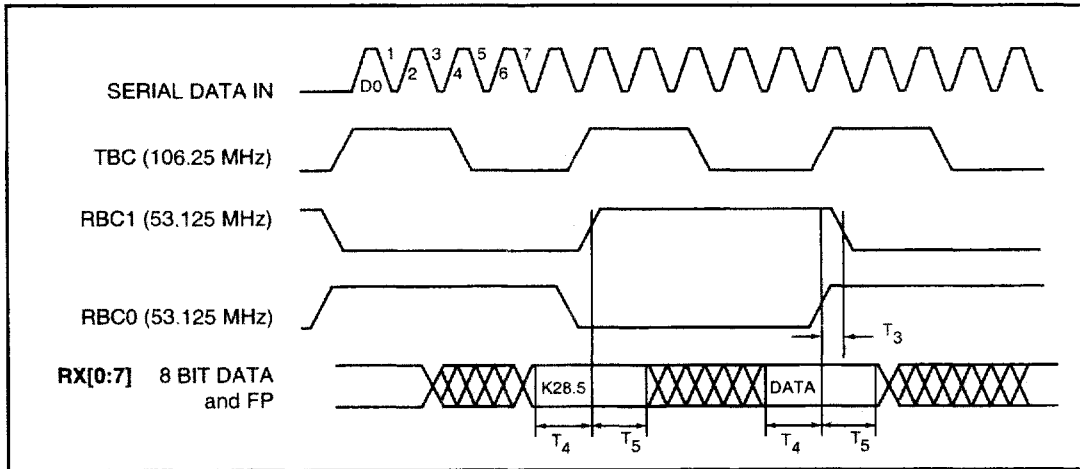
Parameters	Description	Min	Max	Units	Conditions
$T_3$	RBC0 to RBC1 skew	—	1	ns	Tested on a sample basis.
$T_4$	Data setup w.r.t. RBC0, RBC1	3.0		ns	1.0625 GHz Mode
$T_5$	Data hold w.r.t. RBC0, RBC1	1.5		ns	1.0625 GHz Mode
$T_6$	Data setup w.r.t. RBC0, RBC1	2.5		ns	1.250 GHz Mode
$T_7$	Data hold w.r.t. RBC0, RBC1	1.5		ns	1.250 GHz Mode
$T_{RCR}, T_{RCF}$	RBC0, RBC1 rise and fall time	—	3.0	ns	Measured from .8V to 2.0V.
$T_{DR}, T_{DF}$	Data Output rise and fall time	—	3.0	ns	Measured from .8V to 2.0V.
$T_{SDR}, T_{SDF}$	Serial data input rise and fall	—	300	ps	20% to 80%. (See Figure 10.)
$T_{LOCK}$	Data acquisition lock time @ <1.0625Gb/s	—	2.4	μs	8B/10B IDLE pattern sample basis
Duty Cycle	RBC0/RBC1 Duty Cycle	40%	60%		
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤1E-12	30%	—	bit time	As specified in Fibre Channel FC-PH standard eye diagram jitter mask.

Note: All TTL/CMOS AC measurements are assumed to have the output load of 10pF.

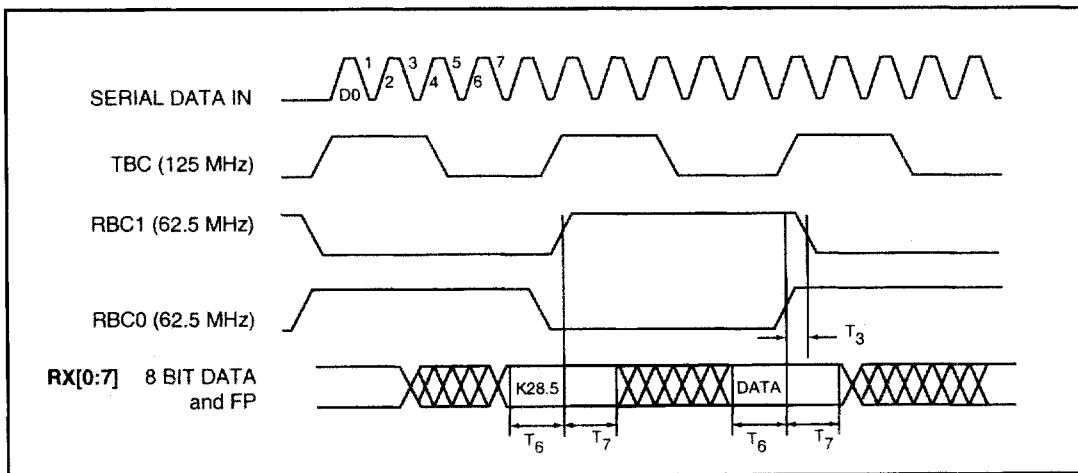
**Figure 6. Transmitter Timing Diagram**



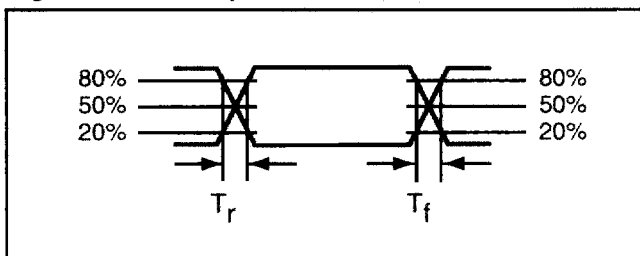
**Figure 7. Receiver Timing Diagram (1062.5 Mbits/sec mode)**



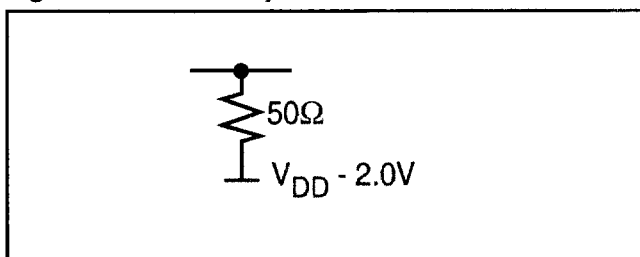
**Figure 8. Receiver Timing Diagram (1250 Mbits/sec mode)**



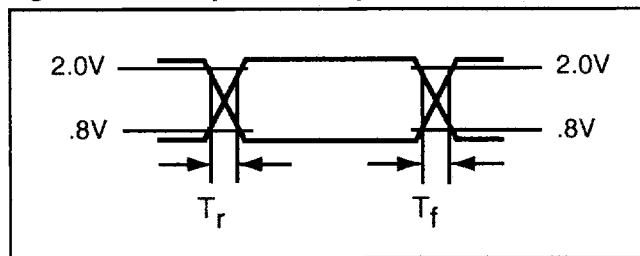
**Figure 9. Serial Input Rise and Fall Time**



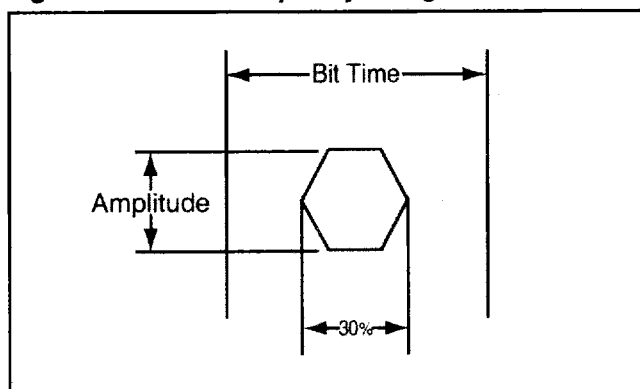
**Figure 10. Serial Output Load**



**Figure 11. TTL Input and Output Rise and Fall Time**



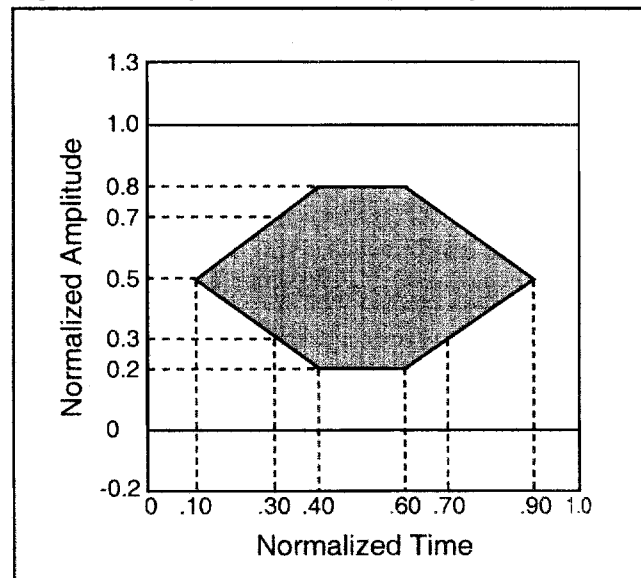
**Figure 12. Receiver Input Eye Diagram Jitter Mask**



**ACQUISITION TIME**

With the input eye diagram shown in Figure 12, the S2061 will recover data with a  $10^{-9}$  BER within 50 bit times after an instantaneous phase shift of the incoming data.

**Figure 13. Acquisition Time Eye Diagram**



**Ordering Information**

<b>GRADE</b>	<b>DEVICE</b>	<b>PACKAGE</b>
S – commercial	2061	B – 64 PQFP/TEP (14mm)

**X**    **XXXX**    **X**  
Grade    Part number    Package



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