TM4256HE4
524,288 BY 4-BIT DYNAMIC RAM MODULE

SEPTEMBER 1985 – REVISED NOVEMBER 1985

- 524,288 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- 24-Pin Single-in-Line Package (SIP)
- Utilizes Eight 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

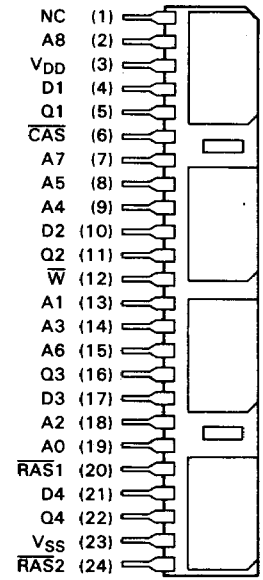
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4256-12	120 ns	60 ns	230 ns	270 ns
TMS4256-15	150 ns	75 ns	260 ns	305 ns
TMS4256-20	200 ns	100 ns	330 ns	370 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4256HE4-12	2600 mW	100 mW
TM4256HE4-15	2400 mW	100 mW
TM4256HE4-20	1800 mW	100 mW

- Operating Free-Air Temperature . . . 0°C to 70°C

E SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



†$\overline{RAS}1$ is the row-address strobe for side 1, and $\overline{RAS}2$ is the row-address strobe for side 2. Side 1 is shown in top view.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
$\overline{RAS}1$, $\overline{RAS}2$	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256HE4 is a 2048K, dynamic random-access memory module organized as 524,288 X 4 bits in a 24-pin single-in-line package (SIP) comprising eight TMS4256FML, 262,144 X 1 bit dynamic RAM's in 18-lead plastic-chip carriers mounted on both sides of a substrate together with four 0.2 μF decoupling capacitors. The on-board capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.475 inch board spacing, the TM4256HE4 has a density of seven devices per square inch (approximately 2.8X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

The TM4256HE4 is organized as two banks of 256K X 4 selected by $\overline{RAS}1$, $\overline{RAS}2$; $\overline{CAS}$ and $\overline{W}$ which are common to all devices. The D and Q signals are common to pairs of devices on opposing sides of the substrate. This configuration requires that only one $\overline{RAS}$ signal be active during a read or write cycle to prevent data bus contention or writing erroneous data. On refresh cycles ($\overline{CAS}$ high), $\overline{RAS}1$ and $\overline{RAS}2$ can be low at the same time.

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Each TMS4256FML is described in the TMS4256 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed.

operation

The TM4256HE4 operates as eight TMS4256s connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of its operation.

specifications

For TMS4256 electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

PC substrate: 1,14 mm (0.045 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

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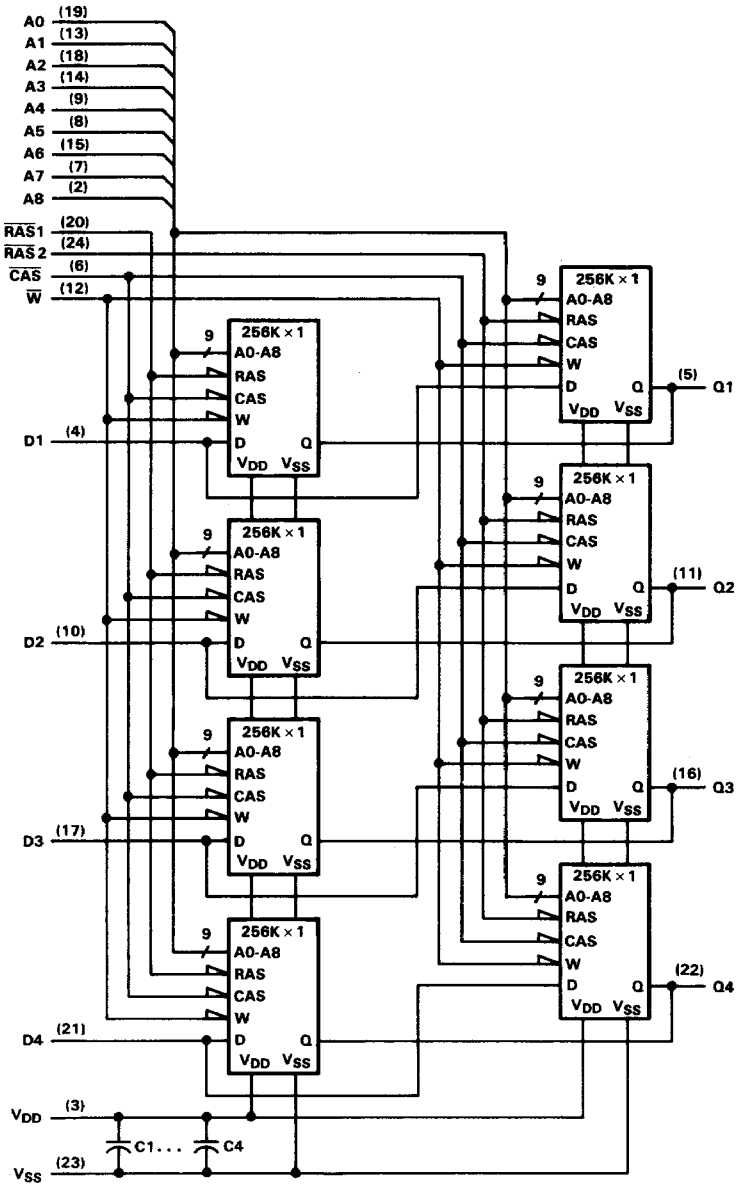
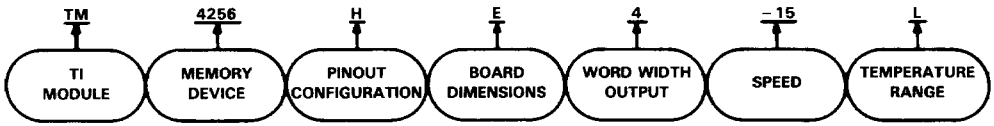
functional block diagram



TI single-in-line package nomenclature



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