ADE-XXX-XXX

HA11569FS
PIP Chroma H/V Signal Processing LSI (NTSC)

HITACHI

Rev. 2
Sep 1993

The HA11569FS is a main/sub Picture chroma and H/V signal processing LSI with built-in video switch for NTSC suited PIP systems. The HA11569FS implements on a single chip the PIP analog signal processing block which had previously been formed by three LSIs, the HA11525MP, the HA11532MP, and the HA118088NT. Furthermore, the HA11569FS has been designed to also handle Y and C inputs (S input).

A PIP system can be constructed from this IC and two other ICs (the HD49412 and the HM53461), that is, from a total of 3 ICs.

Functions

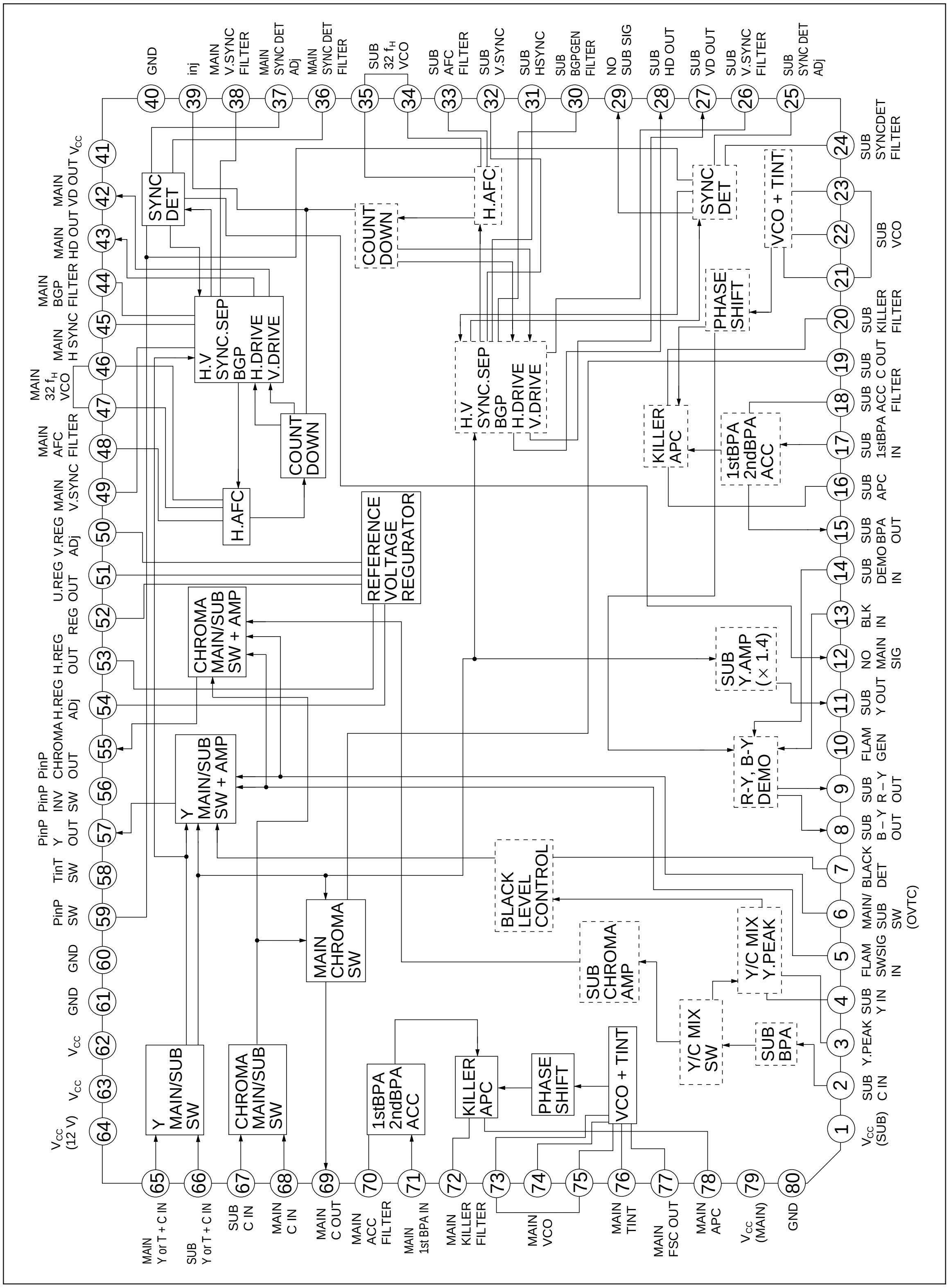
- Main and sub-picture chroma signal processing
- Main and sub-picture synch signal processing
- Built-in three function video switch

	Main input	Sub input	PIP output
1.	Y/C	Y/C	Y/C
2.	Y+C	Y+C	Y+C
3.	Y/C	Y+C	Y/C

Features

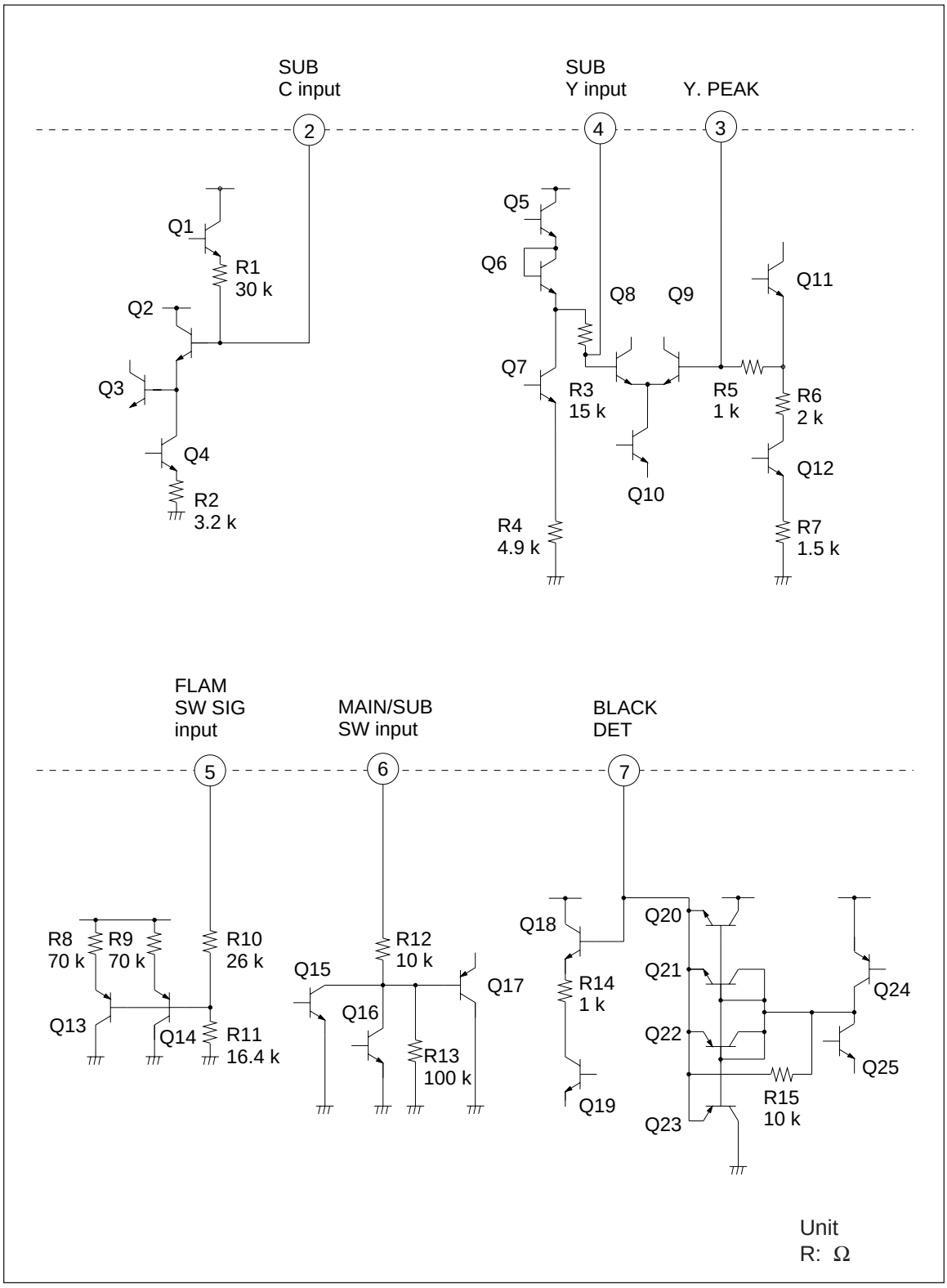
- An NTSC PIP system can be constructed from this and two other (the HD49412 and the HM53461) ICs.
- As compared with earlier PIP chip sets, a large reduction in the number of external components can be achieved.
- Can handle S inputs
- A black level compensation circuit is built into the sub-picture processing circuit, and such problems as black lifting are eliminated.
- A color signal level compensation circuit is built into the sub-picture processing circuit, and the sub-picture color signal level is always stable.

Block Diagram

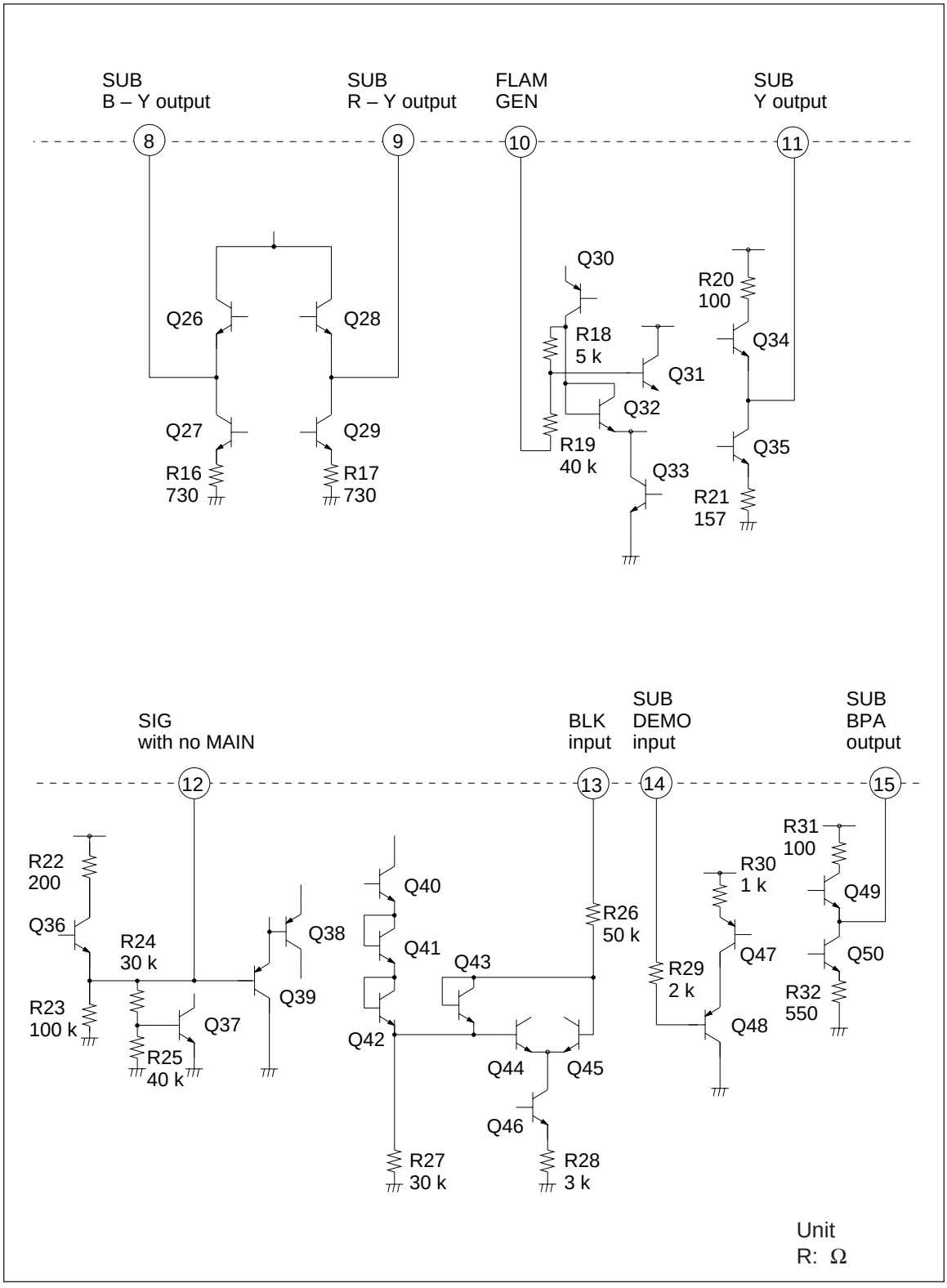


Home Print

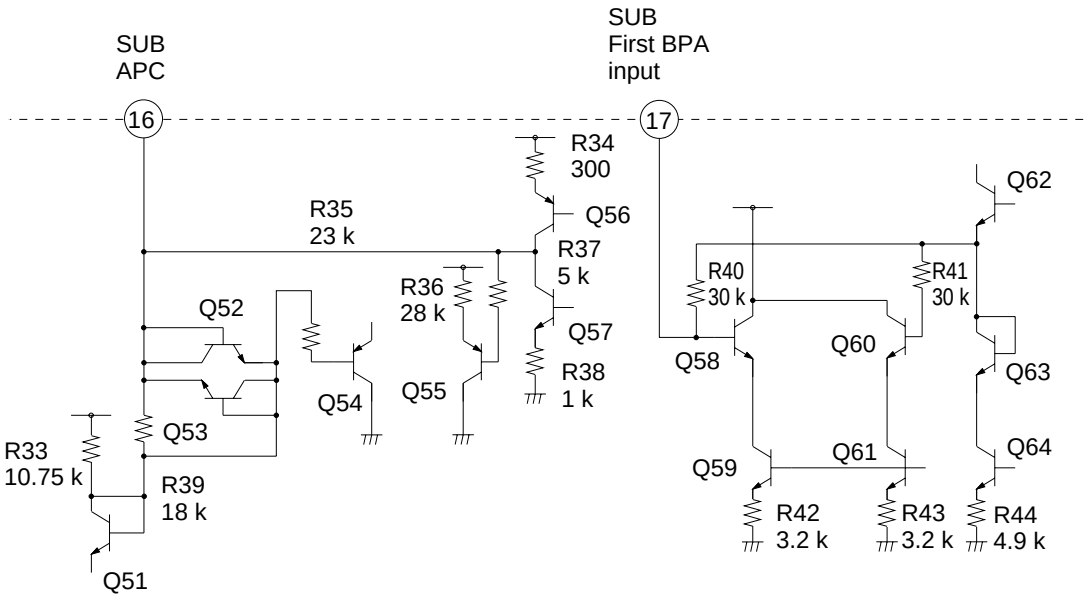
Interface

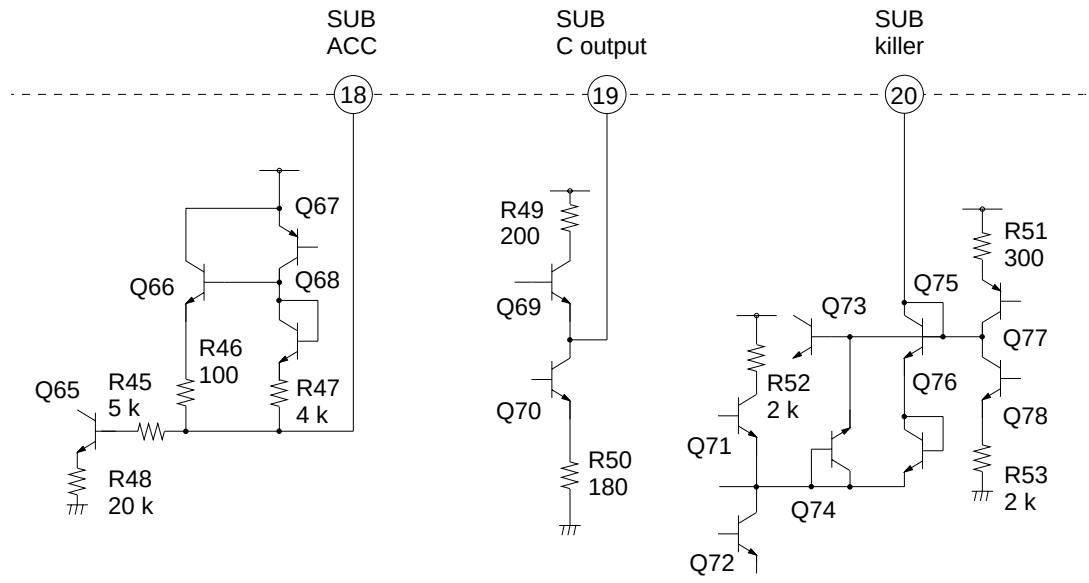

SUB
C input
SUB
Y input
Y. PEAK
2
4
3
Q1
R1
30 k
Q2
Q3
Q4
R2
3.2 k
Q5
Q6
Q8
Q9
Q11
Q7
R3
15 k
R5
1 k
R6
2 k
Q10
Q12
R4
4.9 k
R7
1.5 k
FLAM
SW SIG
input
MAIN/SUB
SW input
BLACK
DET
5
6
7
R8
70 k
R9
70 k
R10
26 k
Q13
Q14
R11
16.4 k
Q15
R12
10 k
Q17
Q16
R13
100 k
Q18
Q20
R14
1 k
Q21
Q24
Q22
Q25
R15
10 k
Q19
Q23
Unit
R: Ω

Interface (cont)

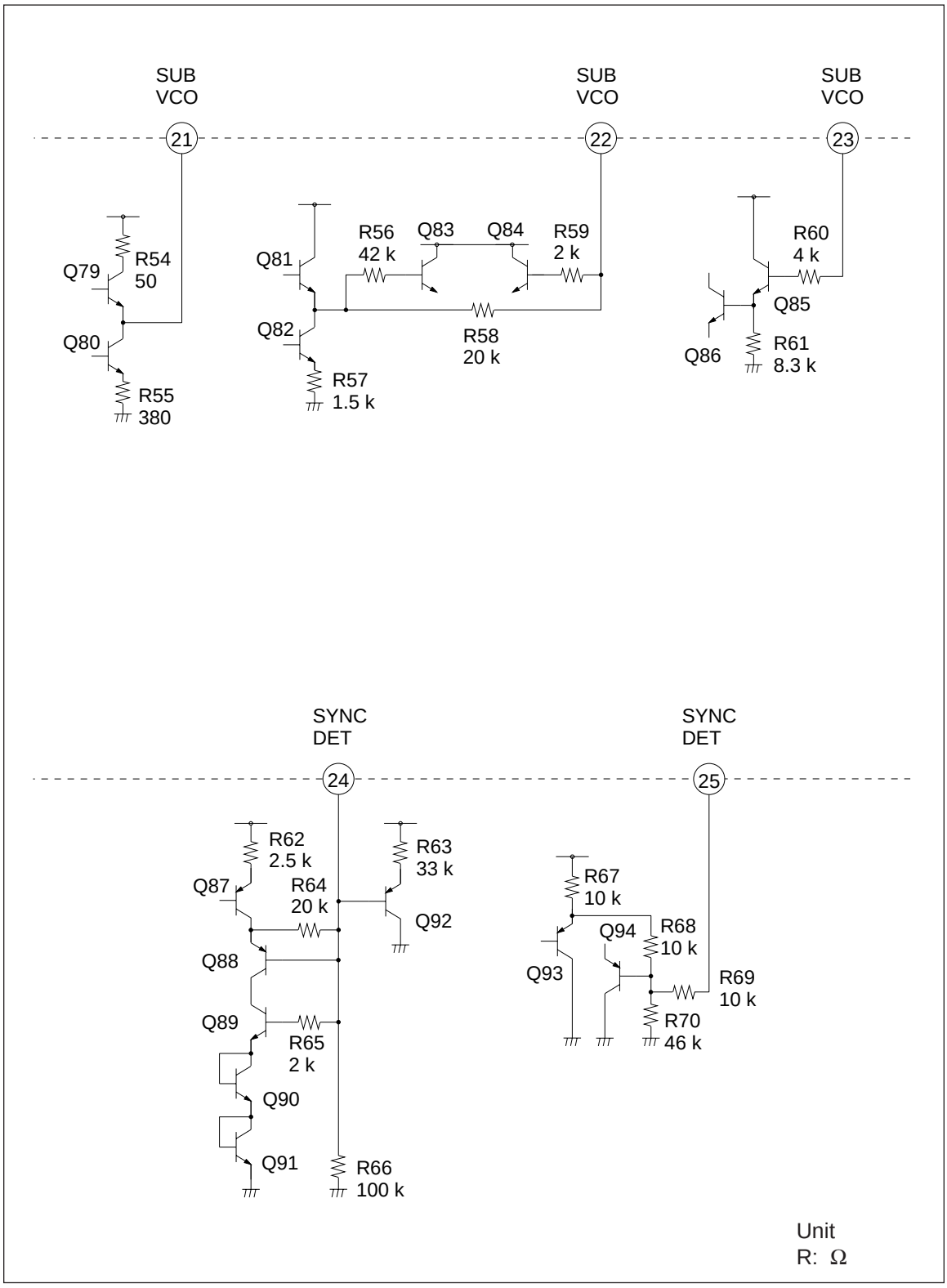


Interface (cont)

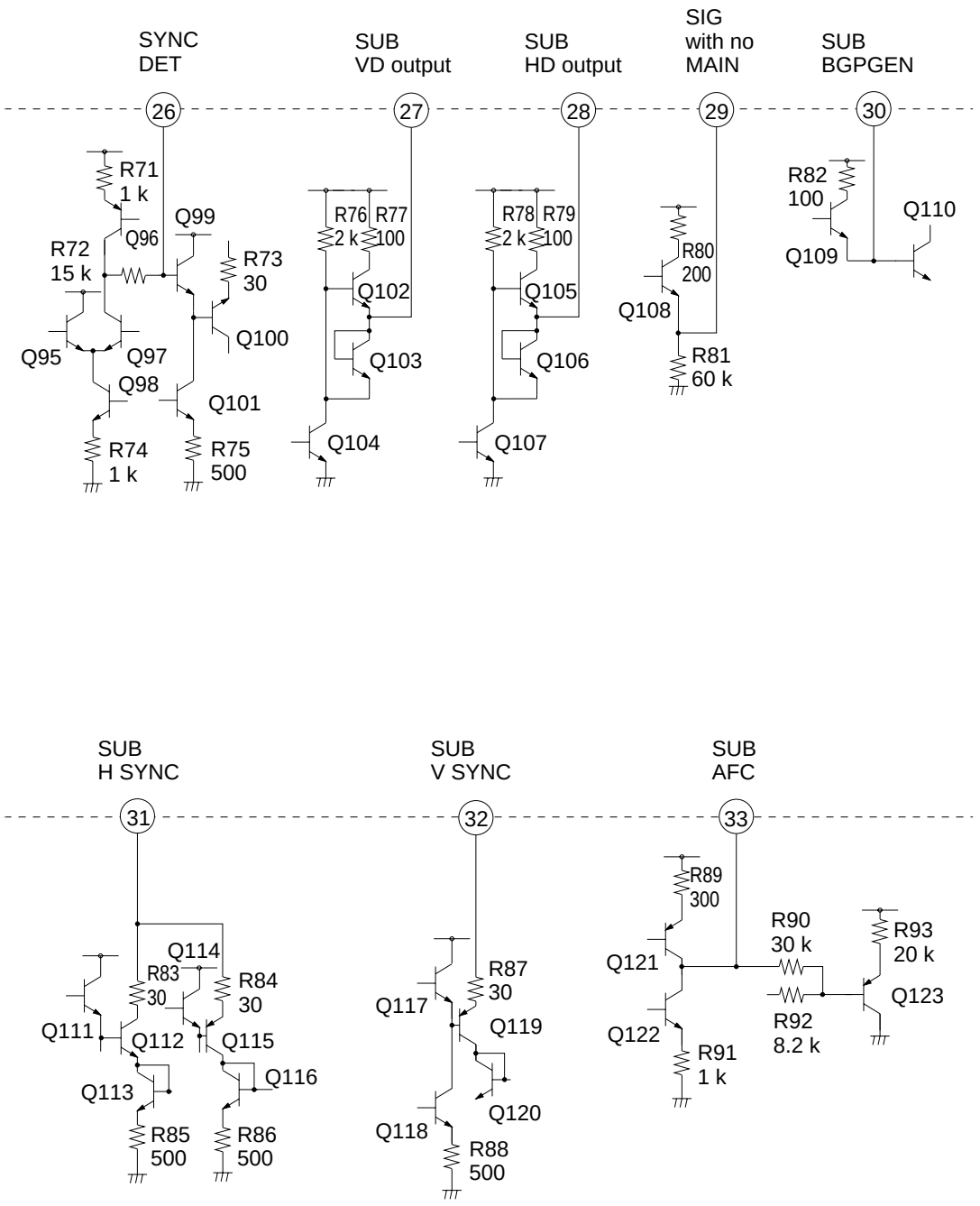




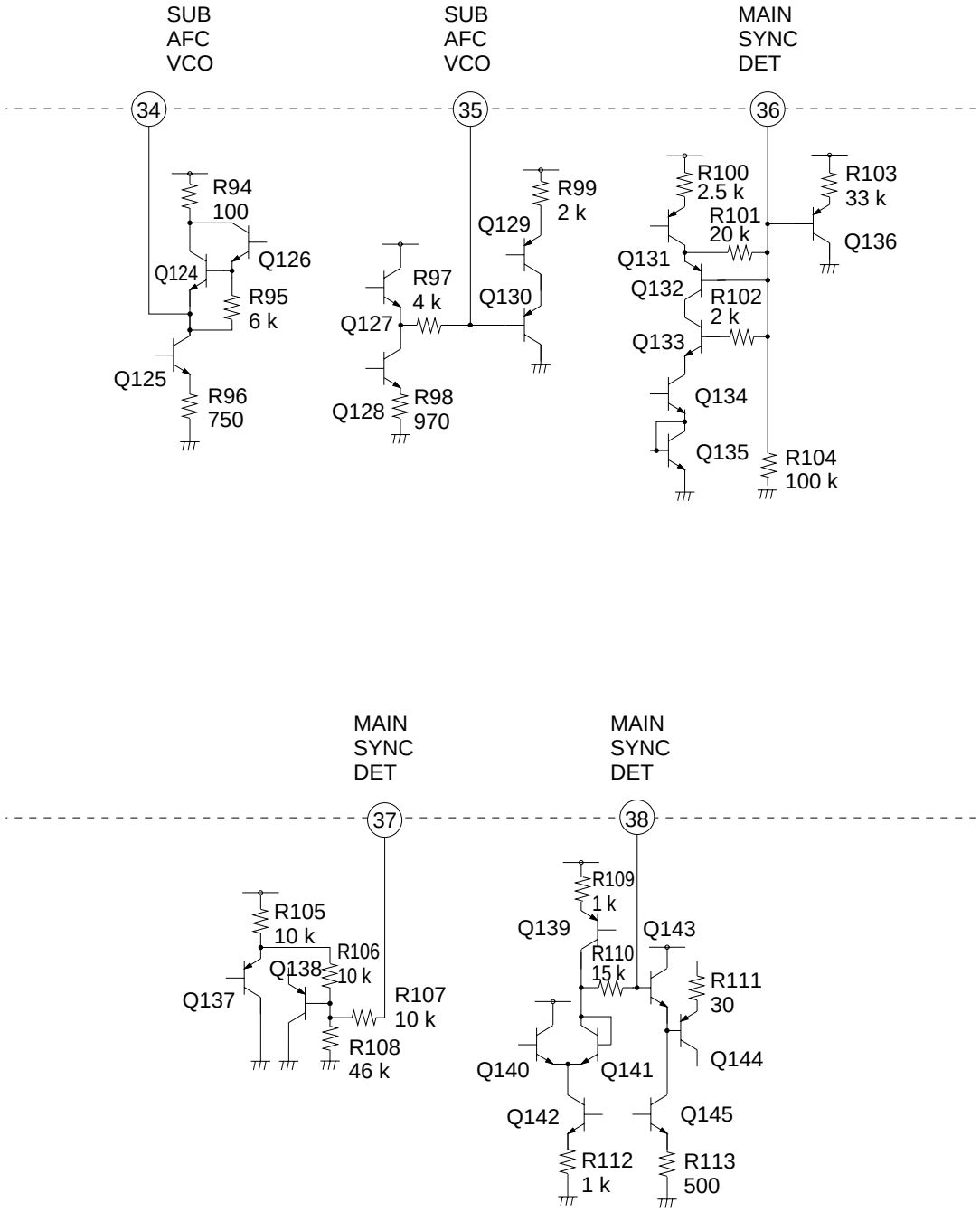
Interface (cont)



Interface (cont)



Interface (cont)



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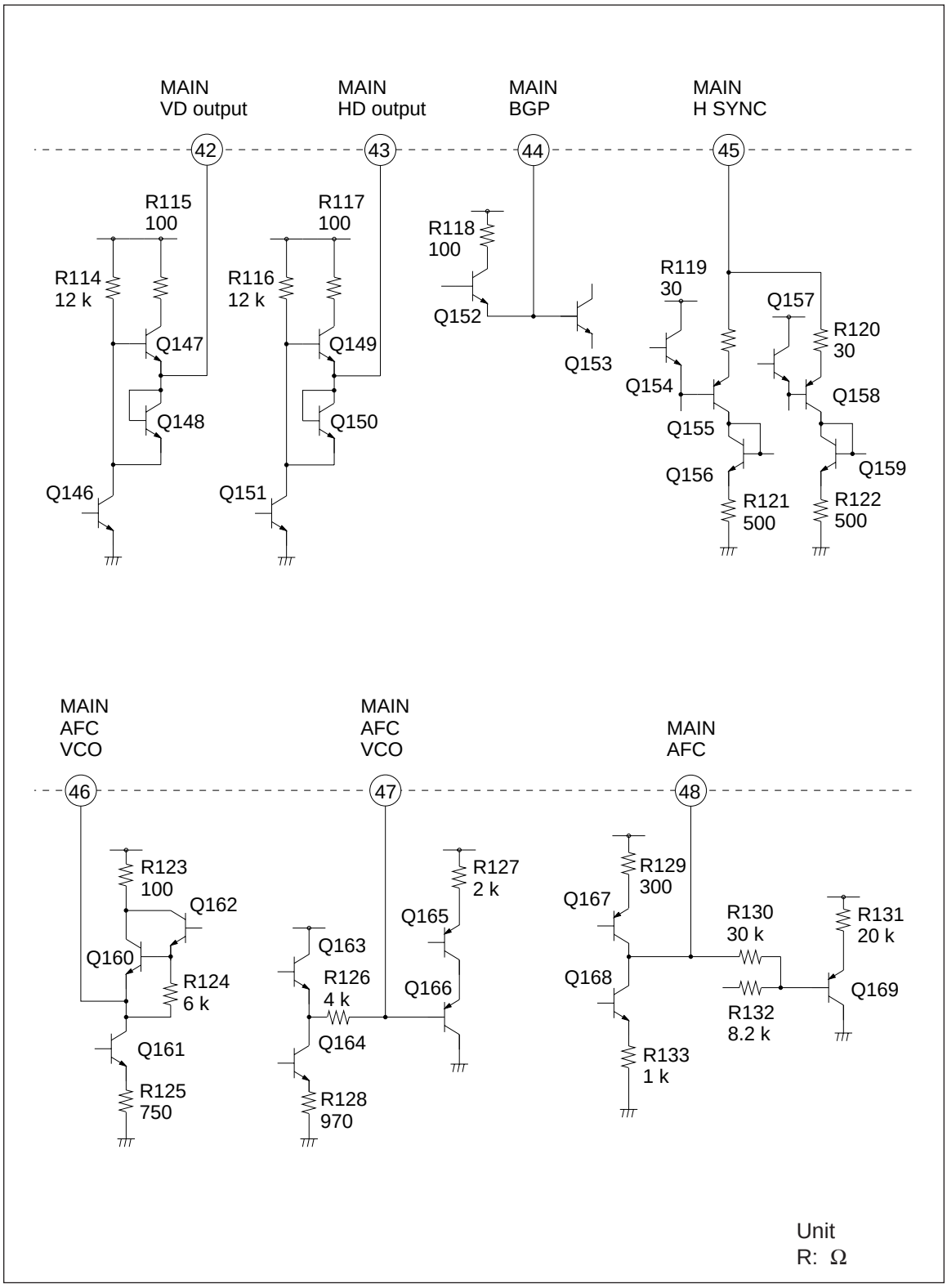

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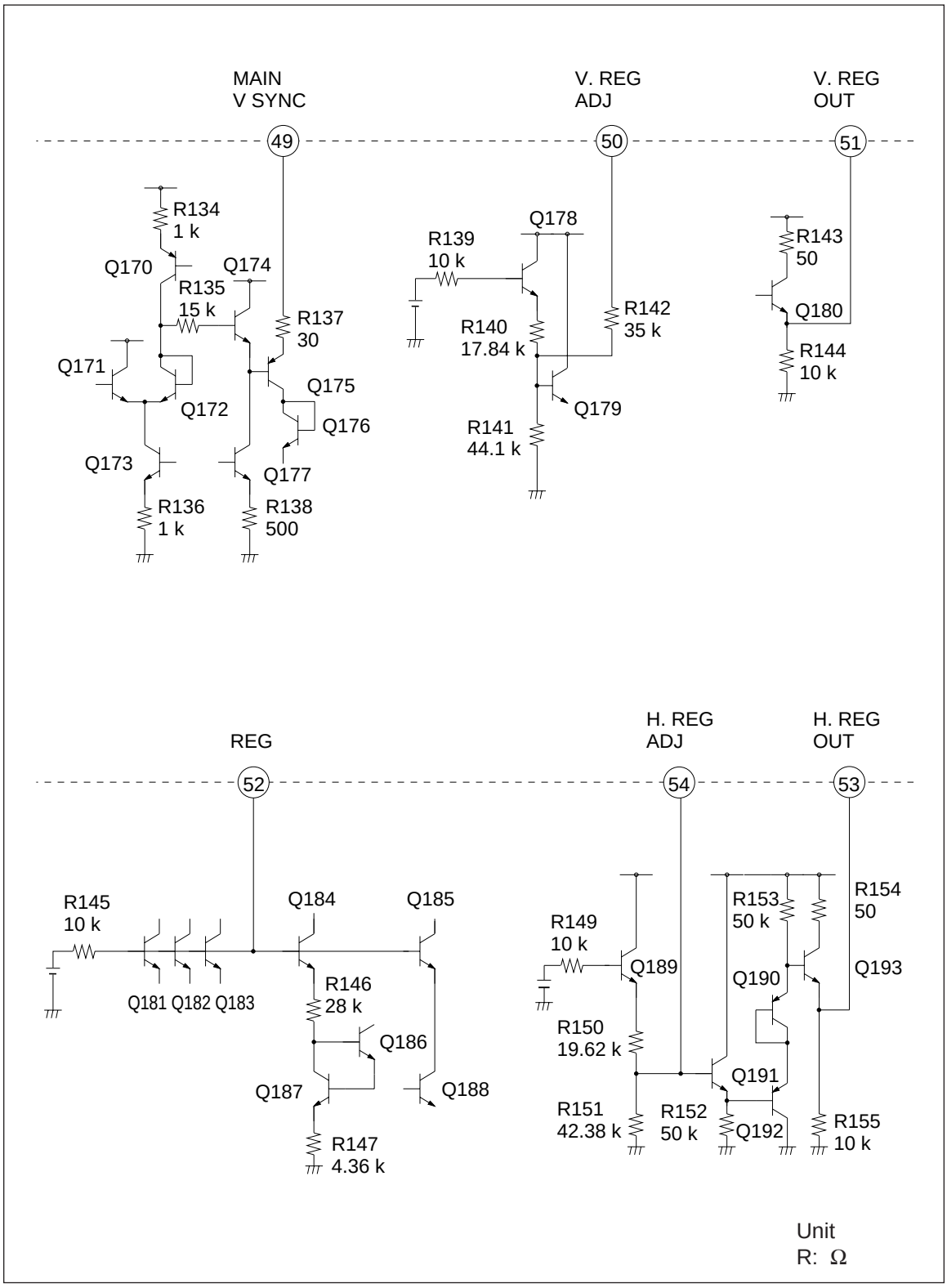

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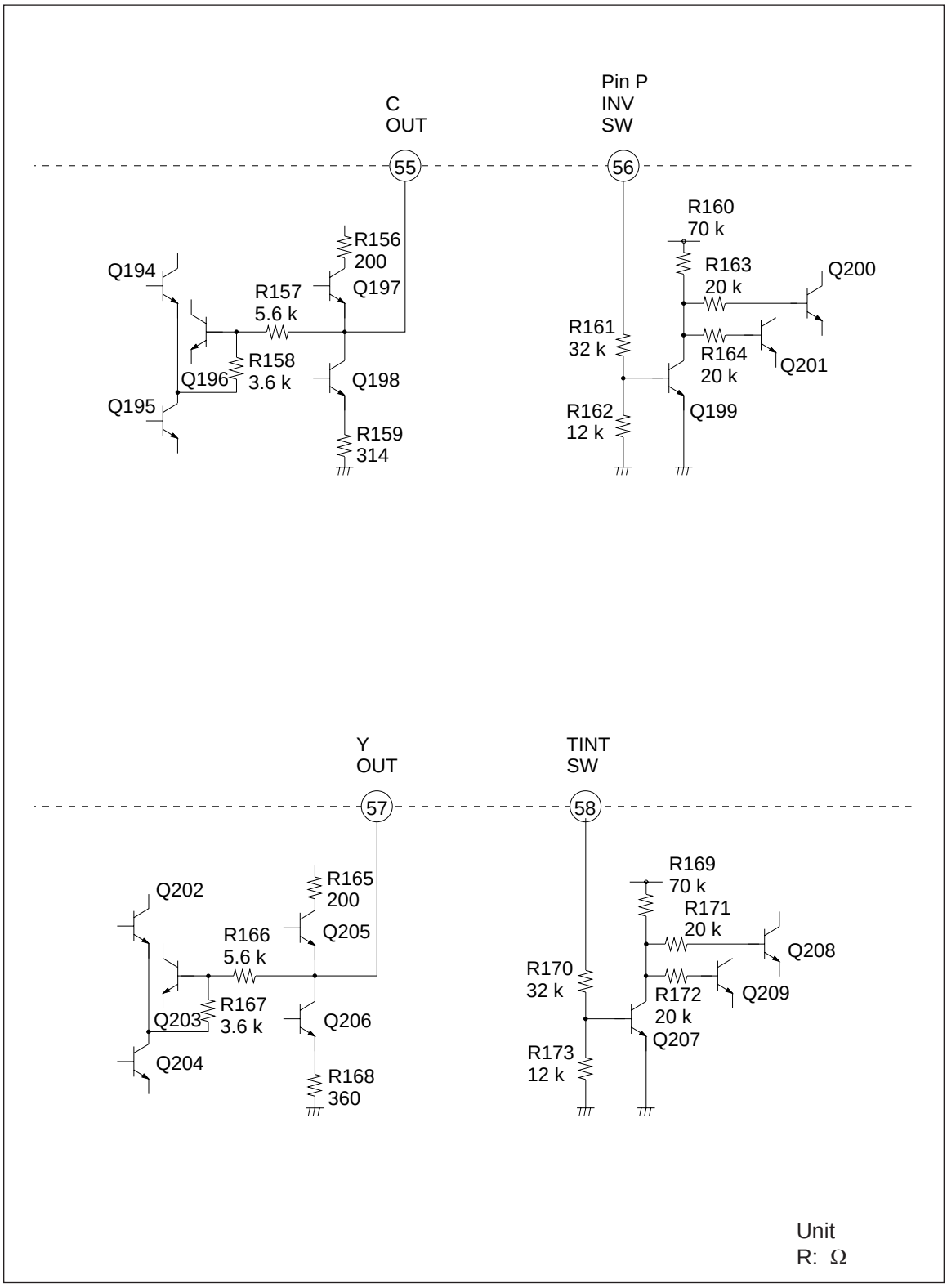

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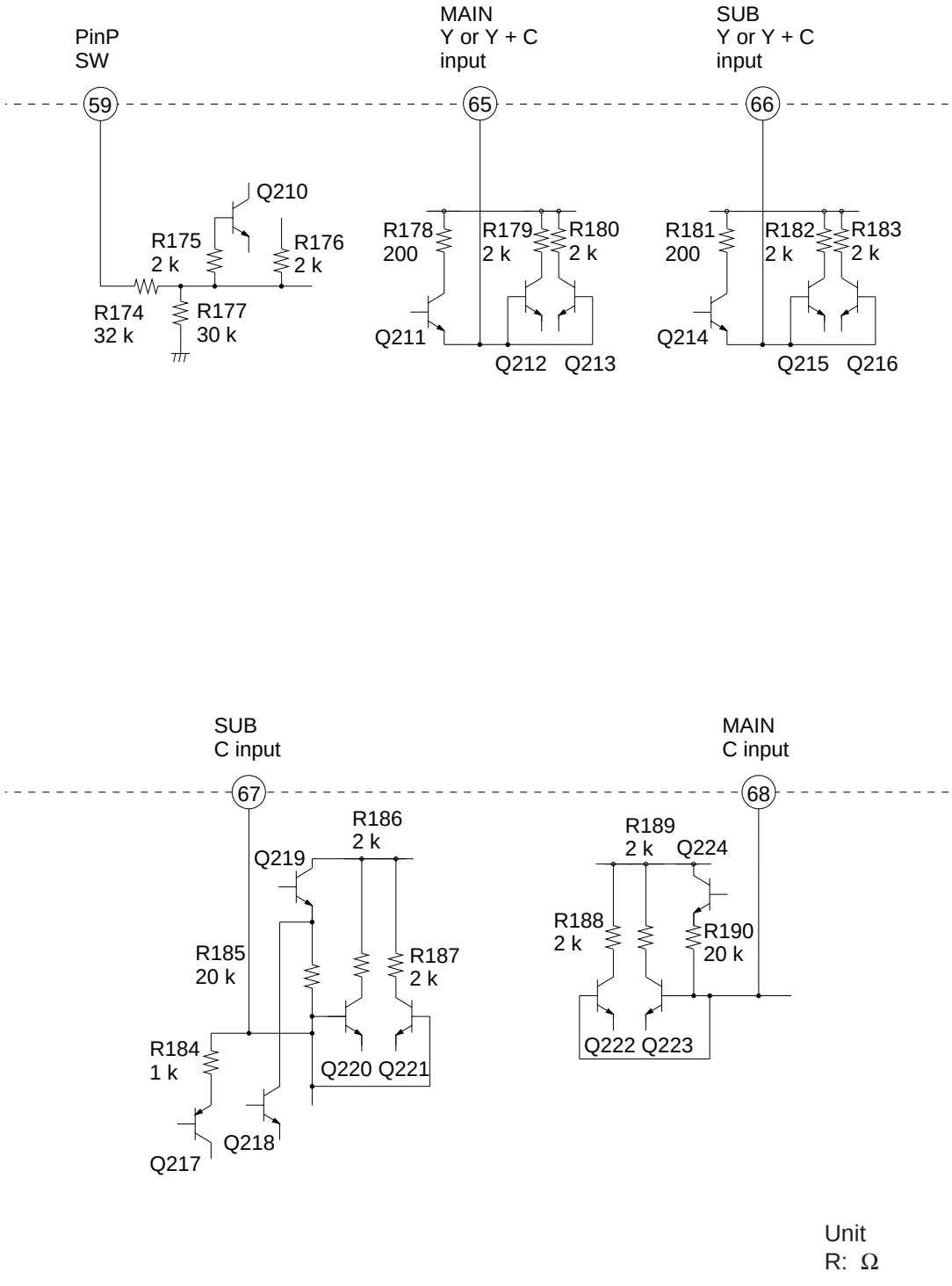
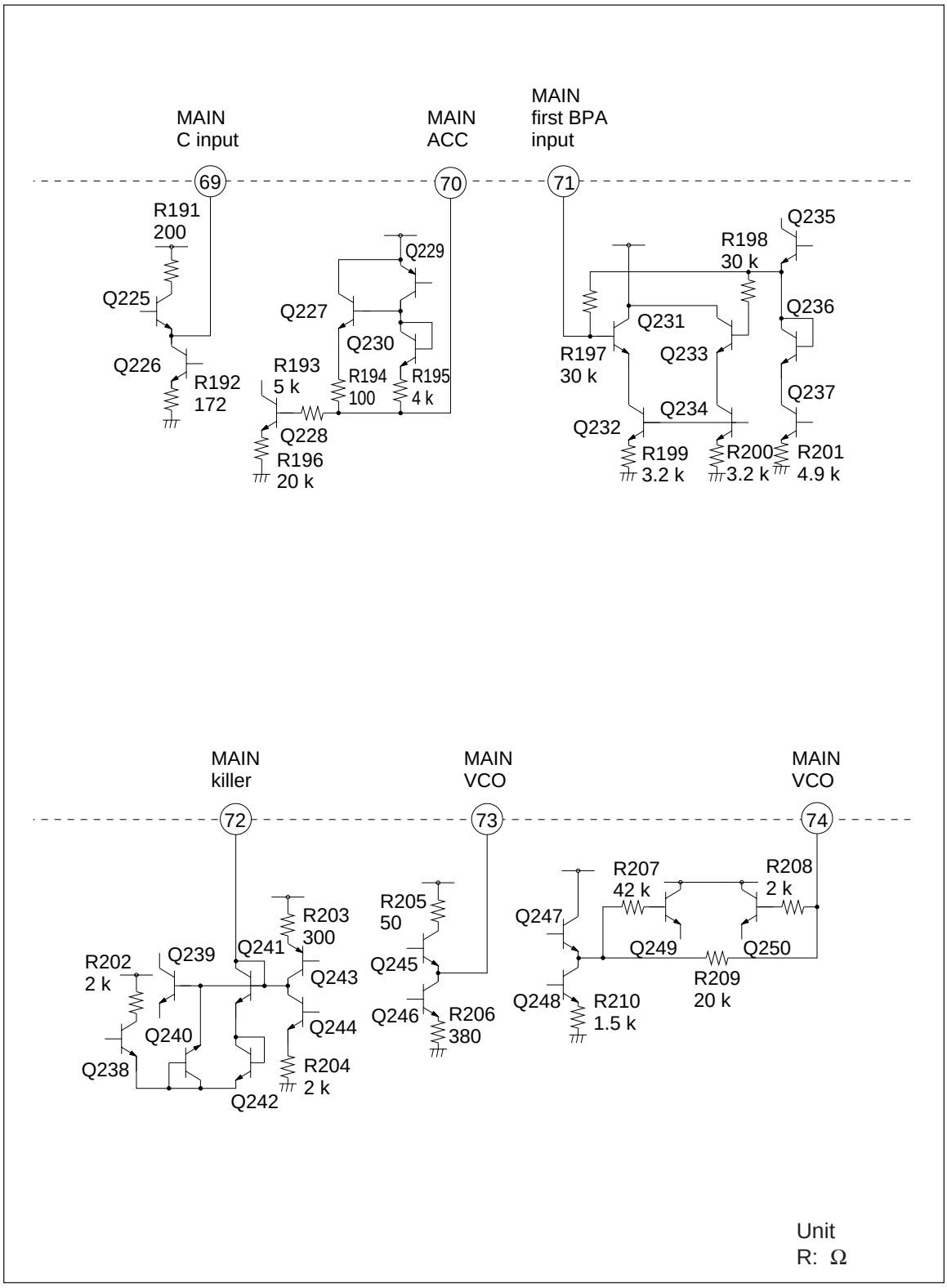
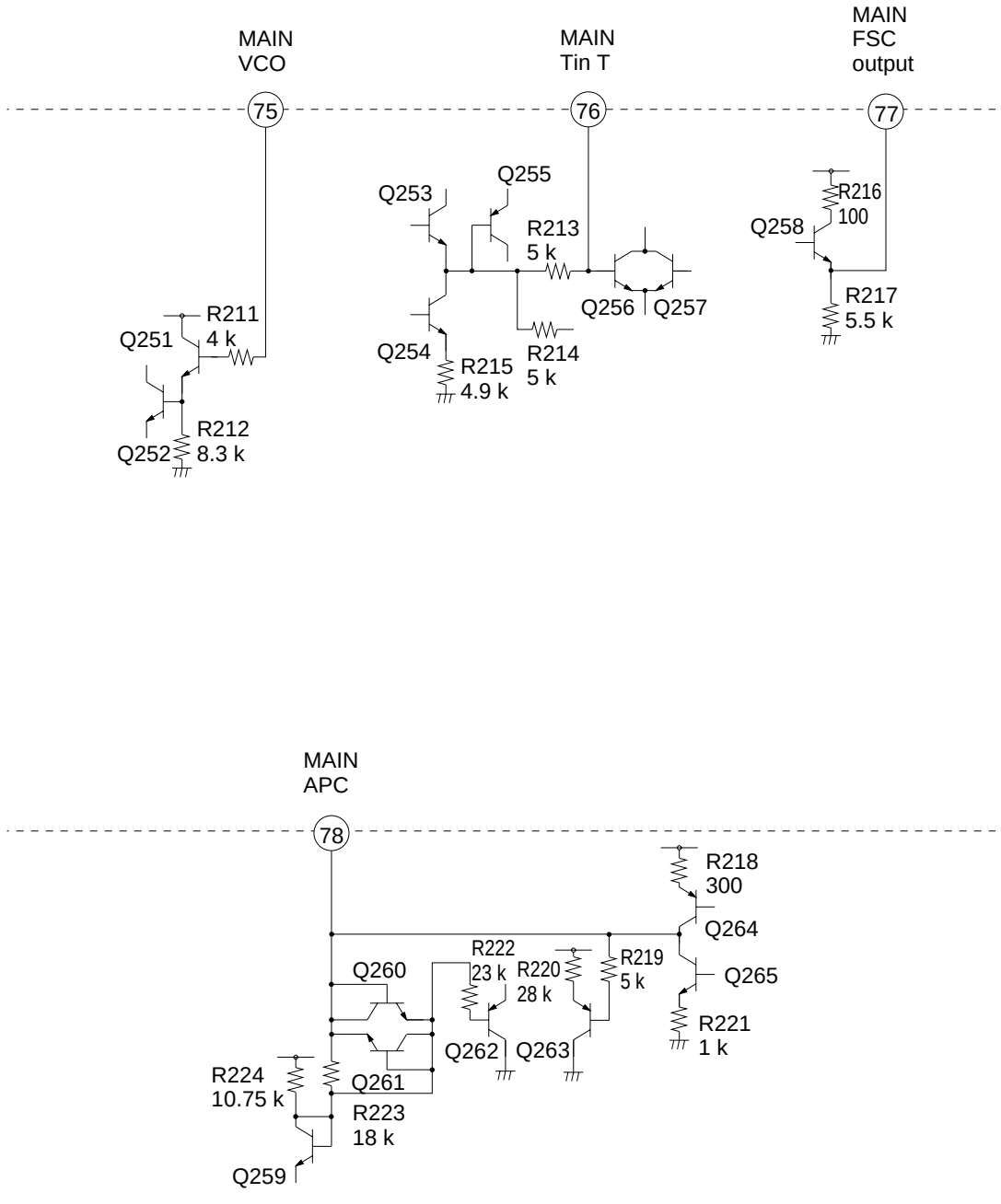


Interface (cont)



Interface (cont)



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Value	Units	Notes
Power supply voltage (5 V system)	$V_{CC1\ MAX}$	7	V	1
Power supply voltage (12 V system)	$V_{CC2\ MAX}$	15	V	2
Power dissipation	P_T	850	mW	
Storage temperature	Tstg	–40 to +150	°C	
Operating temperature	Topr	–10 to +75	°C	

Notes: 1. Operating power supply voltage range: 4.75 to 5.25 V

2. Operating power supply voltage range: 11 to 13 V

Electrical Characteristics (Ta = 25°C, V_{CC1} = 5 V, V_{CC2} = 12 V)

Item	Symbol	Min	Typ	Max	Units	Test Conditions	Application Terminal
Supply current 1	I_{CC1}	70	120	150	mA	5 V system	
Supply current 2	I_{CC2}	4	7.5	12	mA	12 V system	
I/O voltage gain (Y)	G_{YM}	7.0	8.0	9.0	dB	I/O DC gain	MAIN I/O (Y)
I/O voltage gain (C)	G_{CM}	6.7	8.0	9.3	dB	I/O gain at 3.58 MHz	MAIN I/O (C)
I/O frequency characteristics	f_{rio}	–1	0	1	dB	MAIN I/O 8 MHz	MAIN I/O (Y)
Differential gain	DG_M	—	1.0	3.0	%		MAIN I/O (Y)
Differential phase	DP_M	–3.0	1.0	3.0	deg.		MAIN I/O (Y)
FLAM internal setting level	E_{FLM}	1.58	1.7	1.82	V		MAIN I/O (Y)
Threshold voltage 1	E_{TH1}	1.5	2.5	3.5	V		OUTC, PinP WAKU
Threshold voltage 2	E_{TH2}	2.0	2.6	3.2	V		INV, TINT
Sub-image pedestal clamp level offset	epof	–25	0	25	mV	As compared with the main image (converted to 1 V_{PP})	YOUT
MAIN 1st BPA input DC voltage	EMBI (M)	2.75	2.85	2.95	V		
MAIN fsc output level	efsc (M)	200	600	—	mV_{PP}		
MAIN chroma VCO oscillator frequency offset	f_{SCO} (M)	–70	0	+70	Hz		
MAIN tint variation range	$\Delta\phi T$ (M)	75	85	—	deg		
SUB Y signal line gain	G_{YS}	12.3	13.8	15.3	dB		YOUT
SUB C signal line gain	G_{CS}	11.7	14.5	17.8	dB	fi = 3.58 MHz	COUT
MAIN horizontal free running frequency	f_{OH} (M)	15334	15734	16134	Hz		

Electrical Characteristics (Ta = 25°C, V_{CC1} = 5 V, V_{CC2} = 12 V) (cont)

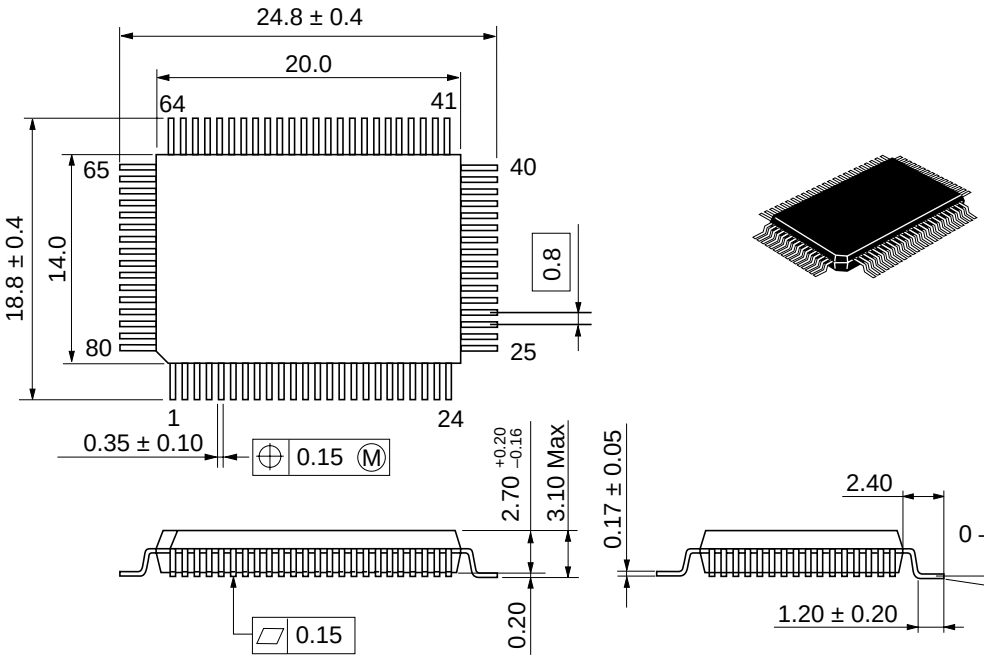
Item		Symbol	Min	Typ	Max	Units	Test Conditions	Application Terminal
MAIN HD pulse width		THD (M)	3.5	3.9	4.2	µs		
MAIN horizontal synchronization pull-in range	+	$f_{HP+ (M)}$	+400	+650	—	Hz		
MAIN horizontal synchronization pull-in range	–	$f_{HP– (M)}$	—	–900	–400	Hz		
MAIN vertical free running frequency		f_{OV} (M)	—	$\frac{fH}{288.5}$	—	Hz		
MAIN VD pulse width		$T_{VD (M)}$	—	10.25H	—	sec	Video input: open	
MAIN HD pulse output voltage (high)		$E_{HDH (M)}$	3.8	4.1	—	V		
MAIN HD pulse output voltage (low)		$E_{HDL (M)}$	—	0.9	1.2	V		
MAIN VD pulse output voltage (high)		$E_{VDH (M)}$	3.8	4.1	—	V		
MAIN VD pulse output voltage (low)		$E_{VDL (M)}$	—	0.9	1.2	V		
SUB 2nd BPA rated output		e_{MBO} (S)	330	380	430	mV_{PP}		
SUB ACC range	MAX	$\Delta G_{MAX (S)}$	–4	–2	+3	dB	Input burst level: –15 dB as compared to the eMBO level	
SUB ACC range	MIN	$\Delta G_{MIN (S)}$	–3	0.5	+3	dB	Input burst level: +6 dB as compared to the eMBO level	
SUB 1st BPA input DC voltage		$E_{MBI (S)}$	2.75	2.85	2.95	V		
SUB 2nd BPA output DC voltage		$E_{MBO (S)}$	2.1	2.4	2.7	V		
SUB Killer detection high level		$E_{KH (S)}$	3.4	3.8	4.3	V		
SUB APC control sensitivity		ßs	6	11	—	Hz/mV		
Demod (R – Y) gain		e_{DRO}	420	450	475	mV_{PP}		
Demod (B – Y) gain		e_{DBO}	420	450	475	mV_{PP}		
Demodulation output ratio (R – Y)/(B – Y)		$e\frac{R-Y}{B-Y}$	0.95	1.0	1.05	Multi-plicative factor		
(B – Y) demodulation angle		ϕ_{B-Y}	—	0	—	deg	Tint pin: open	
Color difference output residual upper harmonic level		ecar	—	0.03	0.15	V_{PP}	(B – Y) output = 1 V_{PP}	

Electrical Characteristics (Ta = 25°C, V_{CC1} = 5 V, V_{CC2} = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Units	Test Conditions	Application Terminal
Color difference output blanking residual upper harmonic level		e_{Bcar}	—	0.03	0.05	V_{PP}		
Demodulation angle			—	90	—	deg		
Demodulation output bandwidth		BW_{B-Y}	400	1500	—	kHz		
Color difference output DC voltage (R – Y)		E_{R-Y}	1.65	1.95	2.25	V		
Color difference output DC voltage (B – Y)		E_{B-Y}	1.65	1.95	2.25	V		
BLK threshold value level		E_{DBti}	1.2	2.1	2.7	V		
SUB horizontal free running frequency		$f_{OH\ (S)}$	15334	15734	16134	Hz		
SUB HD pulse width		$T_{HD\ (S)}$	3.5	3.9	4.2	µs		
SUB horizontal synchronization pull-in range	+	$f_{HP+\ (S)}$	+400	+650	—	Hz		
SUB horizontal synchronization pull-in range	–	$f_{HP-\ (S)}$	—	–900	–400	Hz		
SUB vertical free running frequency		$f_{OV\ (S)}$	—		—	Hz		
SUB VD pulse width		$T_{VD\ (S)}$	—	10.25 H	—	sec	Video input: open	
SUB HD pulse output voltage (high)		$E_{HDH\ (S)}$	3.8	4.1	—	V		
SUB HD pulse output voltage (low)		$E_{HDL\ (S)}$	—	0.9	1.2	V		
SUB VD pulse output voltage (high)		$E_{VDH\ (S)}$	3.8	4.1	—	V		
SUB VD pulse output voltage (low)		$E_{VDL\ (S)}$	—	0.9	1.2	V		

Package Dimensions

Unit: mm



Hitachi Code	FP-80B
JEDEC	——
EIAJ	SC-581-H