Advanced Information

General Description

In order to maintain its leading position Siemens is defining a new IC – the DOC – comprising all necessary functional blocks like switching, signaling, DTMF/tone handling and conferencing on a single chip. The transceivers (layer-1 ICs) are not integrated.

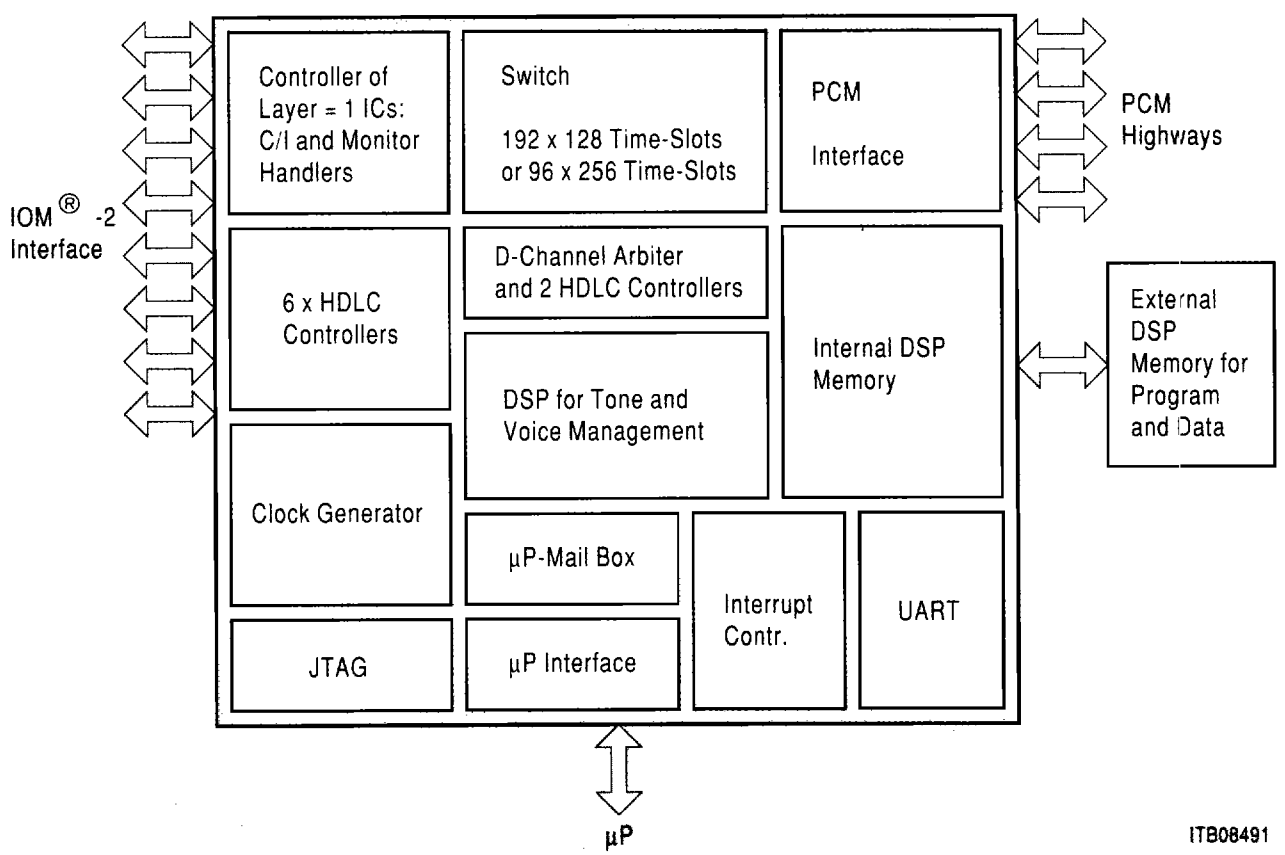
Features

The DOC provides all necessary features for building PBX (Private Branche eXchange) systems and Line Cards.

- In the PBX mode, the DOC provides:
  - 6 fully usable IOM-2 (GCI) interfaces and thus it can control up to 48 ISDN or 96 analog subscribers.
  - 4 PCM highways with 126 time-slots.
- In the Line Card mode, the DOC provides:
  - 2 fully usable IOM-2 interfaces with 16 IOM-2 subframes (2 × 8) and
  - 2 limited IOM-2 interfaces, as two DSP ports are connected, and thus it can control 16 to 24 ISDN (or 32 to 48 analog) subscribers.
  - 4 PCM highways with 256 time-slots.
- Signaling via 8 assignable HDLC controllers, each with a 64-byte data FIFO for transmit and for receive direction.
  - 2 HDLC controllers (SACCO-A) assignable of two of up to 48 ISDN subscribers at a time via two different D-channel arbiters.
  - 4 HDLC controllers (SIDEC) assignable to any D-/B-channel in data upstream or data downstream direction on four IOM-2 interfaces.
  - 2 HDLC controllers (SACCO-B) assignable to any time-slot in data upstream or data downstream direction on four IOM-2 interfaces or to PCM highway. Optionally, both controllers can be used as stand alone HDLC controllers with up to 8.192-Mbit/s transfer rate. They support DMA interface.

Type	Package
PEB 20560	P-MQFP-160-1 (SMD)

- On-chip user programmable 16-bit Digital Signal Processor, Siemens OAK, (with 20, 30 or up to 40 MIPS) with access to 64 time-slots (via one or two internal IOM-2 interfaces) for DTMF/tone generation and recognition, conferencing, music-on-hold, modem emulation, etc.
  - 1 K × 16-bit on-chip data memory (X)
  - 512 × 16-bit on-chip data memory (Y)
  - DSP proprietary interface to an external memory:
    Program memory up to 62 K × 16 bit
    Data memory up to 32 K × 16 bit
  - On-chip program memory (Boot)
- a-/µ-Law coding and decoding by hardware (on the fly)
- Firmware for DSP load measurement (within every 125-µs frame)
- µP-DSP communication via a µP-Mail-Box
- On-chip emulation (OCEM) for DSP program debugging
- 8-bit µP interface compatible with Siemens/Intel/Motorola bus schemes
- Programmable clock generator with built-in logic for master and slave configurations
- Watch-dog timer
- Reset logic
- UART for V.24 interface
- Multifunctional input/ouput port configurable as a general I/O port, DMA lines for one SACCO or as additional UART lines for modem connection
- Integrated interrupt controller with vector generation and support for DOC cascading
- JTAG interface for on board tests
- Interface for HW and SW evaluation (debugging)
- Advanced CMOS 0.6-µm technology
- 3.3 and 5-V power supply
- TTL driving capability, TTL and CMOS compatible inputs
- P-MQFP-160 package


Controller of Layer = 1 ICs: C/I and Monitor Handlers
Switch
192 x 128 Time-Slots or 96 x 256 Time-Slots
PCM
Interface
PCM Highways
IOM® -2 Interface
6 x HDLC Controllers
D-Channel Arbiter and 2 HDLC Controllers
Internal DSP Memory
External DSP Memory for Program and Data
DSP for Tone and Voice Management
Clock Generator
µP-Mail Box
Interrupt Contr.
UART
JTAG
µP Interface
µP
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