

512K x 72 Synchronous Pipeline Burst ZBL SRAM

FEATURES

- Fast clock speed: 150, 133, and 100MHz
- Fast access times: 3.8ns, 4.2ns, and 5.0ns
- Fast OE# access times: 3.8ns, 4.2ns, and 5.0ns
- High performance 3-1-1-1 access rate
- 3.3V ± 5% power supply
- I/O supply voltage 3.3V or 2.5V
- Common data inputs and data outputs
- Byte write enable and global write control
- Six chip enables for depth expansion and address pipeline
- Internally self-timed write cycle
- Burst control pin (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- Commercial, industrial and military temperature ranges
- Packaging:
 - 152 PBGA package 17 x 23mm

BENEFITS

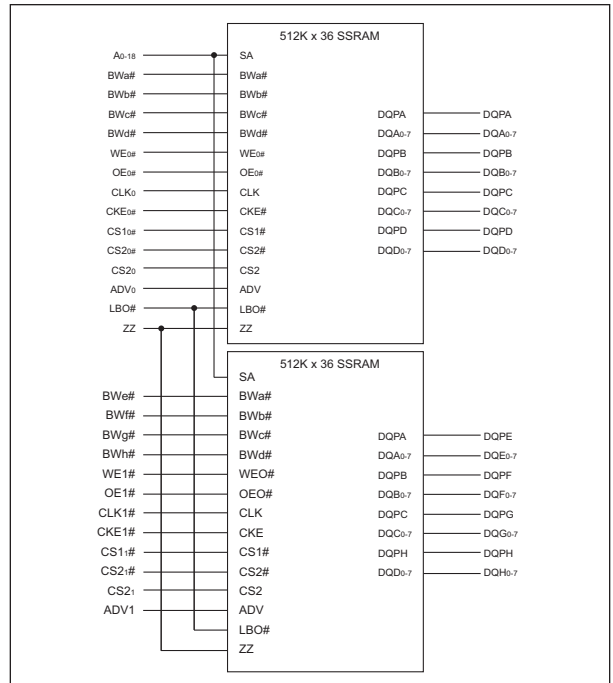
- 30% space savings compared to equivalent TQFP solution
- Reduced part count
- 24% I/O reduction
- Laminate interposer for optimum TCE match
- Low Profile
- Reduce layer count for board routing
- Suitable for hi-reliability applications
- User configurable as 1M x 36 or 2M x 18
- Upgradable to 1M x 72 (contact factory for availability)

DESCRIPTION

The WEDC SyncBurst - SRAM employs high-speed, low-power CMOS design that is fabricated using an advanced CMOS process. WEDC's 32Mb SyncBurst SRAMs integrate two 512K x 36 SSRAMs into a single BGA package to provide 512K x 72 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The ZBL or Zero Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Asynchronous inputs include the sleep mode enable (ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

* Product is subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|----------|--------------------|--------------------|-------------------|------------------|------------------|-------------------|------------------|------------------|------------------|
| A | - | ADV ₀ | OE ₀ # | DQb ₂ | DQb ₄ | DQb ₆ | dnu | DQa ₆ | DQa ₂ |
| B | CKE ₀ # | WE ₀ # | DQb ₇ | DQb ₅ | DQb ₃ | DQb ₀ | DQa ₇ | DQa ₃ | DQa ₁ |
| C | CLK ₀ | CS ₂₀ # | DQc ₂ | DQpc | DQpb | DQb ₁ | DQd ₇ | DQa ₄ | DQa ₀ |
| D | BWa# | BWb# | DQC ₃ | V _{SS} | V _{SS} | V _{SS} | DQD ₆ | DQA ₅ | DQPA |
| E | BWc# | BWd# | DQC ₄ | V _{CCQ} | V _{CCQ} | V _{CCQ} | DQD ₅ | DQPD | ZZ |
| F | CS ₁₀ # | CS ₂₀ | DQC ₅ | V _{CCQ} | V _{CCQ} | V _{SS} | DQD ₄ | DNU* | A ₀ |
| G | A ₇ | DQC ₀ | DQC ₇ | V _{SS} | V _{CC} | V _{CC} | DQD ₃ | A ₁ | A ₃ |
| H | A ₁₈ | DQC ₁ | DQC ₆ | V _{CC} | V _{CC} | V _{CC} ' | DQD ₂ | A ₂ | A ₅ |
| J | A ₉ | A ₆ | DQF ₂ | V _{SS} | V _{SS} | V _{SS} | DQD ₁ | A ₄ | A ₁₆ |
| K | A ₈ | DQF ₄ | FQF ₃ | V _{CC} | V _{CC} | V _{CC} | DQD ₀ | A ₁₄ | A ₁₅ |
| L | A ₁₇ | DQF ₅ | DQF ₆ | V _{CC} | V _{CC} | V _{SS} | DQE ₆ | A ₁₂ | A ₁₃ |
| M | ADV ₁ | OE ₁ # | DQF ₇ | V _{SS} | V _{CCQ} | V _{CCQ} | DQE ₇ | A ₁₀ | A ₁₁ |
| N | CKE ₁ # | WE ₁ # | DQPF | V _{CCQ} | V _{CCQ} | V _{CCQ} | DQE ₅ | DQE ₃ | LBO# |
| P | CLK ₁ | CS ₂₁ # | DQF ₁ | V _{SS} | V _{SS} | V _{SS} | DQE ₄ | DQE ₂ | DQE ₀ |
| R | BWe# | BWf# | DQF ₀ | DQG ₁ | DQG ₄ | DQH ₁ | DQH ₂ | DQE ₁ | DQPE |
| T | BWg# | BWh# | DQG ₀ | DQG ₂ | DQG ₅ | DQH ₀ | DQH ₄ | DQH ₇ | DQPH |
| U | CS ₁₁ # | CS ₂₁ | DQG ₃ | DQPG | DQG ₆ | DQG ₇ | DQH ₃ | DQH ₅ | DQH ₆ |

NOTE: DNU means Do Not Use and are reserved for future use.

* Pin F₈ reserved for A₁₉ upgrade to 1M x 72



FUNCTION DESCRIPTION

The WEDPZ512K72V-XBX is an ZBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of OE#, LBO# and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable (CKE#) pin allows the operation of the chip to be suspended as long as necessary. When CKE# is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when CKE and ADV are driven low at the rising edge of the clock.

Output Enable (OE#) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE# is driven low, the write enable input signals WE# are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation OE# must be driven low for the device to drive out the requested data.

Write operation occurs when WE# is driven low at the rising edge of the clock. BW#[h:a] can be used for byte write operation. The pipe-lined ZBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, WE# and address are registered, and the data associated with that address is required two cycles later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after two cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after two cycles of wake up time.

BURST SEQUENCE TABLE

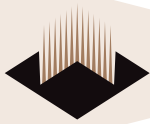
(Interleaved Burst, LBO# = High)

| LBO# Pin | High | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|--------------------------------------|------|--------|----|--------|----|--------|----|--------|----|
| | | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address ↓ Fourth Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

(Linear Burst, LBO# = Low)

| LBO# Pin | High | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|--------------------------------------|------|--------|----|--------|----|--------|----|--------|----|
| | | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address ↓ Fourth Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

NOTE 1: LBO pin must be tied to High or Low, and Floating State must not be allowed.



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

| CEx# | ADV | WE# | BWx# | OE# | CKE# | CLK | Address Accessed | Operation |
|------|-----|-----|------|-----|------|-----|------------------|----------------------------|
| H | L | X | X | X | L | - | N/A | Deselect |
| X | H | X | X | X | L | - | N/A | Continue Deselect |
| L | L | H | X | L | L | - | External Address | Begin Burst Read Cycle |
| X | H | X | X | L | L | - | Next Address | Continue Burst Read Cycle |
| L | L | H | X | H | L | - | External Address | NOP/Dummy Read |
| X | H | X | X | H | L | - | Next Address | Dummy Read |
| L | L | L | L | X | L | - | External Address | Begin Burst Write Cycle |
| X | H | X | L | X | L | - | Next Address | Continue Burst Write Cycle |
| L | L | L | H | X | L | - | N/A | NOP/Write Abort |
| X | H | X | H | X | L | - | Next Address | Write Abort |
| X | X | X | X | X | H | - | Current Address | Ignore Clock |

NOTES:

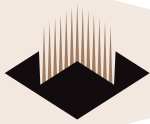
1. X means "Don't Care."
2. The rising edge of clock is symbolized by (-).
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. WRITE# = L means Write operation in WRITE TRUTH TABLE.
WRITE# = H means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins (ZZ and OE).
6. CEx# refers to the combination of CS1#, CS2 and CS2#.

WRITE TRUTH TABLE

| WE# | BWa# | BWb# | BWc# | BWd# | Operation |
|-----|------|------|------|------|-----------------|
| H | X | X | X | X | Read |
| L | L | H | H | H | Write Byte a |
| L | H | L | H | H | Write Byte b |
| L | H | H | L | H | Write Byte c |
| L | H | H | H | L | Write Byte d |
| L | L | L | L | L | Write All Bytes |
| L | H | H | H | H | Write Abort/NOP |

NOTES:

1. X means "Don't Care."
2. All inputs in this table must meet setup and hold time around the rising edge of CLK (-).
3. Replace BWa# with WE#, BWb#, with BWf#, BWc# with BWg# and BWd# with BWn# for operation of IC2.



ABSOLUTE MAXIMUM RATINGS*

| | |
|--|-----------------|
| V _{IN} Voltage or any other pin relative to V _{SS} | -0.3V to +4.6V |
| Voltage on V _{CC} Supply Relative to V _{SS} | -0.3V to +4.6V |
| Storage Temperature (BGA) | -55°C to +150°C |
| Maximum Operating Junction Temperature | 125°C |

* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

-55°C ≤ T_A ≤ +125°C

| Description | Symbol | Conditions | Min | Max | Units | Notes | |
|------------------------------|------------------|--|----------|-------|----------------------|-------|---|
| Input High (Logic 1) Voltage | V _{IH} | | 3.3V I/O | 2.0 | V _{CC} +0.3 | V | 1 |
| | | | 2.5V I/O | 1.7 | V _{CC} +0.3 | | |
| Input Low (Logic 0) Voltage | V _{IL} | | 3.3V I/O | -0.3 | 0.8 | V | 1 |
| | | | 2.5V I/O | -0.3 | 0.7 | | |
| Input Leakage Current | I _{IL} | V _{CC} = Max, 0V ≤ V _{IN} ≤ V _{CC} | -10 | +10 | μA | 2 | |
| Output Leakage Current | I _{OL} | Output(s) Disabled, V _{OUT} = V _{SS} to V _{CCQ} | -5 | +5 | μA | | |
| Output High Voltage | V _{OH} | I _{OH} = -2.0mA (3.3V I/O) | 2.4 | — | V | 1 | |
| | | I _{OH} = -1mA (2.5V I/O) | 2.0 | — | V | | |
| Output Low Voltage | V _{OL} | I _{OL} = 6.0mA (3.3V I/O) | — | 0.4 | V | 1 | |
| | | I _{OL} = 1.0 mA (2.5V I/O) | — | 0.4 | V | | |
| Supply Voltage | V _{CC} | | 3.135 | 3.465 | V | 1 | |
| I/O Power Supply (3.3V) | V _{CCQ} | | 3.135 | 3.465 | V | 1 | |
| I/O Power Supply (2.5V) | V _{CCQ} | | 2.375 | 2.9 | V | 1 | |

NOTES:

- All voltages referenced to V_{SS} (GND)
- LBO# pin has an internal pull-up, and input leakage = ± 200 μA.

DC CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C

| Description | Symbol | Conditions | 150 MHz (Max) | 133 MHz (Max) | 100 MHz (Max) | Units | Notes |
|---------------------------------|------------------|---|---------------|---------------|---------------|-------|-------|
| Power Supply Current: Operating | I _{DD} | Device Selected; All Inputs ≤ V _{IL} or ≥ V _{IH} ; Cycle Time ≥ TCYC MIN; V _{CC} = MAX; Output Open | 700 | 650 | 600 | mA | 1 |
| Power Supply Current: Standby | I _{SB2} | Device Deselected; V _{CC} = MAX; All Inputs ≤ V _{IL} or ≥ V _{IH} All Inputs Static; CLK Frequency = MAX Output Open, ZZ ≥ V _{CC} - 0.2V | 300 | 300 | 300 | mA | |
| Clock Running Standby Current | I _{SB} | Device Deselected; V _{CC} = MAX; All Inputs ≤ V _{SS} + 0.2 or ≥ V _{CC} - 0.2; f = max; ZZ ≤ V _{IL} | 400 | 400 | 400 | mA | |

NOTES:

- I_{DD} is specified with no output current and increases with faster cycle times.
I_{DD} increases with faster cycle times and greater output loading.

BGA CAPACITANCE

T_A = +25°C, f = 1MHz

| Description | Symbol | Max | Units | Notes |
|--------------------------------------|-----------------|-----|-------|-------|
| Control Input Capacitance (LBO#, zz) | C _{IC} | 16 | pF | 1 |
| Control Input Capacitance | C _I | 8 | pF | 1 |
| Input/Output Capacitance (DQ) | C _O | 10 | pF | 1 |
| Address Capacitance | C _A | 16 | pF | 1 |
| Clock Capacitance | C _{CK} | 6 | pF | 1 |

NOTES: 1. This parameter is not tested but guaranteed by design.

THERMAL RESISTANCE

| Parameter | Symbol | Max | Unit |
|---|-----------------|-----|------|
| Thermal Resistance: Die Junction to Ambient | θ _{JA} | TBD | °C/W |
| Thermal Resistance: Die Junction to Ball | θ _{JB} | TBD | °C/W |
| Thermal Resistance: Die Junction to Case | θ _{JC} | TBD | °C/W |

Note: Refer to Application Note "PBGA Thermal Resistance Correlation" for further information regarding WEDC's thermal modeling.



AC CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | 150MHz | | 133MHz | | 100MHz | | Units |
|-------------------------------------|-------------------|--------|-----|--------|-----|--------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Clock Time | t _{cy} | 6.7 | — | 7.5 | — | 10.0 | — | ns |
| Clock Access Time | t _{cd} | — | 3.8 | — | 4.2 | — | 5.0 | ns |
| Output enable to Data Valid | t _{oe} | — | 3.8 | — | 4.2 | — | 5.0 | ns |
| Clock High to Output Low-Z | t _{lzc} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Output Hold from Clock High | t _{oh} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Output Enable Low to output Low-Z | t _{lzoE} | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| Output Enable High to Output High-Z | t _{hzoE} | — | 3.0 | — | 3.5 | — | 3.5 | ns |
| Clock High to Output High-Z | t _{hzc} | — | 3.0 | — | 3.5 | — | 3.5 | ns |
| Clock High Pulse Width | t _{ch} | 2.5 | — | 2.5 | — | 3.0 | — | ns |
| Clock Low Pulse Width | t _{cl} | 2.5 | — | 2.5 | — | 3.0 | — | ns |
| Address Setup to Clock High | t _{as} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| CKE Setup to Clock High | t _{ces} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Data Setup to Clock High | t _{ds} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Write Setup to Clock High | t _{ws} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Address Advance to Clock High | t _{adv} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Chip Select Setup to Clock High | t _{css} | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| Address Hold to Clock high | t _{ah} | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| CKE Hold to Clock High | t _{ceh} | 0.5 | - | 0.5 | — | 0.5 | — | ns |
| Data Hold to Clock High | t _{dh} | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| Write Hold to Clock High | t _{wh} | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| Address Advance to Clock High | t _{advh} | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| Chip Select Hold to Clock High | t _{csH} | 0.5 | — | 0.5 | — | 0.5 | — | ns |

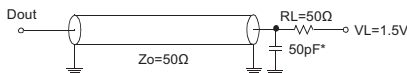
NOTES:

1. All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and CSx# is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.
3. A write cycle is defined by WE# low having been registered into the device at ADV Low. A Read cycle is defined by WE# High with ADV Low. Both cases must meet setup and hold times.

AC TEST CONDITIONS

| Parameter | Value |
|--|-------------------------|
| Input Pulse Level | 0 to 3.6V |
| Input Rise and Fall Time | 1.0V/ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Output Load (A & B) |

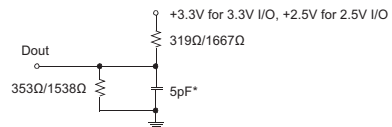
OUTPUT LOAD (A)



V_L = 1.5V for 3.3V I/O
V_{CCQ}/2 for 2.5V I/O

OUTPUT LOAD (B)

FOR t_{lzc}, t_{lzoE}, t_{hzoE}, and t_{hzc}



*Including Scope and Jig Capacitance



SNOOZE MODE

SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to ISB2Z. The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH, ISB2Z is guaranteed after the setup time tzz is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

Snooze Mode

| Description | Conditions | Symbol | Min | Max | Units |
|------------------------------------|------------------|--------|-----|-----|-------|
| Current during SNOOZE MODE | $ZZ \geq V_{IH}$ | ISB2Z | | 20 | mA |
| ZZ active to input ignored | | tzz | | 2 | cycle |
| ZZ inactive to input sampled | | trzz | 2 | | cycle |
| ZZ active to snooze current | | tzz1 | | 2 | cycle |
| ZZ inactive to exit snooze current | | trzz1 | 0 | | ns |

FIGURE 2 – SNOOZE MODE TIMING DIAGRAM

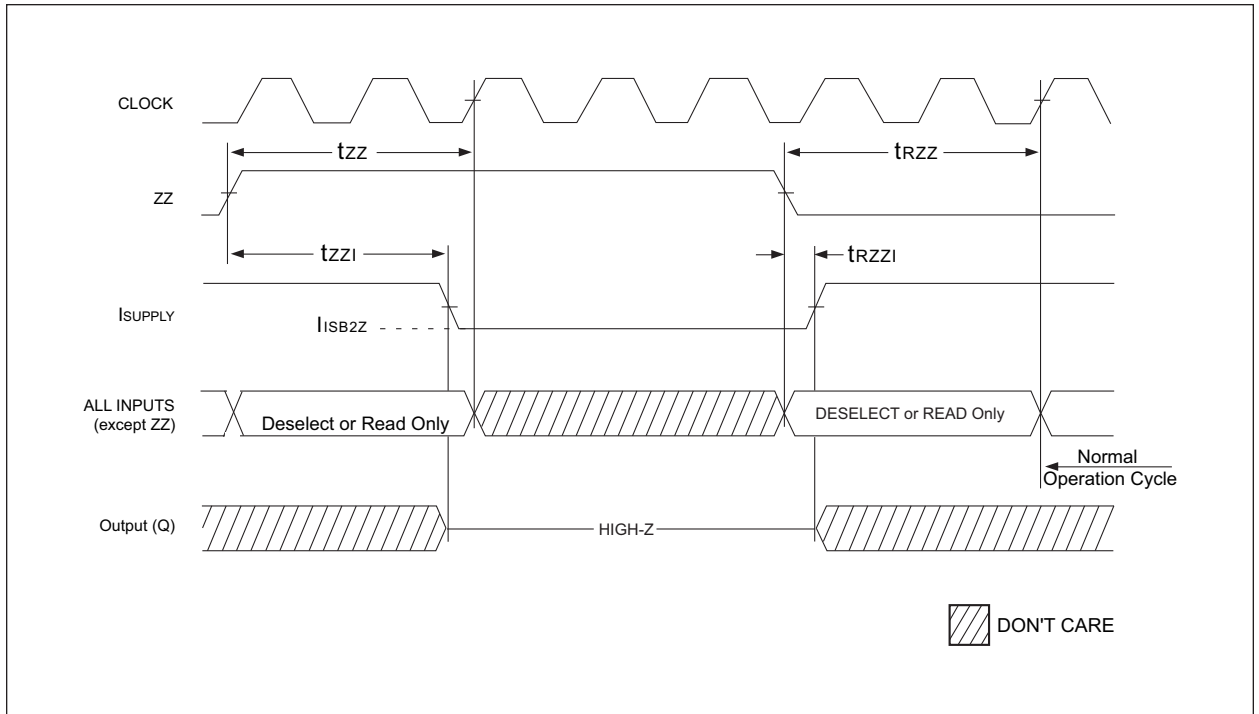




FIGURE 3 – TIMING WAVEFORM OF READ CYCLE

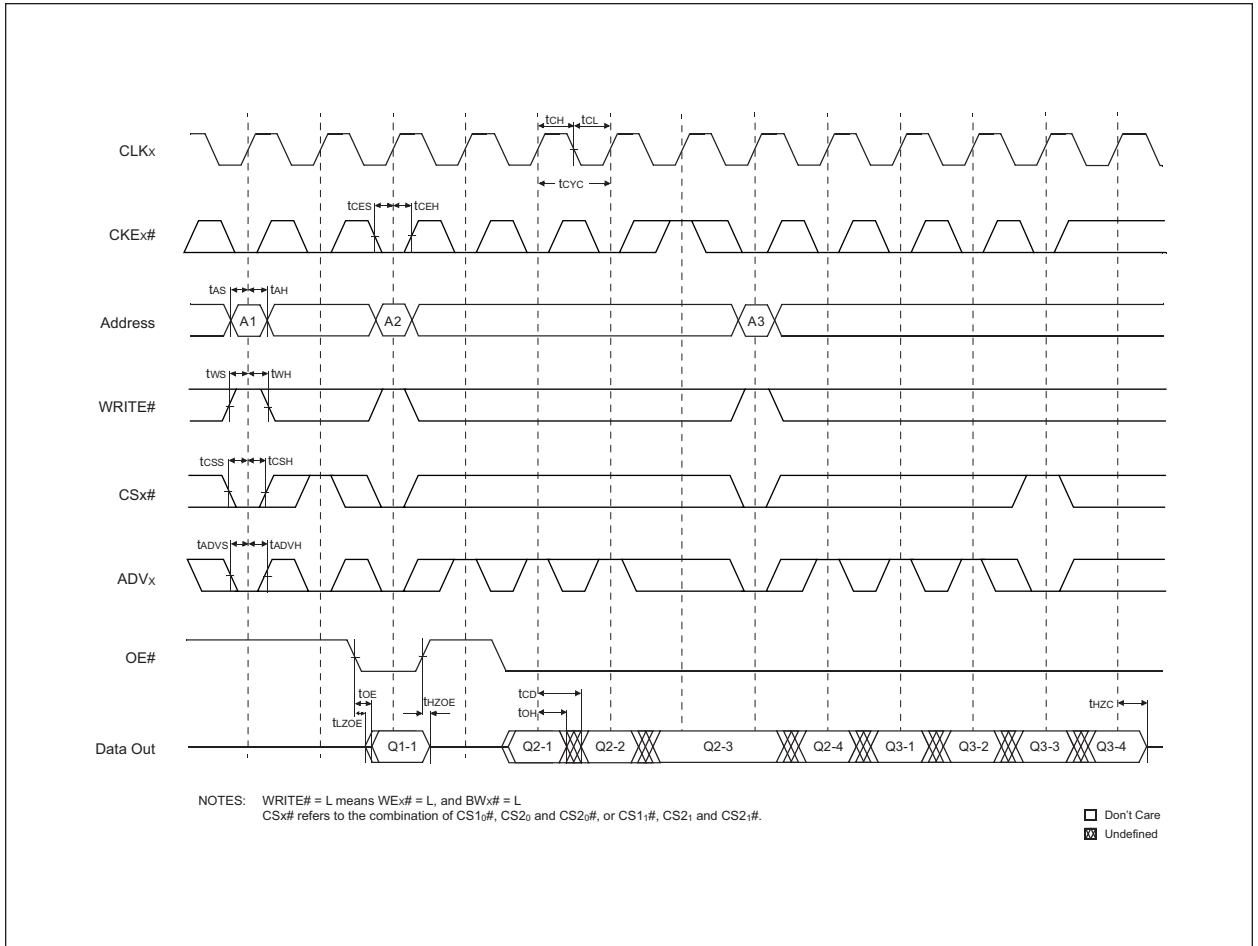
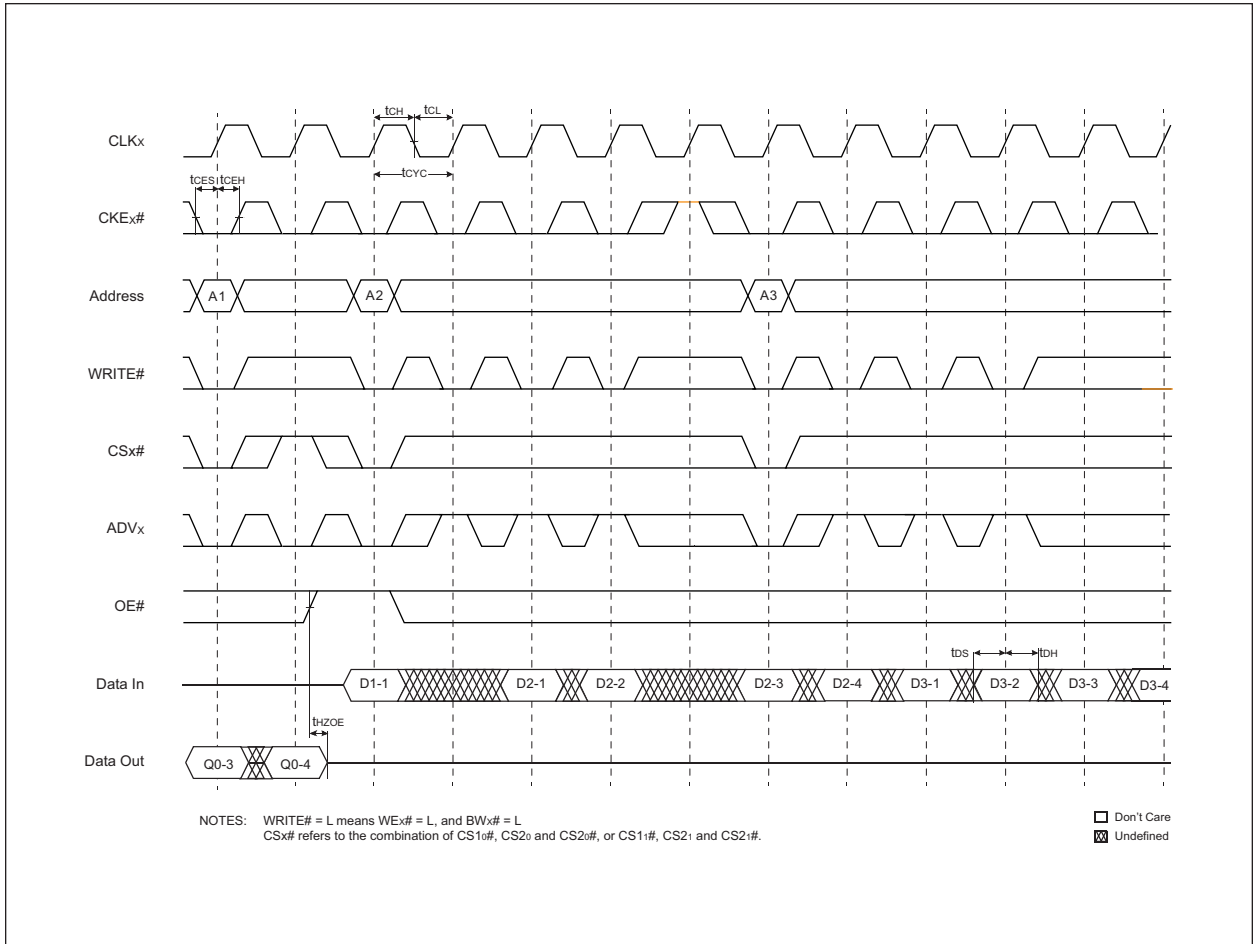




FIGURE 4 – TIMING WAVEFORM OF WRITE CYCLE



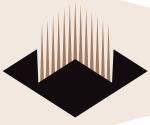


FIGURE 5 – TIMING WAVEFORM OF SINGLE READ/WRITE

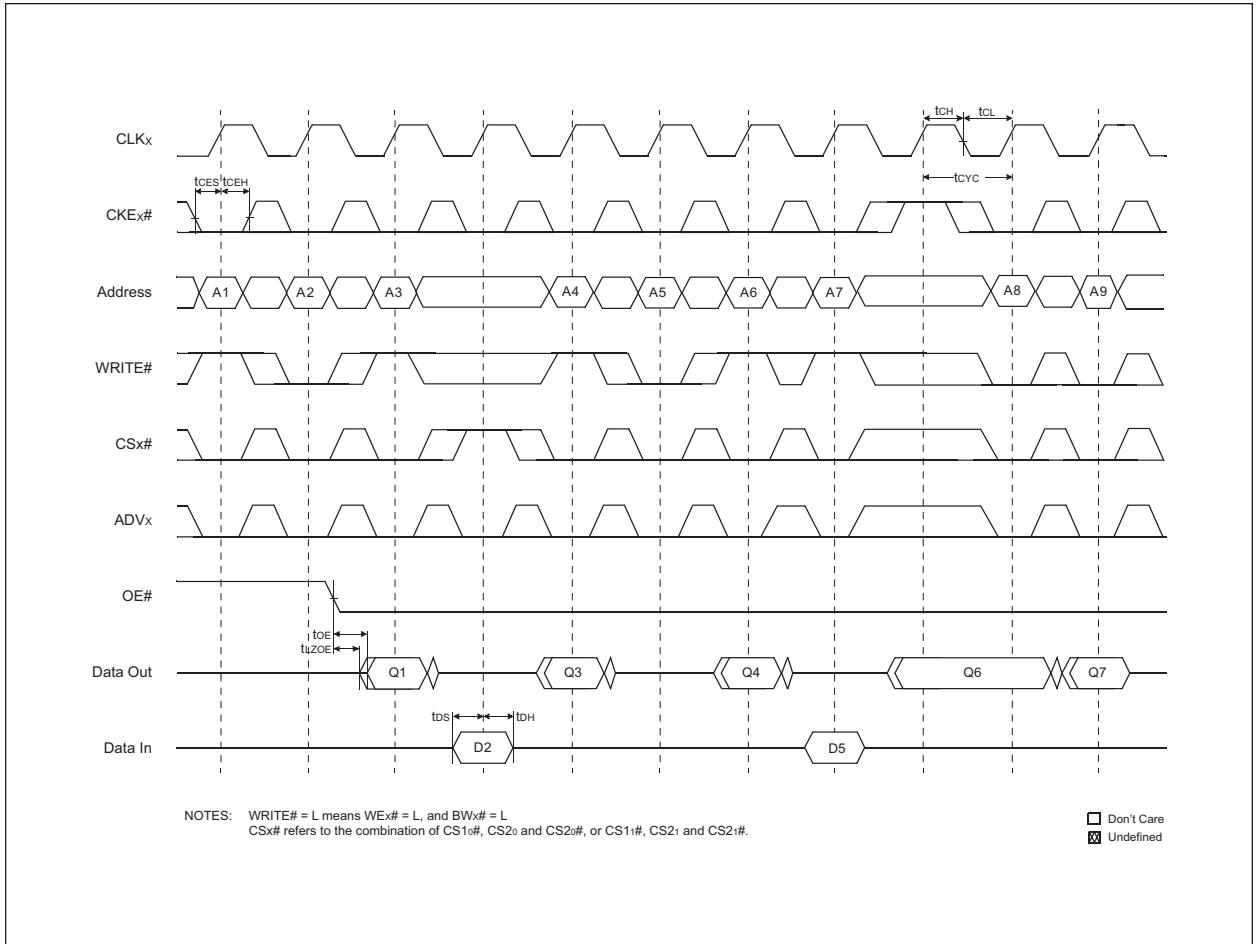




FIGURE 6 – TIMING WAVEFORM OF CKE OPERATION

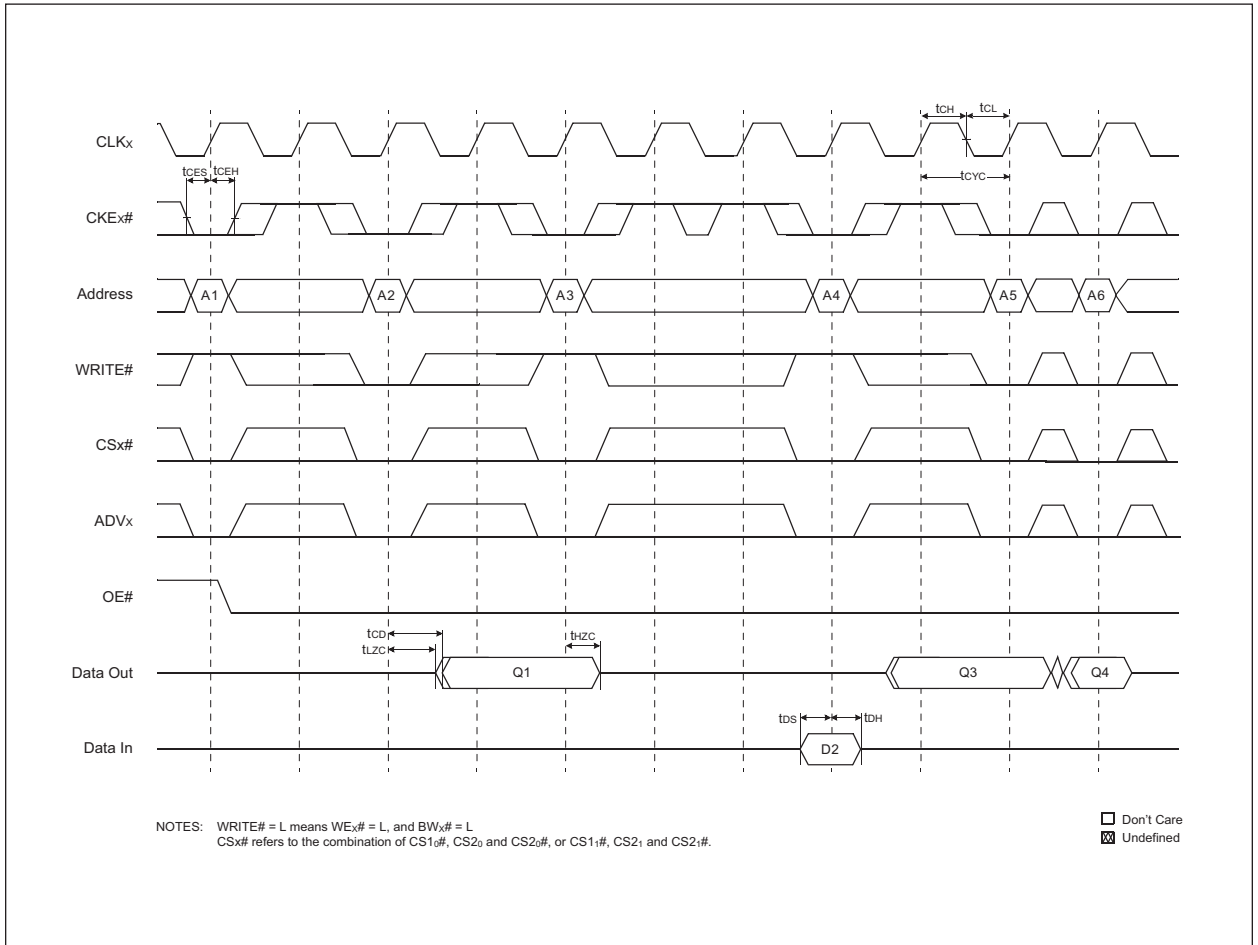
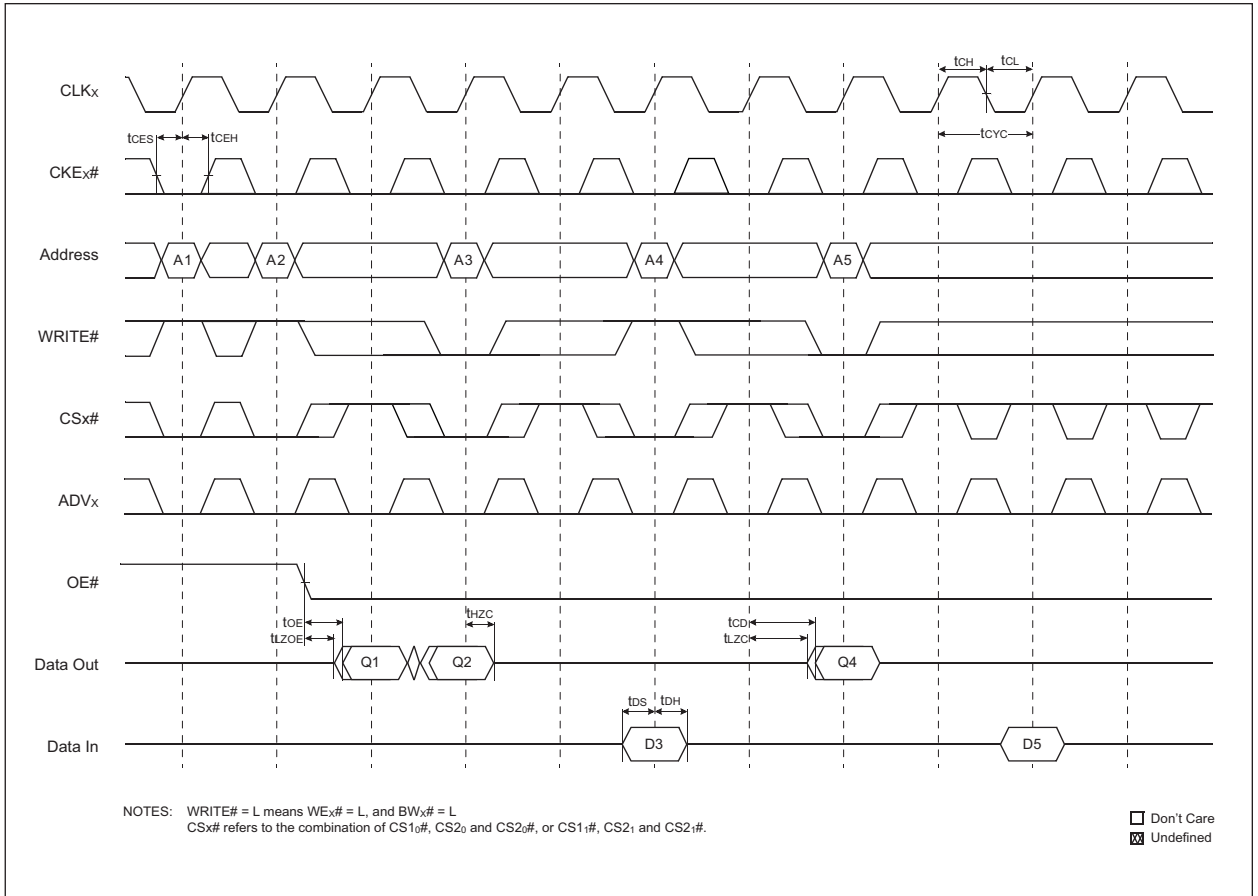


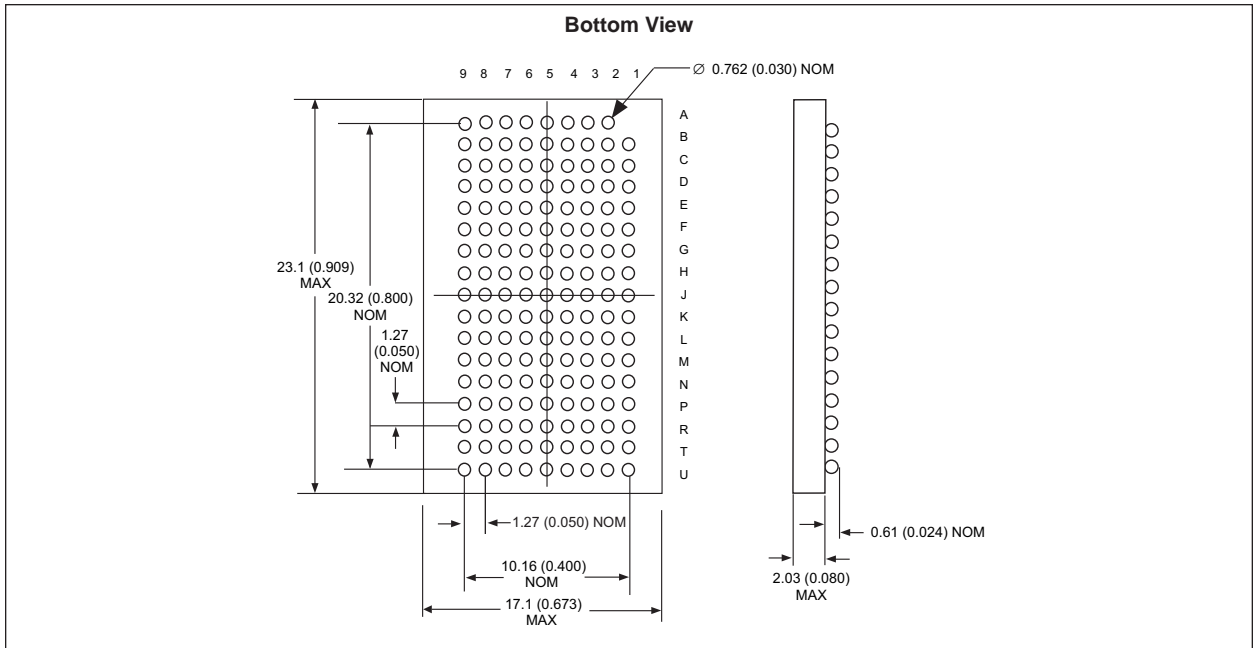


FIGURE 7 – TIMING WAVEFORM OF CE OPERATION



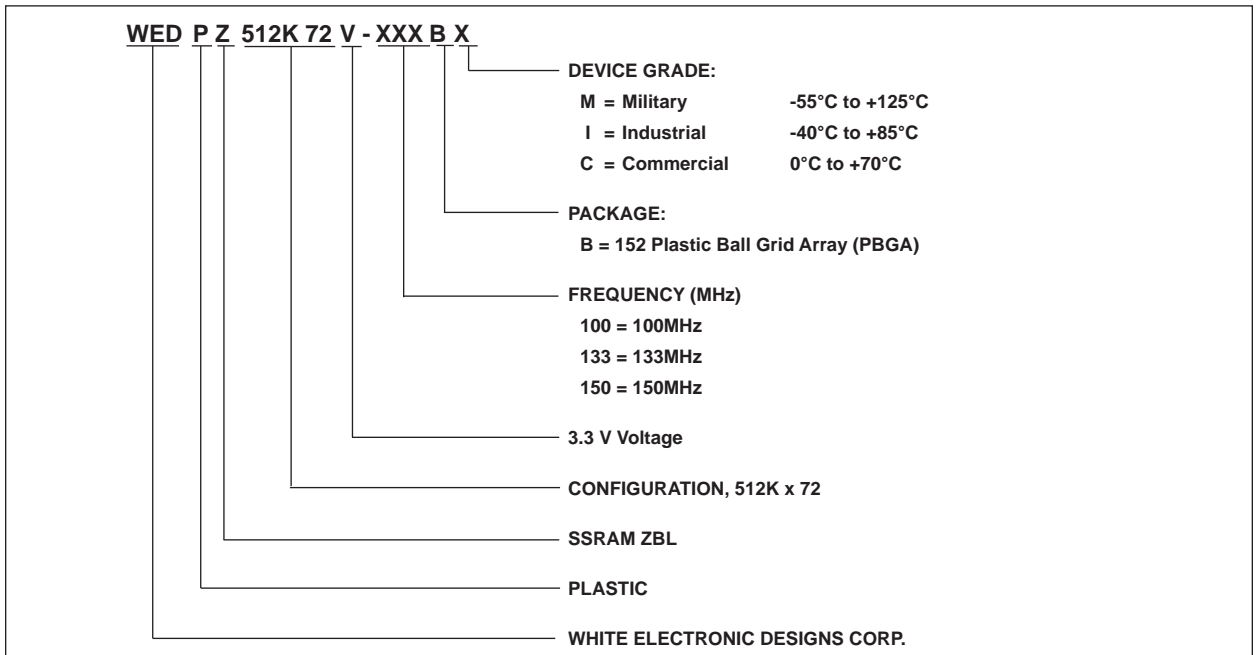


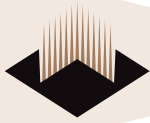
PACKAGE DIMENSION: – 152 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



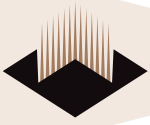


Document Title

512K x 72 Synchronous Pipeline Burst ZBL SRAM

Revision History

| Rev # | History | Release Date | Status |
|-------|---|---------------|-------------|
| Rev 0 | Initial Release | May 2001 | Advanced |
| Rev 1 | Changes (Pg. 1) 1.1 Change status from Advanced to Preliminary | March 2001 | Preliminary |
| Rev 2 | Changes (Pg. 1, 2) 2.1 Block Diagram: Address lines should be A0-18 2.2 Pin Configuration: Add Note *Pin F8 reserved for A19 upgrade to 1Mx72. | March 2002 | Preliminary |
| Rev 3 | Changes (Pg. 1, 5) 3.1 BGA Capacitance: Remove references to temperature in individual conditions 3.2 Change C_i from 10pF to 8pF 3.3 Change C_A from 20pF to 16pF 3.4 Change C_{CK} from 7pF to 6pF 3.5 Add Control Input Capacitance (C_{IC}) 16pF | November 2002 | Preliminary |
| Rev 4 | Changes (Pg. 5) 4.1 Add Thermal Resistance table 4.2 Update current values 4.3 Update package mechanical drawing | May 2003 | Preliminary |
| Rev 5 | Changes (Pg. 1, 5, 14) 5.1 Remove reference to Preliminary status 5.2 Add Maximum Operating Junction Temperature of 125°C | June 2003 | Preliminary |
| Rev 6 | Changes (Pg. 1, 13, 14) 6.1 Change mechanical drawing to new style | November 2003 | Preliminary |
| Rev 7 | Changes (Pg. 1, 5, 14) 7.1 Change VIL 3.3V to 0.7V maximum 7.2 Change status to Final | February 2006 | Final |

**Document Title**

512K x 72 Synchronous Pipeline Burst ZBL SRAM

Revision History Continued

| Rev # | History | Release Date | Status |
|--------------|---|---------------------|---------------|
| Rev 8 | Changes (Pg. 5) 8.1 Die rev to Issi IS6InLP51236 8.2 Electrical Characteristics: $V_{IH\ MAX} = V_{CC} + 0.3$ 8.3 V_{IL} : 3.3V I/O = 0.8 MAX 8.4 I_{IL} : MIN = -10 μ A; MAX = 10 μ A 8.5 I_{OL} : MIN = 5 μ A; MAX = +5 μ A 8.6 Note 2: = \pm 200mA 8.7 ISB22 = 300mA for all speeds 8.8 ISB = 400mA for all speeds 8.9 Thermal Resistance = TBD | November 2008 | Final |
| Rev 9 | Changes (Pg. 5) 9.1 V_{OH} condition changed from: $I_{OH} = -4.0mA$ to: $I_{OH} = -2mA$ (3.3V I/O). 9.2 V_{OL} condition changed from: $I_{OL} = 8.0mA$ (3.3V I/O) to: $I_{OL} = 6mA$ (3.3V I/O). 9.3 Correction to note: ZZ to LBO# | February 2009 | Final |