



## P-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	V <sub>GS(th)</sub> (max)	Order Number / Package			
				TO-39	TO-92	TO-220	DICE†
-160V	12Ω	-0.75A	-2.4V	TP0616N2	TP0616N3	TP0616N5	TP0616ND
-200V	12Ω	-0.75A	-2.4V	TP0620N2	TP0620N3	TP0620N5	TP0620ND

† MIL visual screening available

### High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

### Features

- Low threshold — -2.4 V max
- High input impedance
- Low input capacitance — 85 pF typical
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

### Applications

- Logic level interface – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drive
- Analog switches
- General purpose line driver
- Telecom switches

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

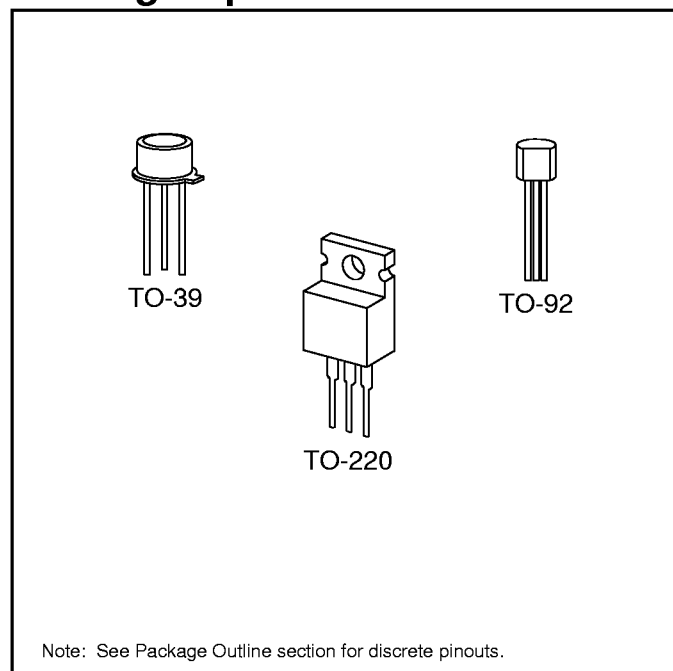
\* Distance of 1.6 mm from case for 10 seconds.

### Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



Note: See Package Outline section for discrete pinouts.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-39	-0.6A	-1.5A	6W	20.8	125	-0.6A	-1.5A
TO-92	-0.4A	-0.8A	1W	125	170	-0.4A	-0.8A
TO-220	-1.4A	-2.5A	45W	2.7	70	-1.4A	-2.5A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

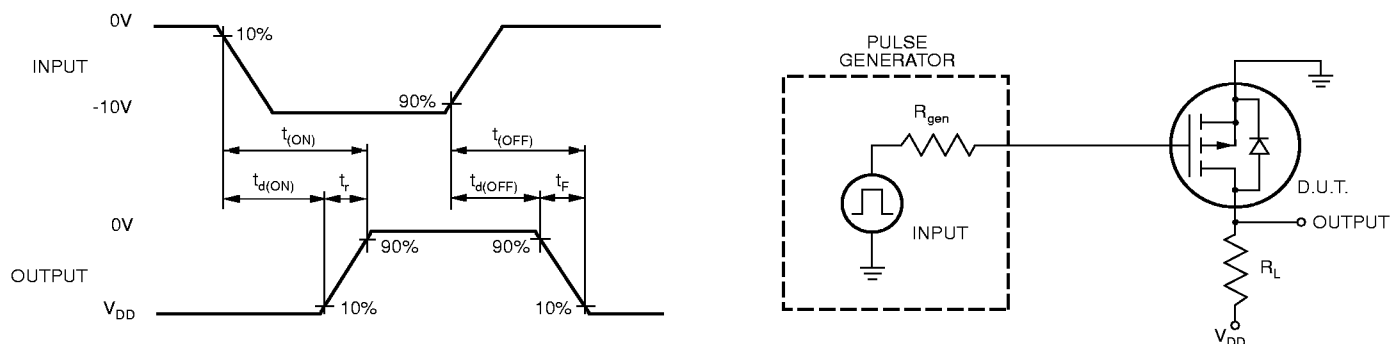
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	TP0620	-200			V $V_{GS} = 0, I_D = -2.0\text{mA}$
		TP0616	-160			
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$I_{GSS}$	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
$I_{DSS}$	Zero Gate Voltage Drain Current			-10	$\mu\text{A}$	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				-1.0	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-0.25			A	$V_{GS} = -5\text{V}, V_{DS} = -25\text{V}$
		-0.75				$V_{GS} = -10\text{V}, V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		9.0	15	$\Omega$	$V_{GS} = -5\text{V}, I_D = -0.1\text{A}$
			7.0	12		$V_{GS} = -10\text{V}, I_D = -0.2\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.7	%/ $^\circ\text{C}$	$V_{GS} = -10\text{V}, I_D = -0.2\text{A}$
$G_{FS}$	Forward Transconductance	100	150		m $\Omega^{-1}$	$V_{DS} = -25\text{V}, I_D = -0.4\text{A}$
$C_{ISS}$	Input Capacitance		85	150	pF	$V_{GS} = 0, V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance		30	85		
$C_{RSS}$	Reverse Transfer Capacitance		10	35		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = -25\text{V}$ $I_D = -0.75\text{A}$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
$t_f$	Fall Time			16		
$V_{SD}$	Diode Forward Voltage Drop			-1.8	V	$V_{GS} = 0, I_{SD} = -0.5\text{A}$
$t_{rr}$	Reverse Recovery Time		300		ns	$V_{GS} = 0, I_{SD} = -0.5\text{A}$

### Notes:

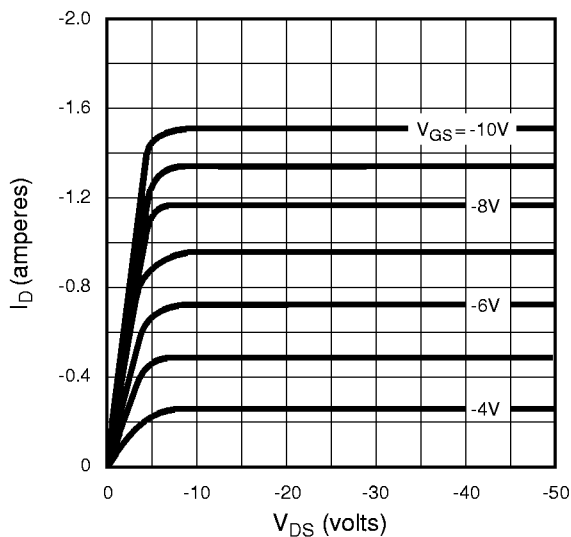
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

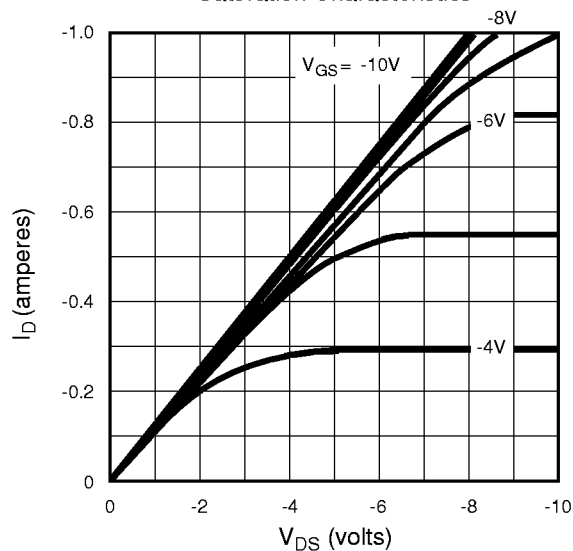


# Typical Performance Curves

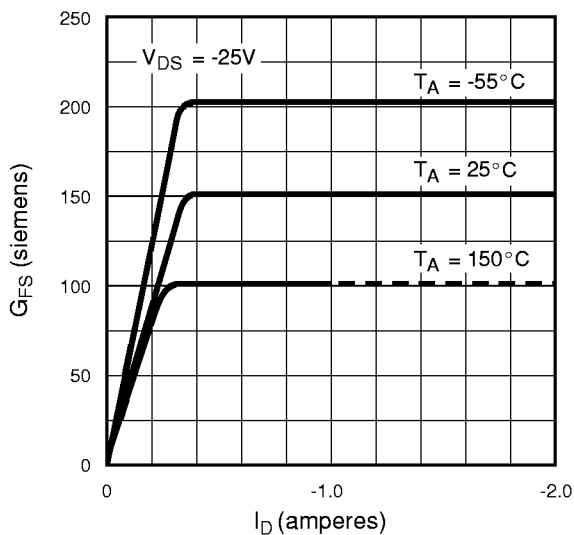
Output Characteristics



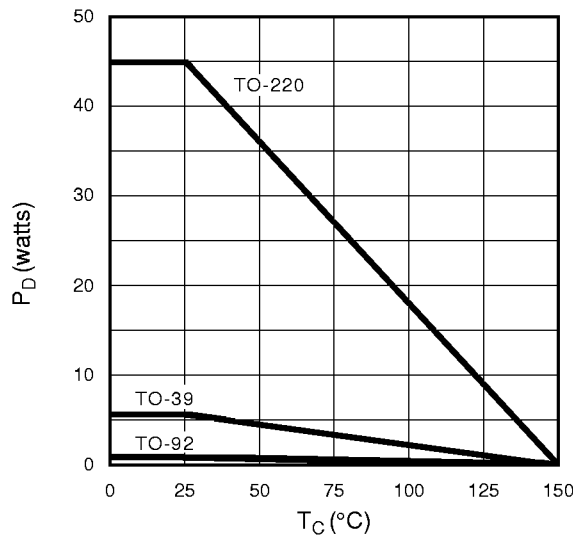
Saturation Characteristics



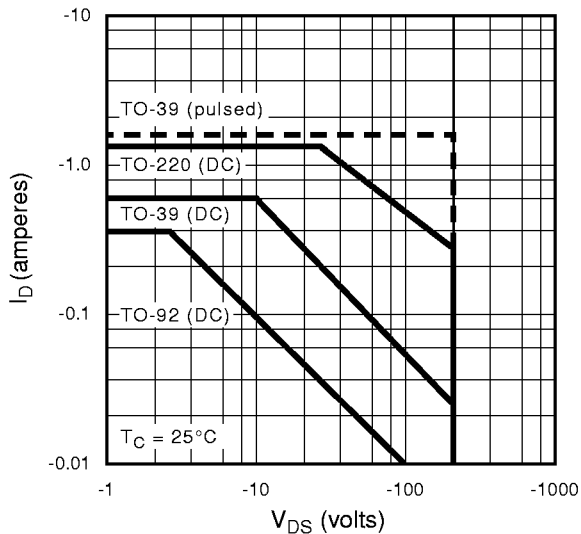
Transconductance vs. Drain Current



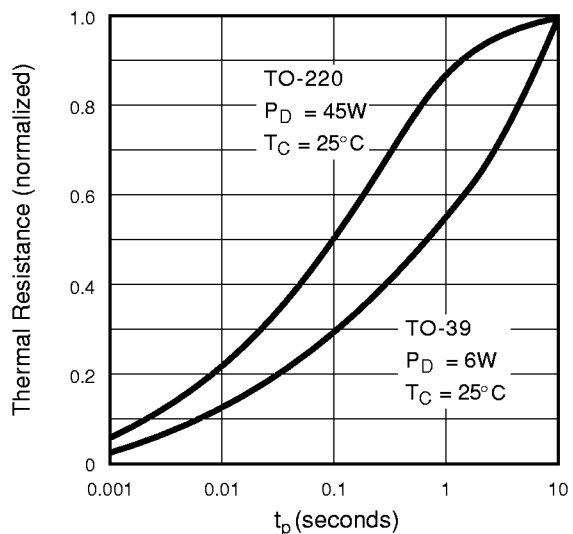
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

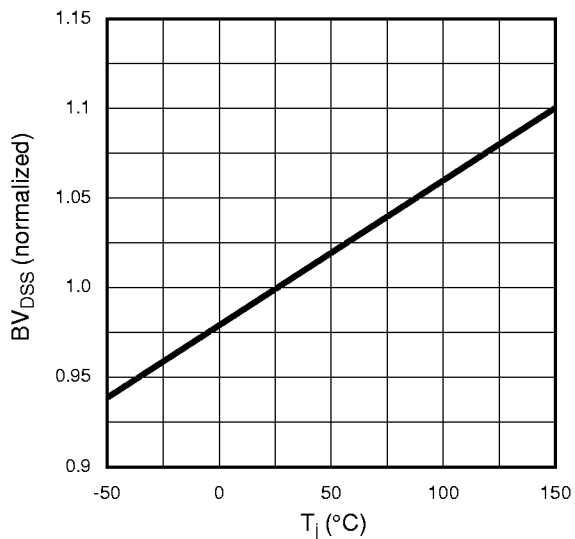


Thermal Response Characteristics

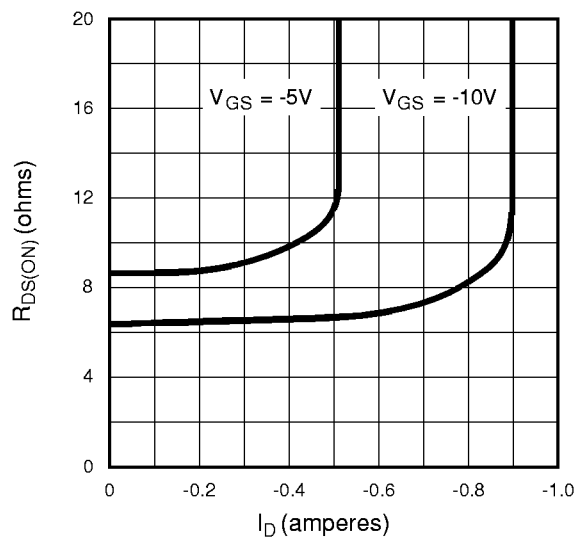


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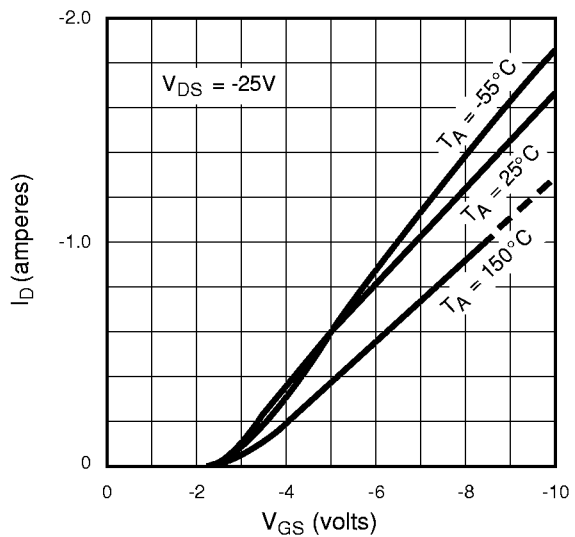
BV<sub>DSS</sub> Variation with Temperature



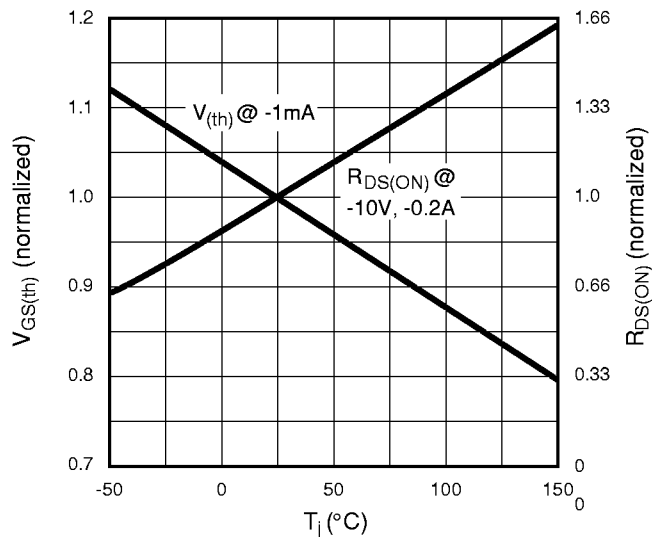
On-Resistance vs. Drain Current



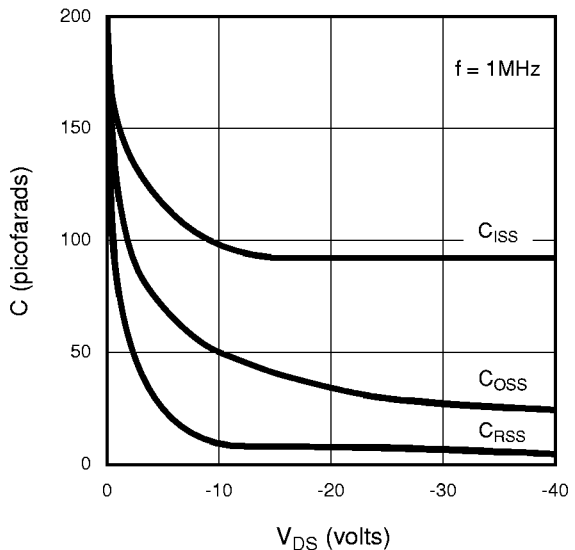
Transfer Characteristics



V<sub>(th)</sub> and R<sub>DS</sub> Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

