MH12808TNA-85,-10,-12,-15/ MH12808TNA-85H,-10H,-12H,-15H

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The MH12808TNA is a 1048576-bits CMOS static RAM module organized as 131072-words by 8-bits. It consists of four industry standard 32K × 8 static RAMs and one decoder.

The stand-by current is low enough for a battery backup application. It is mounted a flat package on a 32-pin dual in line package and configured in an industrial standard 128K × 8-bits pin out.

FEATURES

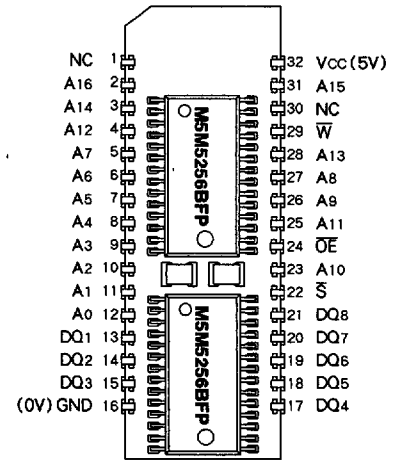
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH12808TNA-85 MH12808TNA-10 MH12808TNA-12 MH12808TNA-15	85ns 100ns 120ns 150ns	70mA	200 μA
MH12808TNA-85H MH12808TNA-10H MH12808TNA-12H MH12808TNA-15H	85ns 100ns 120ns 150ns		40 μA

- JEDEC standard 32-pin 600mil pin out
- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Solder dipping lead

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW) (Both side)



Outline 32N1 NC : NO CONNECTION

MITSUBISHI ELECTRIC

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FUNCTION

The operation mode of the MH12808TNA is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

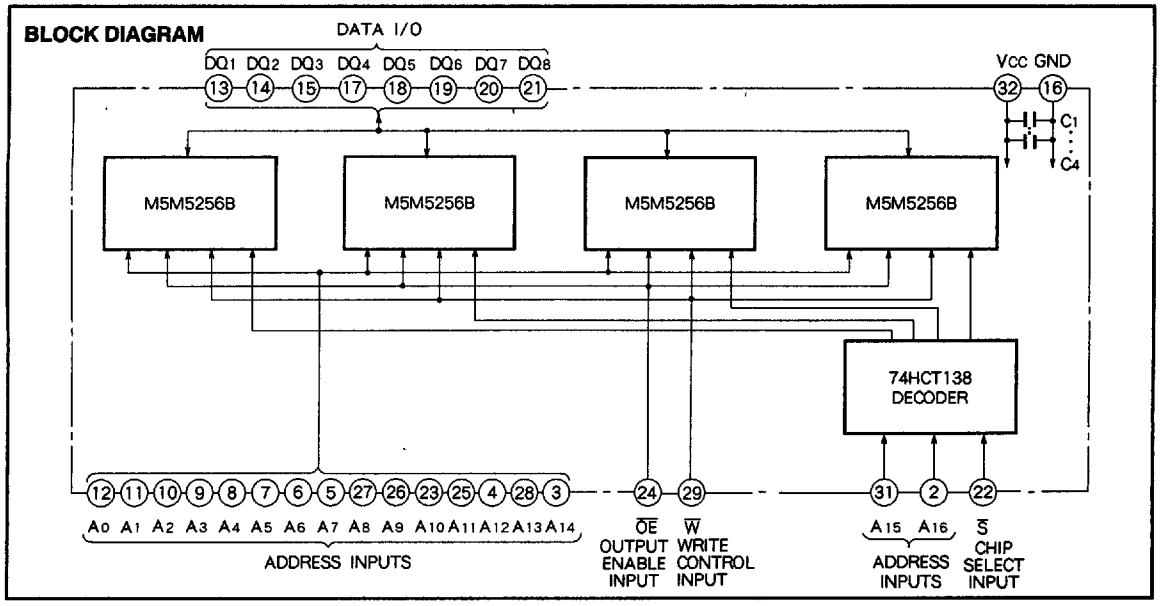
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high- impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	DIN	Active
L	H	L	Read	DOUT	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage		−0.3~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted)

symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IH}	High input voltage	2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage	−0.3		0.8	V

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			−0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = −1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				±4	μA
I_O	Output current in off-state	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				±4	μA
I_{CC1}	Active supply current (AC. MOS level)	$\overline{S}$ < 0.2, output open other input < 0.2V or > V_{CC} − 0.2V Min. cycle			30	65	mA
I_{CC2}	Active supply current (AC. TTL level)	$\overline{S}$ = V_{IL}, output open other input = V_{IL} or V_{IH} Min. cycle			35	70	mA
I_{CC3}	Stand-by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V A_{15} and A_{16} ≦ 0.2V or ≧ V_{CC} − 0.2V Other inputs = 0~V_{CC}	TNA			400	μA
			TNA-H			80	
I_{CC4}	Stand-by supply current	$\overline{S}$ = V_{IH}, Other inputs = 0~V_{CC}				15	mA
C_I	Input capacitance (Ta = 25℃)	V_I = GND, V_i = 25mVrms, f = 1MHz				30	pF
C_O	Output capacitance (Ta = 25℃)	V_O = GND, V_o = 25mVrms, f = 1MHz				30	pF

Note 1 : Direction for current flowing into IC is indicated as positive (no mark).
2 : Typical value is V_{CC} = 5V, Ta = 25℃.

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SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)
Read cycle

Symbol	Parameter	Limits												Unit
		MH12808TNA-85			MH12808TNA-10			MH12808TNA-12			MH12808TNA-15			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			120			150			ns
$t_{a(A)}$	Address access time			85			100			120			150	ns
$t_{a(S)}$	Chip select access time			85			100			120			150	ns
$t_{a(OE)}$	Output enable access time			45			50			60			75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high			30			35			40			45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30			35			40	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5			10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			10			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			20			ns

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)
Write cycle

Symbol	Parameter	Limits												Unit
		MH12808TNA-85			MH12808TNA-10			MH12808TNA-12			MH12808TNA-15			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			120			150			ns
$t_{w(W)}$	Write pulse width	55			60			60			70			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(A-\overline{WH})}$	Address set up time with respect to $\overline{W}$ high	80			90			95			100			ns
$t_{su(S)}$	Chip select set up time	75			85			95			100			ns
$t_{su(D)}$	Data set up time	30			35			35			40			ns
$t_{h(D)}$	Date hold time	0			0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30			35			40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			25			30			35			40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5			5			10			10			ns

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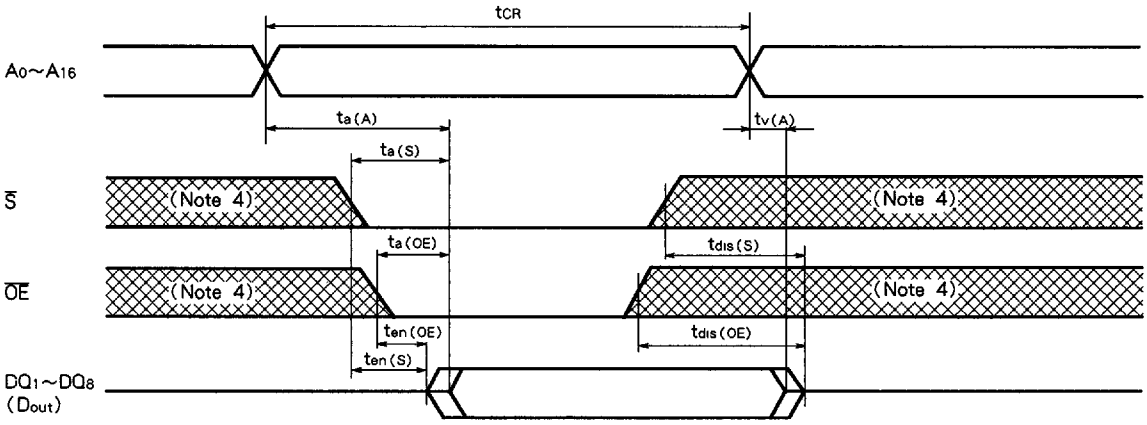
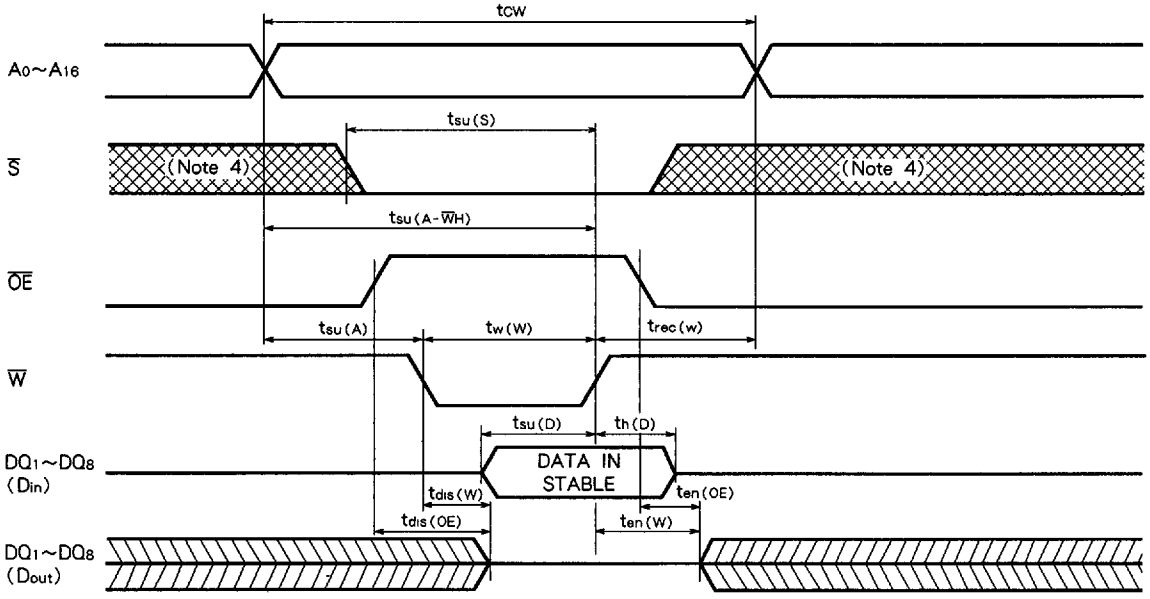
TIMING DIAGRAM

Read cycle



W = "H"level

Write cycle (W control)



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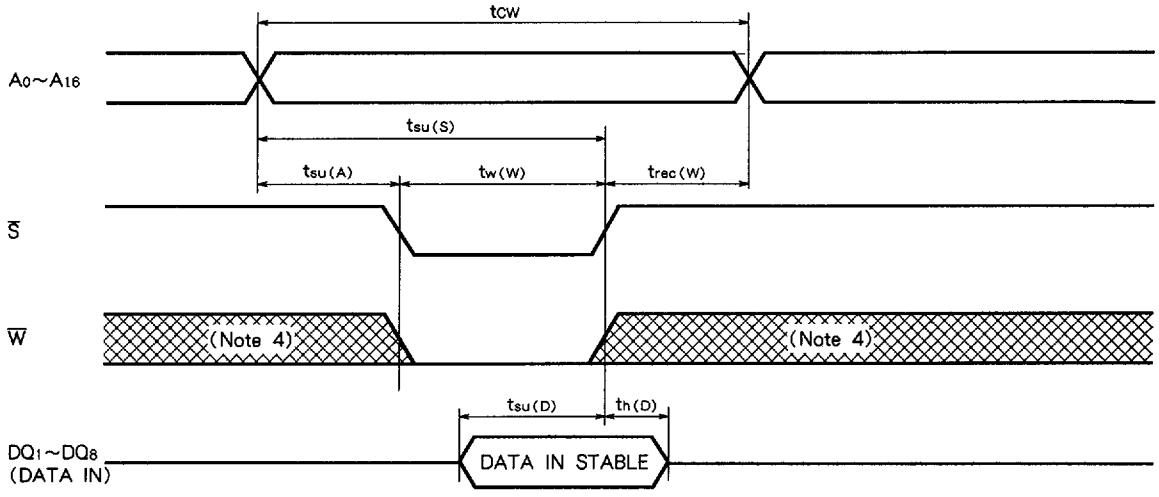
Write cycle ($\overline{S}$ control)



Note 3 : Test condition
Input pulse level : 0.4~2.4V
Input pulse rise fall time : 10ns
Load : 1TTL, CL = 100pF
Conditions of assessment : 1.5V
4 : Hatching indicates the state is don't care.
5 : Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6 : If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high − impedance state.
7 : Don't active inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, A_{15} and A_{16} ≦ 0.2V or ≧ V_{CC} − 0.2V Other inputs = 0~V_{CC}	TNA			200	μA
			TNA-H			40 (Note 8)	

Note 8 : Ta = 25℃, $I_{CC\ (PD)}$ = 9 μA

TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS