OKI Semiconductor

MSM7570L / MSM7590L

3V Single-Rail ADPCM CODECs

DESCRIPTION

The MSM7570L and MSM7590L are single-rail, low-voltage, single-channel, full-duplex ADPCM CODECs which perform voice digitization using presampling and reconstruction filters for transmit and receive operations in systems upgrading to ADPCM (Adaptive Differential Pulse Coded Modulation) encoding techniques. These CODECs offer ADPCM encoder/decoder operation, reducing the data rate required to transmit a PCM encoded voice signal. The MSM7570L (μ-law) and MSM7590L (A-law) implement the two most common companding schemes accepted worldwide. These CODECs convert 300 Hz to 3400 Hz voiceband analog signals into either 32 Kbps to 2048 Kbps ADPCM or 64 Kbps to 2048 Kbps PCM serial data, and are available in two versions, -01 and -02, offering variations in modulated frequency tones.

As the telecommunications industry quickly expands with enhanced applications in next generation digital cordless and Personal Handy Phone (PHP) system applications, OKI's MSM7570L and MSM7590L keep power consumption to a minimum during operation and power-down, saving valuable battery life, while minimizing overall noise. By integrating discrete components on-chip, OKI reduces systems costs while saving board space.

The MSM7570L/MSM7590L series of ADPCM CODECs come in two versions (-01 and -02) offering variations in modulated frequency tones. The CODECs are designed using OKI's high-quality CMOS process, providing superior low-power performance. Designers will find our space-saving 32-pin TSOP (TS-K) package perfect for a variety of applications.

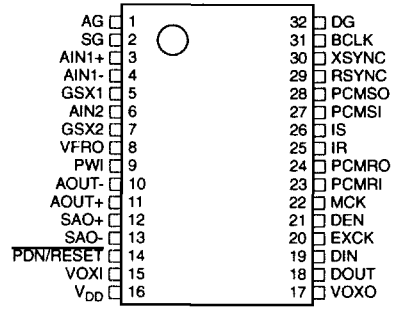
FEATURES

- Single 3V power supply eliminates second supply requirements
- Low power consumption increases battery life
  - Operating mode: 70 mW, typical
  - Power-down mode: 0.5 mW, typical
- ADPCM system conforms to CCITT recommendations G.721 (32 Kbps), G.723 (24 Kbps), and G.726 (16 Kbps)
- Serial ADPCM/PCM data rates of 64 Kbps to 2048 Kbps
- Transmit/receive full-duplex operation provides one-chip solutions
- Transmit/receive synchronous operation only
- Internal two-step amplifier improves sensitivity for analog input gain control
- Transmit/receive programmable gain setting completely integrated
- Side tone generation expands voice feedback option with eight levels of control
- Analog output format: push-pull driving
  - 350 Ω + 120 nF direct driving possible
- PCM code format conforms to standards with selectable dual-standard switching (A-law/μ-law selectable)
- Transmit/receive mute function
- Master clock frequency (only difference between the MSM7570L and the MSM7590L):
  - MSM7570L: 12.288/19.200 MHz, selectable
  - MSM7590L: 10.368 MHz
- DTMF tone generator provides further integration
- Various ringing tone and call-up tone generators lowers external component count
- Control by serial microcomputer interface complies with standards architectures
- Amplifier for drive sound output lowers external component count
- VOX functions offer more integration with voice signal detection (transmit) and background noise generation (receive)
- 814 mil 32-pin TSOP package available

MSM7570L / MSM7590L PACKAGES

Part Number	Package Type	Pins	Package Number
MSM7570L-TS-K-01	TSOP (Type I)	32-pin	TSOP32-P-814-K
MSM7570L-TS-K-02	TSOP (Type I)	32-pin	TSOP32-P-814-K
MSM7590L-TS-K-01	TSOP (Type I)	32-pin	TSOP32-P-814-L
MSM7590L-TS-K-02	TSOP (Type I)	32-pin	TSOP32-P-814-L

PIN CONNECTIONS



32-Pin TSOP

Pin	Description	Pin	Description
AG	Analog ground	DG	Digital ground
SG	Signal ground	BCLK	Shift clock signal input
AIN1+	Non-inverting transmit analog input	XSYNC	Receive PCM/ADPCM synchronizing signal
AIN1-	Inverting transmit analog input	RSYNC	Receive PCM/ADPCM synchronizing signal
GSX1	Transmit amplifier output, channel 1	PCMSO	Transmit PCM signal output
AIN2	Analog signal input, channel 2	PCMSI	Transmit PCM signal input
GSX2	Transmit amplifier output, channel 2	IS	Transmit ADPCM signal output
VFRO	Receive filter output	IR	Receive ADPCM signal input
PWI	Inverting input to the receive power amplifier	PCMRO	Receive PCM signal output
AOUT-	Inverting receive analog output	PCMRI	Receive PCM signal input
AOUT+	Non-inverting receive analog output	MCK	Master clock input
SAO+	Differential analog output	DEN	Enable signal input
SAO-	Differential analog output	EXCK	Data shift clock input
$\overline{\text{PDN/RESET}}$	Power-down/reset input	DIN	PCM signal input
VOXI	Receive VOX input	DOUT	PCM signal output
V_{DD}	+3V power supply	VOXO	Transmit VOX output

CIRCUIT CONFIGURATION

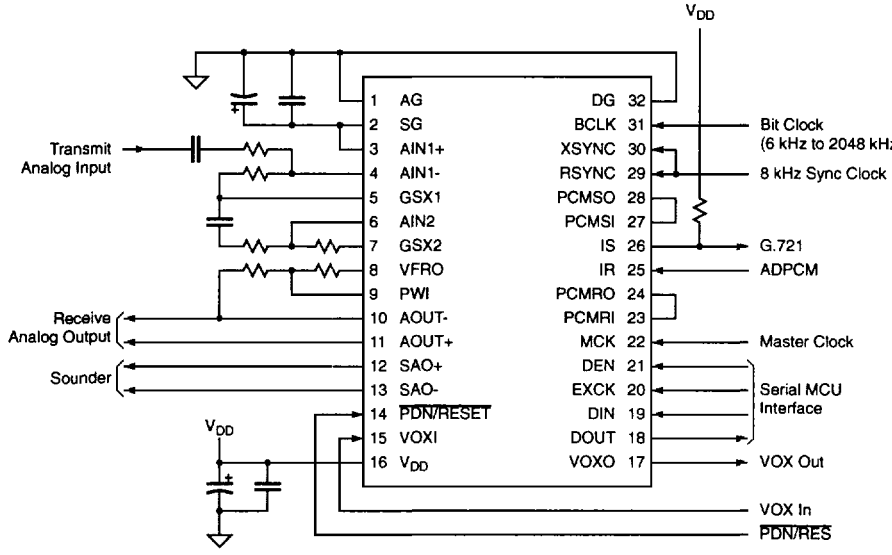


Figure 1. Example Circuit Wiring

BLOCK DIAGRAM

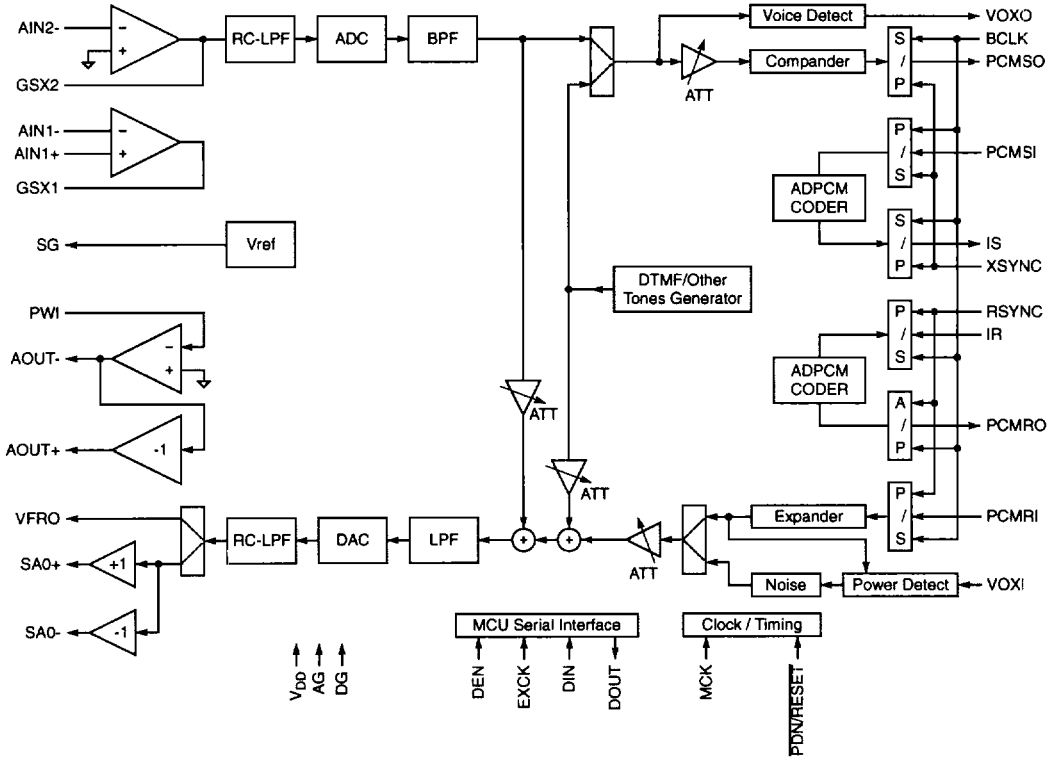


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin Name	Description
AIN1+, AIN1-, AIN2, GSX1, GSX2	Transmit analog input and transmit level control pins. AIN1- (AIN2) is connected to the inverted input pin of the internal transmit amplifier. GSX1 (GSX2) is connected to the output pin of the amplifier. Refer to *Figure 3* for details.
AOUT+, AOUT-, PWI, VFRO	Receive analog output and receive level control pins. VFRO is the receive filter output pin. AOUT+ and AOUT- are differential analog output pins that can directly drive a Z_L = 350 Ω +120 nF or 1.2 kΩ load. Refer to *Figure 3* for details.

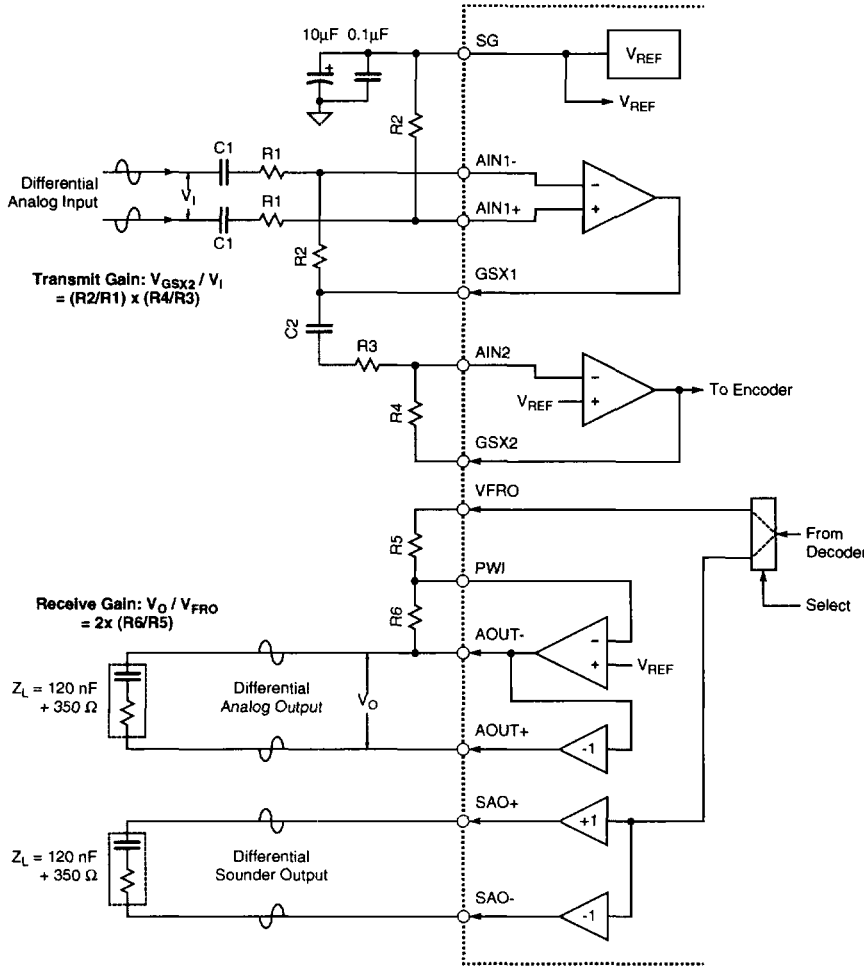


Figure 3. Analog I/O Interface

SAO+, SAO-	Differential analog output pins for sounder output. The output destination of call signals and such tones as sounder, DTMF, R and F can be set to the VFRO pin or SAO+ and SAO- pins by control register CR4/B5. The output load conditions of these pins are the same as AOUT+ and AOUT-.
SG	Analog signal ground potential output pin. The output voltage is about 1.4 V. Insert 10 µF and 0.1 µF (ceramic type) bypass capacitors between SG and AG. This output becomes 0V during power-down.
AG	Analog ground pin

PIN DESCRIPTIONS (Continued)

Pin Name	Description
DG	Digital ground pin. Since DG is separated from the analog ground pin (AG) on the chip, connect DG to AG on the board by the shortest distance.
V_{DD}	+3V power supply
$\overline{PDN/RESET}$	Power-down and reset control input pin. When this pin is set to digital "0", the LSI enters power-down status, and each bit of the control register is reset. During normal operation this pin is set to digital "1". Since this power-down control is processed by OR with CR0/B5 of the control register, set CR0/B5 to digital "0" when the $\overline{PDN/RESET}$ pin is used.
MCK	Master clock input pin. The frequency is either MSM7570L 12.288 MHz or 19.2 MHz, or 10.368 MHz MSM7590L and is selected by CR0/B6 of the control register. The master clock can be asynchronous with XSYNC, RSYNC and BCLK.
PCMSO	Transmit PCM signal output pin. This PCM output signal is output sequentially from MSB, synchronizing with the rise of BCLK and XSYNC. Refer to *Figure 4* for details.

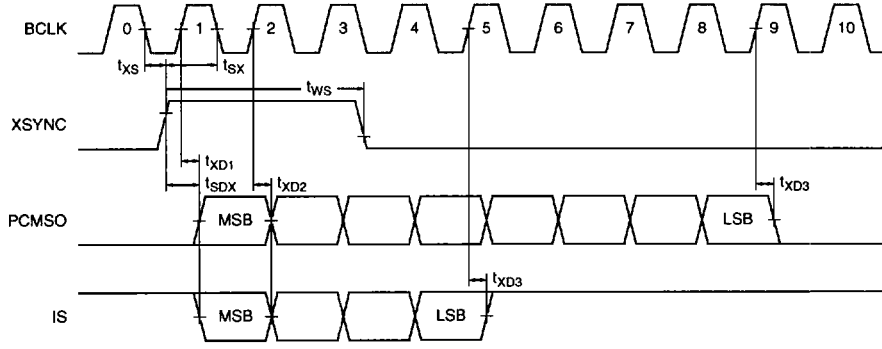


Figure 4. Transmit PCM/ADPCM Data Interface

PCMSI	Transmit PCM signal input pin. This PCM input signal is converted to transmit ADPCM data. PCM signals are shifted at the fall of BLCK, and are then input. Normally PCMSI is connected to PCMSO.
PCMRO	Receive PCM signal output pin. This PCM signal is output after receive ADPCM decoding, and is output sequentially from MSB, synchronizing with the rise of BCLK and RSYNC. Refer to *Figure 5* for details.

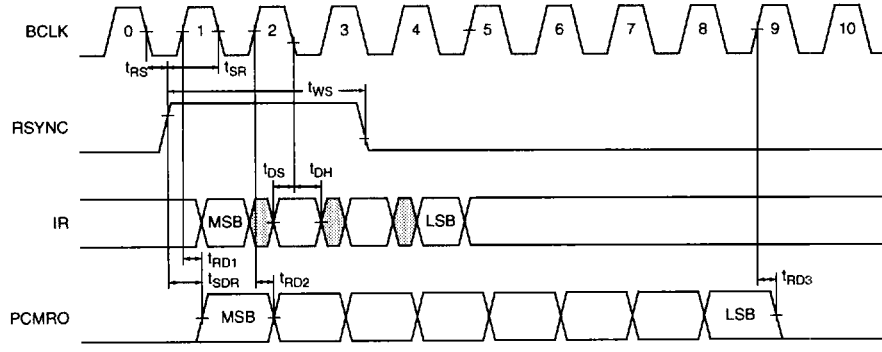
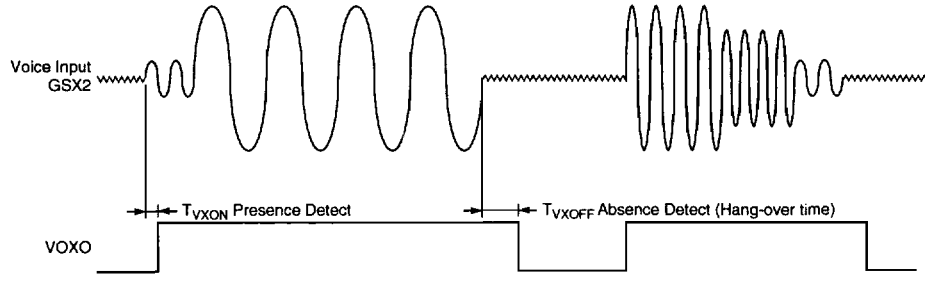


Figure 5. Receive PCM/ADPCM Data Interface

PCMRI	Receive PCM signal input pin. This PCM input signal is shifted at the fall of BCLK, and is input sequentially from MSB. Normally PCMRI is connected to PCMRO.

PIN DESCRIPTIONS (Continued)

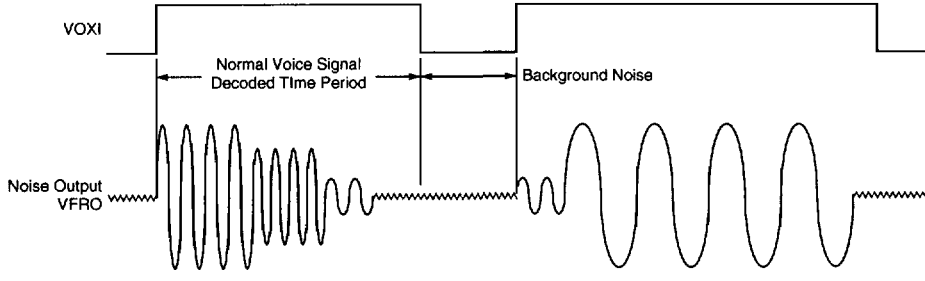
Pin Name	Description
IS	Transmit ADPCM signal output pin. This signal is output after ADPCM encoding, and is output sequentially from MSB, synchronizing with the rise of BCLK and XSYNC. Since this pin has an open drain output, pull-up resistance is required. During power-down, this pin enters high impedance status.
IR	Receive ADPCM signal input pin. This ADPCM signal is shifted at the fall of BCLK, synchronizing with RSYNC, and is input sequentially from MSB.
BCLK	Shift clock input pin for PCM data (PCMSO, PCMSI, PCMRO, PCMRI) and ADPCM data (IS, IR). The frequency is the same as the data speed. The available frequency is 64 kHz to 2048 kHz.
XSYNC	Transmit synchronizing signal input pin for PCM/ADPCM data. This signal must synchronize with BCLK signals. This signal indicates the position of MSB of PCM and ADPCM data.
RSYNC	Receive synchronizing signal input pin for PCM/ADPCM data. This signal must synchronize with BCLK signals. This signal indicates the position of MSB of PCM and ADPCM data.
VOXO	Output pin for transmit VOX functions. Sound/silent status is identified by detecting the power of a transmit signal. When sound exists, this pin becomes digital "1", and when silent, this pin becomes digital "0". The threshold value for identification is set by control register CR6/B6 and B5. This signal is also output to control register CR7/B7. Refer to *Figure 6* for details.



Note: VOXO functions are effective when CR6/B7 is set to "0"

Figure 6. Transmit VOX Function

VOXI	Input pin for receive VOX functions. Digital "1" indicates sound status. In this case normal receive signal processing is performed, and voice signals are output to the analog output pin. Digital "0" indicates silent status. In this case, background noise, generated on the LSI, is output to the analog output pin. The size of the background noise is set by control register CR6. Since this signal is internally combined with OR by CR6/B3, set CR6/B3 to "0" when this pin is used. Refer to *Figure 7* for details.



Note: VOXI functions are effective when CR6/B7 is set to "0"

Figure 7. Receive VOX Function (CR6/B3 = 0)

PIN DESCRIPTIONS (Continued)

Pin Name	Description
DEN, DIN, DOUT, EXCK	Serial control ports for the MCU interface. These LSIs have internal 8-byte control registers. Data is written/read by an external CPU using these pins. DEN is the enable signal input pin, EXCK is the clock signal input pin for data shifting, DIN is the address and data input pin, and DOUT is the data output pin. Refer to *Figure 8*, *Figure 9*, and *Figure 10* for details on the MCU interface.

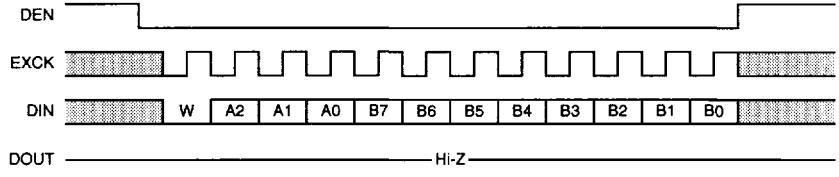


Figure 8. MCU Interface Write Data

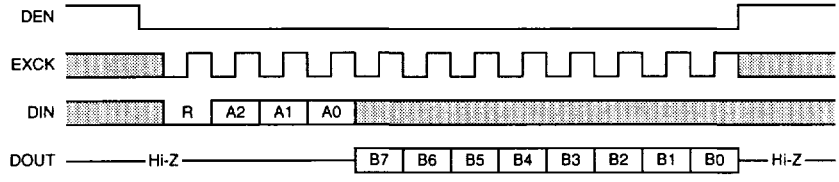


Figure 9. MCU Interface Read Data

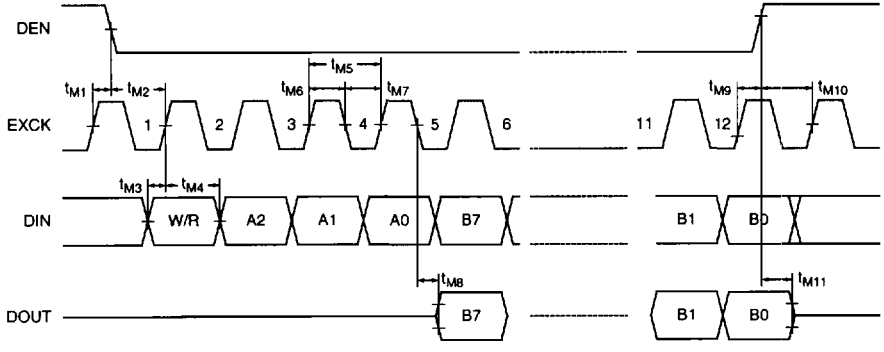


Figure 10. MCU Interface (Serial Data Transfer)

FUNCTIONAL DESCRIPTION

The MSM7570L and MSM7590L operate essentially identical to the transmit section utilizing a low-noise, gain-adjustment amplifier capable of driving 1.2 kΩ loads. Its output is fed to an active 3-pole, anti-aliasing filter. Following this stage, a BPF limits the frequency content to 3.4 kHz, and an oversampling delta sigma ADC converts the analog waveform to a digital sample. The signal is then companded to a PCM formatted signal. Based on the number of channels in a given system, an additional encoder (ADPCM) is available through external pin connections conforming to CCITT recommendations (G.721, G.723, G.726) and ANSI (T1.301 and T1.303) conforming to ADPCM telecom standards.

The receive section is comprised of the ADPCM decoder connected externally to the expander (PCM decoder). A PCM signal can by-pass the ADPCM decoder circuitry with connection directly to the PCMRI pin. Once decoded, equalization takes the form of a digital LPF using digital processing techniques, and noise correction (sin x/x) circuitry. A 10-bit oversampling delta sigma DAC performs quantization providing the LPF with an analog waveform which is then amplified. The power amplifier is capable of driving 350 Ω loads. The MCU oversees internal timing (windowing) via selectable master clock frequencies.

Additional functionality is incorporated to further ease the overall system design such as a push-pull analog output driving capability, simplifying drive interface, and serial microcontroller interface for seamless CODEC control.

CONTROL AND DETECT REGISTERS

The register map is shown below.

Name	Address A2	A1	A0	Control and Detect Data B7	B6	B5	B4	B3	B2	B1	B0	R/W
CR0	0	0	0	A/μ SEL	MCK SEL	PDN ALL	PDN TX	PDN RX	[1]	[1]	PDN SAO/AOUT	R/W
CR1	0	0	1	MODE1	MODE0	TX RESET	RX RESET	TX MUTE	RX MUTE	[1]	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	SIDE TONE GAIN2	SIDE TONE GAIN1	SIDE TONE GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR5	1	0	1	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]	R/W
CR6	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0	R/W
CR7	1	1	1	VOX OUT	TX LVL1	TX LVL0	[1]	[1]	[1]	[1]	[1]	R

[1] This bit is not assigned and is not in use

Control Register Contents

CR0 (Basic Operation Mode Setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/μ SEL	MCK SEL	PDN ALL	PDN TX	PDN RX	–	–	PDN SAO/AOUT
Initial value [1]	0	0	0	0	0	0	0	0

[1] The initial value of a register is reset by $\overline{\text{PDN/RESET}}$

B7

PCM interface recommendation rule. Set to 0 to select μ-law; set to 1 to select A-law.

B6

Master clock frequency. MSM7570L: Set to 0 to select the master clock frequency of 12.288 MHz; set to 1 to select the master clock frequency of 19.200 MHz. MSM7590L: Set to either 0 or 1 to automatically select 10.368 MHz.

B5

Transmit and receive power-down. Set to 0 to select power-on; set to 1 to select power-down.

Note: When using this data for power-down control, $\overline{\text{PDN/RESET}}$ should be set to digital "1"; this signal does not reset the control register.

B4

Transmit power-down. Set to 0 to select power-on; set to 1 to select power-down.

B3

Receive power-down. Set to a 0 to select power-on; set to 1 to select power-down.

B2, B1

Not in use

B0

Analog output amplifiers power-down. Set to 0 to select power-on for both the sounder output amplifier (SAO+, SAO-) and the receiver output amplifier (AOUT+, AOUT-); set to 1 to select power-down for the receiver output amplifier and for CR4/B5 to select the sounder output. Refer to the following table for details on analog output amplifiers.

Analog Output Amplifiers

CR0/B0	0	0	1	1
CR4/B5	0	1	0	1
Sounder amplifiers	Active 1 [1]	Active	PDN 2 [2]	Active
Receive amplifiers	Active	Active 1 [1]	Active	PDN 2 [2]

[1] Low impedance, no AC signal, and DC bias is almost the same as SG's

[2] Hign impedance

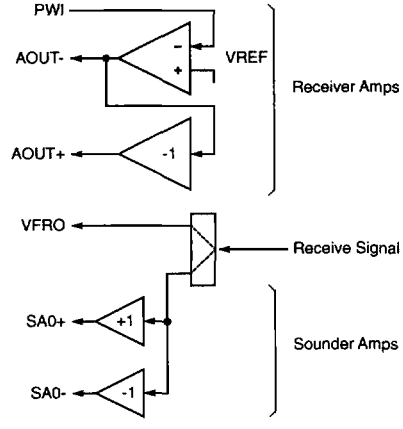


Figure 11. Sounder and Receiver Output Amplifiers

CR1 (ADPCM Block Operation Mode Setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	MODE1	MODE0	TX RESET	RX RESET	TX MUTE	RX MUTE	–	RX PAD
Initial value	0	0	0	0	0	0	0	0

B7, B6

ADPCM data compression algorithm. Set to 0,0 to select 32 Kbps (G.721); set to 0,1 to select 64 Kbps (G.711 through); set to 1,0 to select 24 Kbps (G.723); set to 1,1 to select 16 Kbps (G.726).

B5

Transmit ADPCM reset specified by G.721/G.723/G.726. Set to 1 to select the ADPCM transmit reset.

B4

Receive ADPCM reset specified by G.721/G.723/G.726. Set to 1 to select the ADPCM receive reset.

B3

Transmit ADPCM data mute. Set to 1 to select the ADPCM transmit data mute function.

B2

Receive ADPCM data mute. Set to 1 to select the ADPCM receive data mute function.

B1

Not in use

B0

Receive side PAD. Set to 1 for a 12 dB loss PAD to enter the receive voice path; set to 0 to select no PAD.

CR2 (PCM CODEC Operation Mode Setting and Transmit/Receive Gain Control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial value	0	0	1	1	0	0	1	1

B7

Transmit PCM signal enable. Set to 0 to turn ON the PCM CODEC signal; set to 1 to turn OFF the PCM CODEC signal and transmit PCM idle patterns.

B6, B5, B4

Transmit signal gain control. Refer to the table below for details.

B3

Receive PCM signal enable. Set to 0 to turn ON the PCM signal; set to 1 to turn OFF the PCM signal and receive PCM idle patterns.

B2, B1, B0

Receive signal gain control. These bits control the receive side signal gain control; refer to the table below for details.

Transmit/Receive Gain Setting

B6	B5	B4	Transmit Gain	B2	B1	B0	Receive Gain
0	*0*	*0*	*Transmit gain = -6dB*	*0*	*0*	*0*	*Receive gain = -6dB*
0	0	1	-4dB	0	0	1	-4dB
0	1	0	-2dB	0	1	0	-2dB
0	1	1	0dB	0	1	1	0dB
1	0	0	+2dB	1	0	0	+2dB
1	0	1	+4dB	1	0	1	+4dB
1	1	0	+6dB	1	1	0	+6dB
1	1	1	+8dB	1	1	1	+8dB

The gain setting table indicates the gain of the transmit/receive voice signals, and the transmit of the DTMF and other tones. Tone signal transmits are turned ON by CR4/B6. The gain settings indicate the setup value for the following levels:

- DTMF tone (low group): -16 dBm0
- DTMF tone (high group)/others: -14 dBm0

For example, set the transmit gain setup value to +8dB (B6, B5, B4) = (1,1,1) for the following level of tones to output to PCMSO:

- DTMF tone (low group): -8 dBm0
- DTMF tone (high group)/others: -6 dBm0

The gain of the receive side tone and the gain of the side tone (path from transmit to receive) are set by CR3.

CR3 (Side Tone and Tone Generator Gain Control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	SIDE TONE GAIN2	SIDE TONE GAIN1	SIDE TONE GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial value	0	0	0	0	0	0	0	0

B7, B6, B5

Side tone gain control. These bits set the side tone gain control; refer to the table below for details.

B4

Tone generator enable. Set to 0 to turn OFF the tone generator; set to 1 to turn ON the tone generator.

B3, B2, B1, B0

Tone generator receive gain control. These bits set the receive tone generator gain control to either ON or OFF; refer to the following table for details.

Side Tone Gain Setting

B7	B6	B5	Side Tone Path Gain
0	0	0	Side tone OFF
0	0	1	Gain = -21dB
0	1	0	-19dB
0	1	1	-17dB
1	0	0	-15dB
1	0	1	-13dB
1	1	0	-11dB
1	1	1	-9dB

Receive Tone Generator Gain Setting

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	Tone generator gain = -36dB	1	0	0	0	Gain = -20dB
0	0	0	1	-34dB	1	0	0	1	-18dB
0	0	1	0	-32dB	1	0	1	0	-16dB
0	0	1	1	-30dB	1	0	1	1	-14dB
0	1	0	0	-28dB	1	1	0	0	-12dB
0	1	0	1	-26dB	1	1	0	1	-10dB
0	1	1	0	-24dB	1	1	1	0	-8dB
0	1	1	1	-22dB	1	1	1	1	-6dB

The receive tone generator gain settings are based on the following reference levels:

- DTMF tone (low group): -2 dBm0
- DTMF tone (high group)/others: 0 dBm0

For example, set this gain to -6 dB (B3, B2, B1, B0) = (1,1,1,1) for the following level of tone to output to either SAO+/SAO- or VFRO.

- DTMF tone (low group): -8 dBm0
- DTMF tone (high group)/others: -6 dBm0

CR4 (Tone Generator Operation Mode and Frequency Setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/ OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0
Initial value	0	0	0	0	0	0	0	0

B7

Selects DTMF signals and other tones. Set to 1 to select DTMF signals; set to 0 to select other tones.

B6

Tone transmit enable. Set to 0 to transmit a voice signal; set to 1 to transmit a tone.

B5

Tone receive enable output pin. Set to 0 to select VFRO output; set to 1 to select SAO output.

B4, B3, B2, B1, B0

Tone frequency enable. Refer to *Figure 12* and the following tables for details.

B7 = 1 (DTMF Tone)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0	0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0	1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0	1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz +1 633 Hz
*	0	1	0	0	770 Hz + 1209 Hz	*	1	1	0	0	941 Hz + 1209 Hz
*	0	1	0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1	1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1	1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

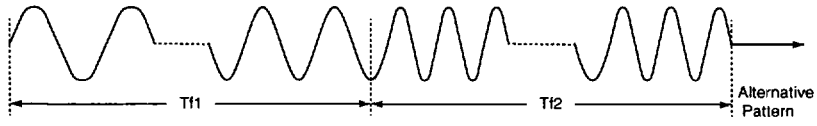
*Unrelated

B7 = 0 (Other Tones – MSM 7570L-01 / MSM7590L-01)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	1k/1333 Hz, 16 Hz mod	1	0	0	0	0	2000 Hz, single tone
0	0	0	0	1	800/667 Hz, 16 Hz mod	1	0	0	0	1	2042 Hz, single tone
0	0	0	1	0	800/1k Hz, 16 Hz mod	1	0	0	1	0	2514 Hz, single tone
0	0	0	1	1	500/667 Hz, 16 Hz mod	1	0	0	1	1	500 Hz, single tone
0	0	1	0	0	500/400 Hz, 16 Hz mod	1	0	1	0	0	667 Hz, single tone
0	0	1	0	1	800/1k Hz, 8 Hz mod	1	0	1	0	1	1333 Hz, single tone
0	0	1	1	0	500/400 Hz, 8 Hz mod	1	0	1	1	0	2100 Hz, single tone
0	0	1	1	1	400 Hz, 16 Hz mod	1	0	1	1	1	–
0	1	0	0	0	400 Hz, 20 Hz mod	1	1	0	0	0	–
0	1	0	0	1	400 Hz, single tone	1	1	0	0	1	–
0	1	0	1	0	425 Hz, single tone	1	1	0	1	0	–
0	1	0	1	1	440 Hz, single tone	1	1	0	1	1	–
0	1	1	0	0	450 Hz, single tone	1	1	1	0	0	–
0	1	1	0	1	800 Hz, single tone	1	1	1	0	1	–
0	1	1	1	0	1000 Hz, single tone	1	1	1	1	0	–
0	1	1	1	1	1300 Hz, single tone	1	1	1	1	1	–

B7 = 0 (Other Tones – MSM 7570L-02 / MSM7590L-02)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	1k/1333 Hz, 16 Hz mod	1	0	0	0	0	2500 Hz, single tone
0	0	0	0	1	800/1k Hz, 16 Hz mod	1	0	0	0	1	2600 Hz, single tone
0	0	0	1	0	800/1k Hz, 16 Hz mod	1	0	0	1	0	2670 Hz, single tone
0	0	0	1	1	400 Hz, 16 Hz mod	1	0	0	1	1	2700 Hz, single tone
0	0	1	0	0	2700 Hz, 16 Hz mod	1	0	1	0	0	2800 Hz, single tone
0	0	1	0	1	400 Hz, single tone	1	0	1	0	1	2910 Hz, single tone
0	0	1	1	0	800 Hz, single tone	1	0	1	1	0	3000 Hz, single tone
0	0	1	1	1	1000 Hz, single tone	1	0	1	1	1	3110 Hz, single tone
0	1	0	0	0	1333 Hz, single tone	1	1	0	0	0	3200 Hz, single tone
0	1	0	0	1	1440 Hz, single tone	1	1	0	0	1	–
0	1	0	1	0	1900 Hz, single tone	1	1	0	1	0	–
0	1	0	1	1	2000 Hz, single tone	1	1	0	1	1	–
0	1	1	0	0	2100 Hz, single tone	1	1	1	0	0	–
0	1	1	0	1	2180 Hz, single tone	1	1	1	0	1	–
0	1	1	1	0	2300 Hz, single tone	1	1	1	1	0	–
0	1	1	1	1	2400 Hz, single tone	1	1	1	1	1	–



8HZ mod.: Tf1 = Tf2 = 62.5 ms
16HZ mod.: Tf1 = Tf2 = 31.25 ms
20HZ mod.: Tf1 = Tf2 = 25 ms

Figure 12. Modulated Timing Waveform

CR5 (Reserved)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0

B7, B6, B5, B4, B3, B2, B1, B0

Not in use

CR6 (VOX Function Control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0
Initial value	0	0	0	0	0	0	0	0

B7

VOX function enable. Set to 1 to turn ON the VOX function; set to 0 to turn OFF the VOX function.

B6, B5

Transmit sound/silent detect VOX function. Set to 0,0 to select -30 dBm0; set to 0,1 to select -35 dBm0; set to 1,0 to select -40 dBm0; set to 1,1 to select -45 dBm0.

B4

Hand over time settings. Set to 0 to select 160 ms; set to 1 to select 320 ms; refer to *Figure 6*, Tvxoff for details.

B3

Receive VOX function. Set to 0 to select internal background noise; set to 1 to select voice signal.

Note: When using this data for control, VOXI must to set to digital "0".

B2

Receive background noise level setting. Set to 0 to select automatic; set to 1 to select programmable by B1 and B0.

Note: The automatic mode is set at the voice signal level when B3 (or VOXI) changes from digital "0" t o "1".

B1, B0

Receive noise level select. Set to 0,0 for no noise; set to 0,1 to select -55 dBm0; set to 1,0 to select -45 dBm0; set to 1,1 to select -35 dBm0.

CR7 (Detection Register, Read Only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	TX LVL1	TX LVL0	–	–	–	–	–
Initial value	0	0	0	[1]	[1]	[1]	[1]	[1]

[1] Used for IC test

B7

Transmit sound/silent detect VOX function. Set to 0 to turn OFF (silent); set to 1 to turn ON (sound) the VOX function.

B6, B5

Transmit signal level indicator. Set to 0,0 to select -60 dBm0* or below; set to 0,1 to select -50 dBm0 to -60 dBm0*; set to 1,0 to select -40 dBm0 to -50 dBm0*; set to 1,1 to select -40 dBm0* and over.

Note: Output is valid only when VOX function is enabled by CR6/B7.

* 0 dBm0 = 3.0 dBm (600 Ω)

B4, B3, B2, B1, B0

Not in use

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rated Value	Unit
Power supply voltage	V_{DD}	-0.3 ~ 5	V
Analog input voltage	V_{AIN}	-0.3 ~ V_{DD}+0.3	
Digital input voltage	V_{DIN}	-0.3 ~ V_{DD}+0.3	
Operating temperature	T_{OP}	-30 ~ +85	°C
Storage temperature	T_{stg}	-55 ~ +150	

Recommended Operating Conditions

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}		+2.7	–	+3.6	V
Operating temperature	T_a		-25	+25	+70	°C
Digital input high voltage	V_{IH}	XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, MCK, $\overline{PDN/RESET}$ DEN, EXCK, DIN	0.45*V_{DD}	–	V_{DD}	V
Digital input low voltage	V_{IL}	XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, MCK, $\overline{PDN/RESET}$, DEN, EXCK, DIN	0	–	0.16*V_{DD}	V
Master clock frequency	FM_{CK1}	MCK (CR0/B6 = "0")	-0.01%	12.288	+0.01%	MHz
	FM_{CK2}	MCK (CR0/B6 = "1")	-0.01%	19.200	+0.01%	
	FM_{CK3}	MCK (CR0/B6 = "0/1")	-0.01%	10.368	+0.01%	
Bit clock frequency	FB_{CK}	BCLK	64	–	2048	kHz
Synchronizing pulse frequency	F_{SYNC}	XSYNC, RSYNC	–	8.0	–	
Bit clock duty cycle	D_C	MCK, BCLK, EXCK	30	50	70	%
Digital input rise time	T_{IR}	XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, MCK, $\overline{PDN/RESET}$, DEN, EXCK, DIN	–	–	50	ns
Digital input fall time	T_{IF}	XSYNC, RSYNC, PCMRI, PCMSI, BCLK, IR, MCK, $\overline{PDN/RESET}$, DEN, EXCK, DIN	–	–	50	ns
Transmit synchronous timing	T_{XS}	BCLK → XSYNC (refer to *Figure 1*)	100	–	–	ns
	T_{SX}	XSYNC → BCLK (refer to *Figure 1*)				
Receive synchronous timing	T_{RS}	BCLK → RSYNC (refer to *Figure 1*)	100	–	–	ns
	T_{SR}	RSYNC → BCLK (refer to *Figure 1*)				
Synchronous signal width	T_{WS}	XSYNC, RSYNC	1BCLK	–	100	µs
PCM, ADPCM setup time	T_{DS}	Refer to *Figure 4* and *Figure 5*	100	–	–	ns
PCM, ADPCM hold time	T_{DH}					
Digital output load	R_{DL}	IS (pull-up resistance)	500	–	–	Ω
	C_{DL}	IS, PCMSO, PCMRO, VOXO, DOUT	–	–	100	pF
By-pass capacitor for SG	C_{SG}	Between SG and AG	10+0.1	–	–	µF
Allowable jitter	J_t	XSYNC, RSYNC, BCLK	–	–	1	ns

DC Characteristics (V_{DD} = 2.7 ~ 3.6V, T_a = -25 ~ +70°C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Power supply current	I_{DD1}	No signal during operation (V_{DD} = 3.0 V)	–	7	14	mA
	I_{DD2}	During power-down (V_{DD} = 3.0 v)	–	0.1	0.2	
Input high level voltage	V_{IH}		0.45*V_{DD}	–	V_{DD}	V
Input low level voltage	V_{IL}		0.0	–	0.16*V_{DD}	
Input high leakage current	I_{IH}	V_I = V_{DD}	–	–	2.0	µA
Input low leakage current	I_{IL}	V_I = 0V	–	–	0.5	
Output high voltage	V_{OH}	I_{OH} = 0.4 mA	0.5*V_{DD}	–	V_{DD}	V
		I_{OH} = 1 µA	0.8*V_{DD}	–	V_{DD}	
Output low voltage	V_{OL}	1LSTTL, pull-up = 500 Ω	0.0	0.2	0.4	
Output leakage current	I_O	IS	–	–	10	µA
Input capacitance	C_{IN}		–	5	–	pF
SG pin output impedance	R_{OSG}	SG	–	25	50	k Ω

Transmit Analog Interface

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Input resistance	R_{INX}	AIN1+, AIN1-, AIN2	10	–	–	MΩ
Output load resistance	R_{LGX}	GSX1, GSX2	20	–	–	kΩ
Output load capacitance	C_{LGX}		–	–	100	pF
Output amplitude	V_{OGX}	GSX1, GSX2, R_L= 20 kΩ	–	–	1.3 [1]	V_{PP}
Offset voltage	V_{OFGX}	Pre op-amps	-20	–	20	mV

[1] -7.7 dBm (600 Ω = 0 dBm0 + 3.14 dBm0 = 1.3 V_{PP}

Receive Analog Interface

Parameter	Symbol	Condition	Rated Value Min	Typ	Max	Unit
Input resistance	R_{INPW}	PWI	10	–	–	MΩ
Output load resistance	R_{LVF}	VFRO	20	–	–	kΩ
	R_{LAO}	AOUT+,AOUT-, SAO+, SAO-	1.2	–	–	
Output load capacitance	C_{LVF}	VFRO	–	–	100	pF
	C_{LAO}	AOUT+, AOUT-, SAO+, SAO-				
Output voltage level	V_{OVF}	VFRO, R_L = 20 kΩ	–	–	1.3 [1]	V_{PP}
	V_{OAO}	AOUT+, AOUT-, SAO+, SAO-				
		Z_L = 350 Ω + 120 nF (refer to *Figure 1*)				
Offset voltage	V_{OFVF}	VFRO	-100	–	100	mV
	V_{OFAO}	AOUT+, AOUT- Gain = 0 dB power amplifier only (refer to *Figure 1*)	-20	–	20	
Op-amp open loop gain	G_{DB}	Power amplifier 0.3 kHz to 3.4 kHz, Z_L = 350 Ω + 120 nF (refer to *Figure 1*)	40	–	–	dB

[1] -7.7 dBm (600 Ω = 0 dBm0 + 3.14 dBm0 = 1.3 V_{PP}

AC Characteristics (V_{DD} = 2.7 ~ 3.6V, T_a = -25 ~ +70°C)

Parameter	Symbol	Condition Frequency (Hz)	Condition Level (dBm0)	Condition Other	Rated Value Min	Typ	Max	Unit
Transmit frequency response	L_{OSS} T1	0 ~ 60	0	–	25	–	–	dB
	L_{OSS} T2	300 ~ 3k			0.15	–	0.20	
	L_{OSS} T3	1020			Reference value			
	L_{OSS} T4	3300			-0.15	–	0.80	
	L_{OSS} T5	3400			00	–	0.80	
	L_{OSS} T6	3968.75			13	–	–	
Receive frequency response	L_{OSS} R1	0 ~ 3000	0	–	-0.15	–	0.20	dB
	L_{OSS} R2	1020			Reference value			
	L_{OSS} R3	3300			-0.15	–	0.80	
	L_{OSS} R4	3400			00	–	0.80	
	L_{OSS} R5	3968.75			13	–	–	
Transmit signal-to-distortion ratio	SD T1	1020	3	[1]	35	–	–	dB
	SD T2		0					
	SD T3		-30					
	SD T4		-40		28	–	–	
	SD T5		-45		23	–	–	

AC Characteristics (V_{DD} = 2.7 ~ 3.6V, T_a = -25 ~ +70°C) (Continued)

Parameter	Symbol	Condition			Rated Value			Unit
		Frequency (Hz)	Level (dBm0)	Other	Min	Typ	Max	
Receive signal-to-distortion ratio	SD R1	1020	3	[1]	35	–	–	dB
	SD R2		0					
	SD R3		-30					
	SD R4		-40		28	–	–	
	SD R5		-45		23	–	–	
Transmit gain tracking	GT T1	1020	3	–	-0.2	–	0.2	dB
	GT T2		-10		Reference value			
	GT T3		-40		-0.2	–	0.2	
	GT T4		-50		-0.5	–	0.5	
	GT T5		-55		-1.2	–	1.2	
Receive gain tracking	GT R1	1020	3	–	-0.2	–	0.2	dB
	GT R2		-10		Reference value			
	GT R3		-40		-0.2	–	0.2	
	GT R4		-50		-0.4	–	0.4	
	GT R5		-55		-1.2	–	1.2	
Idle channel noise	NIDLET	–	AIN = SG	[1]	–	–	-68 (-75.7)	dBm0p (dBmp)
	NIDLER			[1] [2]	–	–	-72 (-79.7)	
Absolute level	AV T	1020	0	GSX2	0.285	0.320 [3]	0.359	V_{RMS}
	AV R			VFRO				
PSRR	PSRR T	0 ~ 50 kHz	50 mV_{PP}	Inband	30	–	–	dB
	SPRR R							
Digital output delay time PCM, ADPCM interface	T_{SDX}	C_L = 1LSTTL + 100 pF Pull-up = 500 Ω (refer to *Figure 4* and *Figure 5*)			00	–	200	ns
	T_{SDR}							
	T_{XD1}/T_{RD1}							
	T_{XD2}/T_{RD2}							
	T_{XD3}/T_{RD3}							

AC Characteristics (V_{DD} = 2.7 ~ 3.6V, T_a = -25 ~ +70°C) (Continued)

Parameter	Symbol	Condition			Rated Value			Unit
		Frequency (Hz)	Level (dBm0)	Other	Min	Typ	Max	
Serial port digital I/O timing characteristic	TM 1	C_L = 100 pF (refer to *Figure 4* and *Figure 5*)			50	–	–	ns
	TM 2				50	–	–	
	TM 3				50	–	–	
	TM 4				50	–	–	
	TM 5				100	–	–	
	TM 6				50	–	–	
	TM 7				50	–	–	
	TM 8				00	–	50	
	TM 9				50	–	–	
	TM 10				50	–	–	
	TM 11				00	–	50	
EXCK clock frequency	F_{EXCK}	–	–	EXCK	–	–	10	MHz

[1] P-message filter is used
[2] PCM input data code
[3] 0.320 V_{RMS} = 0 dBm0 = -7.7 dBm

AC Characteristics – DTMF/Other Tones (V_{DD} = 2.7 ~ 3.6V, T_a = -25 ~ +70°C)

Parameter	Symbol	Condition		Rated Value			Unit
				Min	Typ	Max	
Frequency deviation	Δf_{TONE}	DTMF tones		-7	–	+7	Hz
		Other tones					
Tone reference output level [1] [2]	V_{TL}	Transmit side tones [3]	DTMF (low group), others	-18	-16	-14	dBm0
	V_{TH}		DTMF (high group), others	-16	-14	-12	
	V_{RL}	Receive side tones	DTMF (low group)	-4	-2	0	
	V_{RH}		DTMF (high group), others	-2	0	+2	
DTMF tone level relative value	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		+1	+2	+3	dBm0

[1] Programmable gain setup value is not included
[2] 0 dBm0 = -3.0 dBm (600 Ω)
[3] Transmit tones actually appear in PCM/ADPCM digital format on the chip

AC Characteristics – Gain Settings (V_{DD} = 2.7 ~ 3.6V, T_a = -25 ~ +70°C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Transmit/receive gain setting accuracy	ΔG	For all gain setup values	-1	0	+1	dB

AC Characteristics – VOX Functions (V_{DD} = 2.7 ~ 3.6V, T_a = -25 ~ +70°C)

Parameter	Symbol	Condition		Rated Value			Unit
				Min	Typ	Max	
Transmit VOX detect time (sound, silent detect time)	T_{VXON}	Silent → sound	VOXO pin (refer to *Figure 6*)	–	5	–	ms
	T_{VXOFF}	Sound → silent		150/ 310	160/ 320	170/ 330	
Transmit VOX detect level (sound detect level)	Δ_{VTH}	For detect level setup, value by CR6/B6, CR6/B5		-2.5	0	+2.5	dB