LXT6234

E-Rate Multiplexer

Datasheet

The LXT6234 E-Rate Multiplexer is a single-chip solution for multiplexing four tributary channels into a single high speed data stream and for demultiplexing a high speed data stream back to four tributary channels. All of the necessary circuitry is integrated into the LXT6234 E-Rate Multiplexer; there is no need for an external framing device.

The LXT6234 E-Rate Multiplexer conforms to both the (ITU) G.742 and (ITU) G.751 multiplexing formats defined by the International Telecommunications Union (ITU; formerly known as CCITT): G.742 recommendation for multiplexing four E1 channels into an E2 frame; and the G.751 recommendation for multiplexing four E2 channels into an E3 frame.

The LXT6234 E-Rate Multiplexer also encodes and decodes HDB3 zero suppression line coding used on E1, E2, and E3 signals. The coder and decoder input/output pins are externally accessible, allowing either HDB3 or NRZ (non-return-to-zero) I/O to the multiplexer. The LXT6234 E-Rate Multiplexer can also serve as a five channel HDB3 coder and decoder.

Applications

- E1/E2 Multiplexer (2/8 Mbit/s)
- E2/E3 Multiplexer (8/34 Mbit/s)
- E1/E3 Multiplexer (2/34 Mbit/s)
- Digital Loop Carrier (DLC) Terminal
- Add / Drop Multiplexers (ADM)
- 4 - to - 1 Non-Standard Multiplexer

Product Features

- Performs four-E1 to one-E2, or four-E2 to one-E3 multiplexing. Five ICs will implement a sixteen-E1 to one-E3 multiplexer.
- Fully compliant with the G.742 and G.751 ITU recommendations. Fully compliant with G.703 when used with LXT305/332 Line Interface.
- A robust frame-acquisition and frame-holding algorithm minimizes frame slippage, acquires and holds frame below 10^{-2} bit error rate.
- Four auxiliary low speed data or flag channels are available via the Stuffing Bits on each tributary channel.
- Access to the Alarm bit and the National bit. These can be used as recommended by ITU or for proprietary use.
- Five independent HDB3 CODECs allow multiplexer I/O in either HDB3 or NRZ formats. The LXT6234 can also function as a stand alone five-channel HDB3 transcoder.

As of January 15, 2001, this document replaces the Level One document *LXT6234 E-Rate Multiplexer Datasheet*.

Order Number: 249301-001
January 2001

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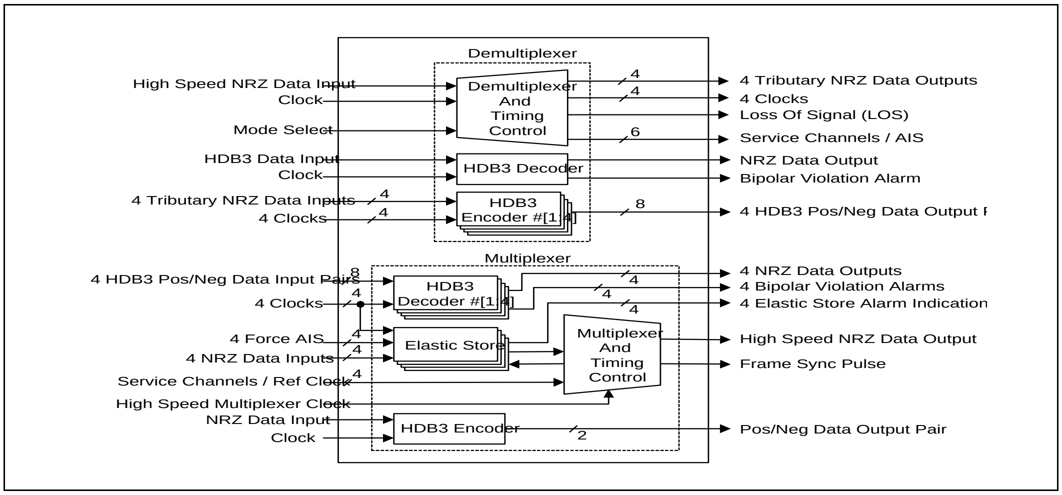
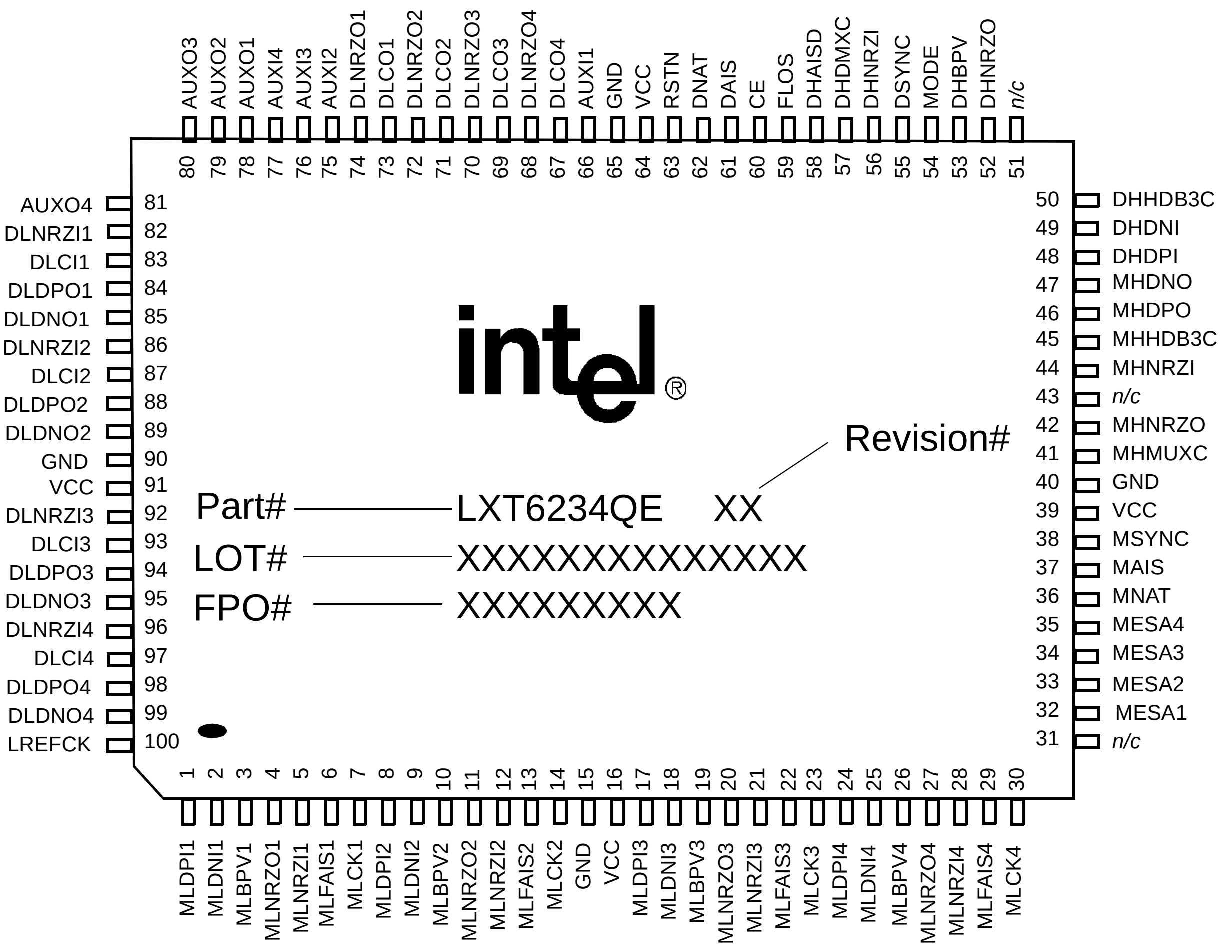


2.0 Conscription

Figure 2. LXT6234 Pin Assignment



Package Topside Markings

Marking	Definition
Part #	LXT6234 is the unique identifier for this product family. QE indicates the family member.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Input Signals

Pin #	Sym	Description
1	MLDPI1	HDB3 Decoder #1 Positive Data Input. HDB3 Decoder #1 positive rail input clocked on the positive transitions of the clock signal MLCK1.
2	MLDNI1	HDB3 Decoder #1 Negative Data Input. HDB3 Decoder #1 negative rail input clocked on the positive transitions of the clock signal MLCK1.
8	MLDPI2	HDB3 Decoder #2 Positive Data Input. HDB3 Decoder #2 positive rail input clocked on the positive transitions of the clock signal MLCK2.
9	MLDNI2	HDB3 Decoder #2 Negative Data Input. HDB3 Decoder #2 negative rail input clocked on the positive transitions of the clock signal MLCK2.
17	MLDPI3	**HDB3 Decoder #3 Positive Data Input.** HDB3 Decoder #3 positive rail input clocked on the positive transitions of the clock signal MLCK3.
18	MLDNI3	**HDB3 Decoder #3 Negative Data Input.** HDB3 Decoder #3 negative rail input clocked on the positive transitions of the clock signal MLCK3.
24	MLDPI4	**HDB3 Decoder #4 Positive Data Input.** HDB3 Decoder #4 positive rail input clocked on the positive transitions of the clock signal MLCK4.
25	MLDNI4	**HDB3 Decoder #4 Negative Data Input.** HDB3 Decoder #4 negative rail input clocked on the positive transitions of the clock signal MLCK4.
7	MLCK1	**Multiplexer Tributary #1 Clock Input.** Clock input for Multiplexer side tributary channel #1. This clock is used by both the associated HDB3 decoder and the Multiplexer. For standard rate applications, this clock must have a frequency of ±50 ppm for 2048 kbit/s operation and ±30 ppm for the 8448 kbit/s operation as per ITU G.703.
14	MLCK2	**Multiplexer Tributary #2 Clock Input.** Idem as MLCK1 with tributary #2 in.
23	MLCK3	**Multiplexer Tributary #3 Clock Input.** Idem as MLCK1 with tributary #3 in.
30	MLCK4	**Multiplexer Tributary #4 Clock Input.** Idem as MLCK1 with tributary #4 in.
5	MLNRZI1	**Multiplexer Tributary #1 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK1.
12	MLNRZI2	**Multiplexer Tributary #4 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK2.
21	MLNRZI3	**Multiplexer Tributary #3 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK3.
28	MLNRZI4	**Multiplexer Tributary #4 NRZ Data Input.** Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK4.
6	MLFAIS1	**Force AIS on Multiplexer Tributary #1.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #1.
13	MLFAIS2	**Force AIS on Multiplexer Tributary #2.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #2.
22	MLFAIS3	**Force AIS on Multiplexer Tributary #3.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #3.
29	MLFAIS4	**Force AIS on Multiplexer Tributary #4.** Active high signal to force AIS (all 1's) data and LREFCK clock on Multiplexer tributary #4.
66	AUXI1	**Auxiliary Flag/Data #1 Input.** The signal on this pin is clocked into the frame at the stuffing bit location (J1) when justification is such that tributary data is NOT placed at this location. A high on alarm signal MESA1 indicates this condition during the current frame.
75	AUXI2	**Auxiliary Flag/Data #2 Input.** See AUXI1 Description. MESA2 is relevant indication signal.
76	AUXI3	**Auxiliary Flag/Data #3 Input.** See AUXI1 Description. MESA3 is relevant indication signal.
77	AUXI4	**Auxiliary Flag/Data #4 Input.** See AUXI1 Description. MESA4 is relevant indication signal.

Table 1. Input Signals (Continued)

Pin #	Sym	Description
36	MNAT	**National Bit Input.** National Bit input that is placed in the 12th bit of the frame as per ITU G.742, G.751 specifications.
37	MAIS	**AIS/Error Bit Input.** AIS Bit input that is placed in the 11th bit of the frame, as per ITU G.742, G.751 specifications.
41	MHMUXC	**High speed Multiplexer Clock Input.** Clock input for Multiplexer functions and NRZ high speed data output. For standard rate applications, this clock must have a frequency of ±30 ppm for the 8448 kbit/s operation and ±20 ppm for the 34368 kbit/s operation as per ITU G.703.
44	MHNRZI	**HDB3 Encoder #5 NRZ Input.** HDB3 Encoder #5 (High speed) NRZ input clocked on the rising edge of MHHDB3C.
45	MHHDB3C	**HDB3 Encoder #5 Clock Input.** When used in conjunction with the Multiplexer, this pin should be tied to the high speed Multiplexer Clock, MHMUXC, P41.
48	DHDPI	**HDB3 Decoder #5 Positive Data Input.** HDB3 Decoder #5 (High Speed) positive rail input clocked on the rising edge of DHHDB3C.
49	DHDNI	**HDB3 Decoder #5 Negative Data Input.** HDB3 Decoder #5 (High Speed) positive rail input clocked on the rising edge of DHHDB3C.
50	DHHDB3C	**HDB3 Decoder #5 Clock Input.** When used in conjunction with the Demultiplexer, this pin should be tied to the high speed Demultiplexer Clock, DHMUXC, P57.
56	DHNRZI	**Demultiplexer NRZ Data Input.** Demultiplexer NRZ input clocked on rising edge of DHDMXC.
57	DHDMXC	**High speed Demultiplexer Clock Input.** Clock input for Demultiplexer functions and NRZ high speed data in. For standard rate applications, this clock must have a frequency of ±30 ppm for the 8448 kbit/s operation and ±20 ppm for the 34368 kbit/s operation as per ITU G.703.
82	DLNRZI1	**HDB3 Encoder #1 NRZ Data Input.** HDB3 Encoder #1 NRZ input clocked on rising edge of DLCI1.
86	DLNRZI2	**HDB3 Encoder #2 NRZ Data Input.** HDB3 Encoder #2 NRZ input clocked on rising edge of DLCI2.
92	DLNRZI3	**HDB3 Encoder #3 NRZ Data Input.** HDB3 Encoder #3 NRZ input clocked on rising edge of DLCI3.
96	DLNRZI4	**HDB3 Encoder #4 NRZ Data Input.** HDB3 Encoder #4 NRZ input clocked on rising edge of DLCI4.
83	DLCI1	**HDB3 Encoder #1 Clock Input.** Clock input for HDB3 Encoder #1.
87	DLCI2	**HDB3 Encoder #2 Clock Input.** Clock input for HDB3 Encoder #2.
93	DLCI3	**HDB3 Encoder #3 Clock Input.** Clock input for HDB3 Encoder #3.
97	DLCI4	**HDB3 Encoder #4 Clock Input.** Clock input for HDB3 Encoder #4.
54	MODE	**E12/E23 Mode Select.** Mode selection for multiplexer/demultiplexer operation. A low signal selects 4E1/E2 multiplexing. A high signal selects 4E2/E3 multiplexing.
100	LREFCK	**Tributary Reference Clock.** This clock is used as a reference for the Force AIS functions (See Pin 6 Description). For standard rate applications, this clock must have a frequency of ±50 ppm for the 2048 kbit/s operation and ±30 ppm for the 8448 kbit/s operation as per ITU G.703.
60	CE	**Chip Enable.** A high signal forces all outputs into tri-state; used for PCB Testing. This signal should be low for normal operation.
63	RSTN	**Reset.** An active low reset pin. Must be pulsed low on power up to initialize all internal circuits after V_{CC} and clocks are stable.
15, 40 65, 90	GND	**Ground.** Ground Reference.
16, 39 64, 91	V_{CC}	**Voltage.** 5-volt supply voltage.

Table 2. Output Signals

Sym	Pin #	Description
MLNRZO1	4	**HDB3 Decoder #1 NRZ Output.** HDB3 Decoder #1 NRZ output clocked on the rising edge of MLCK1.
MLNRZO2	11	**HDB3 Decoder #2 NRZ Output.** HDB3 Decoder #2 NRZ output clocked on the rising edge of MLCK2.
MLNRZO3	20	**HDB3 Decoder #3 NRZ Output.** HDB3 Decoder #3 NRZ output clocked on the rising edge of MLCK3.
MLNRZO4	27	**HDB3 Decoder #4 NRZ Output.** HDB3 Decoder #4 NRZ output clocked on the rising edge of MLCK4.
MLBPV1	3	**HDB3 Decoder #1 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MLBPV2	10	**HDB3 Decoder #2 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MLBPV3	19	**HDB3 Decoder #3 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MLBPV4	26	**HDB3 Decoder #4 Bipolar Violation Alarm.** This open collector output pulses every time a bipolar violation occurs in the decoding process.
MESA1	32	**Multiplexer Tributary #1 Elastic Store Alarm Indication.** Multiplexer justification status for tributary #1. A high indicates bit stuffing on the current frame. A low indicates an information bit. When externally filtered, this signal can be used to indicate elastic store failure or incorrect tributary frequency.
MESA2	33	**Multiplexer Tributary #2 Elastic Store Alarm Indication.** Idem as MESA1 with tributary channel 2.
MESA3	34	**Multiplexer Tributary #3 Elastic Store Alarm Indication.** Idem as MESA1 with tributary channel 3.
MESA4	35	**Multiplexer Tributary #4 Elastic Store Alarm Indication.** Idem as MESA1 with tributary channel 4.
MHNRZO	42	**High speed Multiplexer NRZ Output.** Multiplexer NRZ data clocked out on the rising edge of MHMUXC.
MHDPO	46	**HDB3 Encoder #5 Positive Data Output.** HDB3 Encoder #5 Positive rail clocked out on the rising edge of MHHDB3C.
MHDNO	47	**HDB3 Encoder #5 Negative Data Output.** HDB3 Encoder #5 Negative rail clocked out on the rising edge of MHHDB3C.
DLNRZO1	74	**Demux Tributary #1 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO1.
DLNRZO2	72	**Demux Tributary #2 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO2.
DLNRZO3	70	**Demux Tributary #3 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO3.
DLNRZO4	68	**Demux Tributary #4 NRZ Output.** This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO4.
DLCO1	73	**Demux Tributary #1 Clock Output.** Demultiplexer side recovered clock of tributary #1. This clock has a duty cycle of 75% and is gapped at points in the frame where tributary data is not present (i.e., frame word). The maximum gap is 3 clocks at the frame word location. The frequency will match that of the far end multiplexer tributary input. This signal is clocked out on the rising edge of DHDMXC.
DLCO2	71	**Demux Tributary #2 Clock Output.** Demultiplexer side recovered clock of tributary #2. See DLCO1 description.
DLCO3	69	**Demux Tributary #3 Clock Output.** Demultiplexer side recovered clock of tributary #3. See DLCO1 description.
DLCO4	67	**Demux Tributary #4 Clock Output.** Demultiplexer side recovered clock of tributary #4. See DLCO1 description.
DLDPO1	84	**HDB3 Encoder #1 Output +.** HDB3 Encoder #1 positive rail output clocked out on the rising edge of DLCI1.

Table 2. Output Signals (Continued)

Sym	Pin #	Description
DLDNO1	85	**HDB3 Encoder #1 Output -.** HDB3 Encoder #1 negative rail output clocked out on the rising edge of DLCI1.
DLDPO2	88	**HDB3 Encoder #2 Output +.** HDB3 Encoder #2 positive rail output clocked out on the rising edge of DLCI2.
DLDNO2	89	**HDB3 Encoder #2 Output -.** HDB3 Encoder #2 negative rail output clocked out on the rising edge of DLCI2.
DLDPO3	94	**HDB3 Encoder #3 Output +.** HDB3 Encoder #3 positive rail output clocked out on the rising edge of DLCI3.
DLDNO3	95	**HDB3 Encoder #3 Output -.** HDB3 Encoder #3 negative rail output clocked out on the rising edge of DLCI3.
DLDPO4	98	**HDB3 Encoder #4 Output +.** HDB3 Encoder #4 positive rail output clocked out on the rising edge of DLCI4.
DLDNO4	99	**HDB3 Encoder #4 Output -.** HDB3 Encoder #4 negative rail output clocked out on the rising edge of DLCI4.
DHNRZO	52	**HDB3 Decoder #5 NRZ Data Output.** HDB3 Decoder #5 NRZ data clocked out on the rising edge of DHHDB3C.
DHBPV	53	**HDB3 Decoder #5 Bipolar Violation Alarm.** This active high signal pulses every time a bipolar violation occurs in the decoding process.
AUXO1	78	**Auxiliary Flag/Data #1 Output.** Auxiliary Data #1 output that contains data value input on AUXI1. See AUXI1 Description.
AUXO2	79	**Auxiliary Flag/Data #2 Output.** Auxiliary Data #2 output that contains data value input on AUXI2. See AUXI1 Description.
AUXO3	80	**Auxiliary Flag/Data #3 Output.** Auxiliary Data #3 output that contains data value input on AUXI3. See AUXI1 Description.
AUXO4	81	**Auxiliary Flag/Data #4 Output.** Auxiliary Data #4 output that contains data value input on AUXI4. See AUXI1 Description.
DNAT	62	**National Bit Output.** Updated every frame based on the contents of the 12th bit in the frame as per ITU G.742, G.751
DHAISD	58	**Demultiplexer Input AIS Detect.** Active high alarm occurs when an all 1's condition (AIS) is detected at the DHNRZI input. This alarm will not occur if the input is a framed signal (i.e. all tributaries are AIS on multiplexer side).
FLOS	59	**Demultiplexer Loss of Frame Alarm.** Active high Frame Loss Alarm that occurs when the Demux has not detected the Frame word.
MSYNC	38	**Multiplexer Frame Sync Pulse.** Pulse of one high speed clock cycle synchronous with the last bit of the frame (just before the frame word of the next frame).
DSYNC	55	**Dmx Frame Sync Pulse.** Pulse of one high speed clock cycle synchronous with the first bit of the frame word of the high speed incoming signal.
DAIS	61	**AIS Error Bit Output.** Updated every frame based on the contents of the 11th bit in the frame as per ITU G.742 and G.751.
NC	31, 43 51	**Not Connected.** These pins must be left unconnected.

3.0 Functional Description

The LXT6234 E-Rate Multiplexer consists of a multiplexer block, a demultiplexer block, five HDB3 decoders, and five HDB3 encoders. If the HDB3 codecs are used, the signal flow would be as follows:

Multiplexer: Four tributaries of data feed HDB3 decoders one through four. The NRZ outputs of the decoders are connected to the multiplexer tributary inputs. Within the multiplexer, the justification or stuffing for each tributary is determined; the frame word is added; and the high speed NRZ data sent out. The multiplexer output is connected to HDB3 encoder five where it is encoded and sent out as Positive Data Output (MHDPO) and Negative Data Output (MHDNO).

Demultiplexer: High speed encoded data feeds the HDB3 decoder five and is output as NRZ data. The decoder output is connected to the demultiplexer input where it enters both the frame search circuitry and the demultiplexing circuitry. Once the frame is detected, the NRZ data is demultiplexed into the four tributaries and the justification is removed. Tributary data is then sent out in NRZ format. These tributary outputs, both Clock Output (DLCO*x*) and NRZ Output (DLNRZO*x*), are connected to HDB3 encoders one through four, encoded, and output as Positive Data (MHDPO) and Negative Data (MHDNO).

3.1 Frame Format

The multiplexer and demultiplexer share the Mode Select (MODE) control pin. When MODE is low, the multiplexer conforms to the ITU G.742 format for four-E1 to E2 (Figure 4). An E2 frame is 848 bits long, with 205 data bits and one justification bit for each E1 tributary. When MODE is high, the multiplexer conforms to the ITU G.751 format for four-E2 to E3 (Figure 5). This E3 frame is 1536 bits long, with 377 data bits and one justification bit for each E2 tributary.

In both E2 and E3 formats, there are two flag bits per frame: the AIS bit and the National bit. The four justification bits may also be used as additional flag bits.

3.2 HDB3 Codecs

Five HDB3 codecs are included within the LXT6234 to allow easy integration with a wide range of line interface circuits. There are four low speed codecs for the tributary streams and one high speed codec to process the high speed output data. All five codecs are identical and all I/O pins are externally accessible for each device. All codecs can be operated at the maximum operating speed if the chip is used as a stand alone HDB3 transcoder. Note that the "low speed" decoders share a clock with the multiplexer tributary clocks.

Each HDB3 decoder is provided with Positive Data, Negative Data, and clock; they decode the data into a single NRZ bit stream. The HDB3 encoders are provided with NRZ data and clock; they produce the Positive Data and Negative Data bit streams.

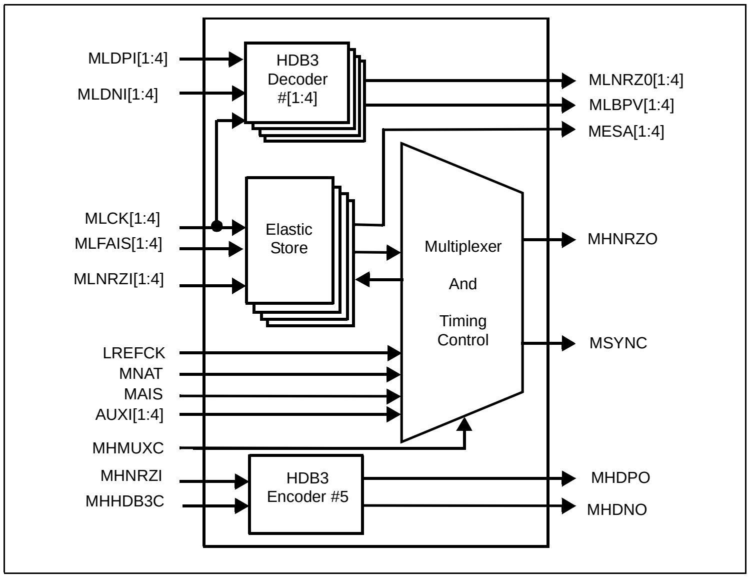
3.3 HDB3 Decoder Alarms

A Bipolar Violation Alarm (MLBPV*x*, DHBPV) associated with each HDB3 decoder indicate detection of a coding violation error within the data. Coding violations include Bipolar Violations, a string of more than four zeros in a row, or encoding violations. The active high alarm is one clock cycle in duration.

3.4 Multiplexer

The multiplexer formats four low speed NRZ tributaries into a single high speed bit stream (Figure 3). Tributary data rates are synchronized via internal elastic store memories using a positive justification process as specified in the ITU recommendations.

Figure 3. Multiplexer Side Block Diagram



Data enters a first-in/first-out (FIFO) elastic store block. The FIFO receives the data along with the tributary clock and a pointer generated from the timing control. The output of the elastic store block is clocked by the tributary enable pulses from the timing control, and the data is finally processed by the multiplexer. Processing normally places the output data bit into the high speed bit stream during the tributary enable. An once-per-frame exception occurs during justification. During this event the location of the pointer in the FIFO is determined and a decision made for justification. If the elastic store is less than half full, a justification bit (used for the auxiliary flag channels) is placed in the bit stream and the MESA*x* pin is set high. When the elastic store becomes over half full, a tributary bit is clocked out from the FIFO, placed in the bit stream, and the MESA*x* pin set low. There are three justification indicators spread throughout the frame to show the status of the justification bit to the demultiplexer. Finally, the National and AIS bits are added at the beginning of each frame, and the bit stream is clocked out on MHNRZO.

The multiplexer timing control receives a high speed clock and generates the frame structure and timing control according to the bit length of each frame. This is 848 bits for an E2 frame, and 1536 bits for an E3 frame. MODE provides for either E2 or E3 selection.

In case of tributary transmission failure or the loss of a signal, tributary data can be forced to an all 1's state. For each tributary this function is controlled at the MLFAIS*x* pin.

Figure 4. E2 Frame

213 217

J1	J2	J3	J4	208 E1

425 429

J1	J2	J3	J4	208 E1

637 641 645

J1	J2	J3	J4	S1	S2	S3	S4	204 E1

4xE1	Tributaries Data	205 x 4	820
F1...F10	Frame Bits	1 x 10	10
J1...J4	Justification Ind.	4 x 3	12
S1...S4	Justification Bits		
	Auxiliary Bits	1 x 4	4
AIS	Alarm Bit	1 x 1	1
NAT	National Bit	1 x 1	1
	Total		848

Figure 5. E3 Frame

F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	AIS	NAT	372 E2

385 389

J1	J2	J3	J4	380 E2

769 773

J1	J2	J3	J4	380 E2

1153 1157 1161

J1	J2	J3	J4	S1	S2	S3	S4	376 E2

4xE2	Tributaries Data	377 x 4	1508
F1...F10	Frame Bits	1 x 10	10
J1...J4	Justification Ind.	4 x 3	12
S1...S4	Justification Bits		
	Auxiliary Bits	1 x 4	4
AIS	Alarm Bit	1 x 1	1
NAT	National Bit	1 x 1	1
	Total		1536

3.4.1 Flag Bits

Two flag bits, defined as the National Bit (MNAT) and AIS/Error Bit (MAIS) are transmitted with each frame. At the appropriate time the bit values of the MNAT and MAIS inputs are inserted into the frame. There are also four auxiliary flag channels available (AUXI*x*) that use the justification bit. These flags are placed in the frame approximately 40% of the time, depending on the ratio of the tributary clock to the multiplexer clock. A high on MESA*x* indicates that the AUXI*x* flag will be inserted into the current frame.

3.4.2 Multiplexer Alarms

An indicator bit (MESAx) for each tributary monitors the status of the elastic store memory. This pin provides the justification status of the tributary. Under normal conditions this pin toggles at the frame rate with a 40% duty cycle. Large variation of the duty cycle indicates the tributary clock frequency is out of specification. Loss of clock would cause MESA to assume a rail value.

For use as a frequency alarm this signal should be filtered by a single-pole RC filter far below the frame frequency, and connected to a pair of voltage comparators. The unfiltered alarm signal can be used to clock the auxiliary data channel inputs.

3.5 Demultiplexer

Data entering the demultiplexer is sent to both the demultiplexing block and the framer. The framer, using a Sieve algorithm, examines the incoming data to find the framing word. A frame is declared found when three passes show the frame word has been found at the same location within the frame. The timing module is then synchronized to the incoming data frame and the Frame Loss Alarm turns off.

Valid tributary data can be extracted after the frame is found. For each tributary, three justification indicator bits are stored. A majority-rule determination decides whether the justification bit is sent as tributary data (with clock) or as an auxiliary bit (with no clock).

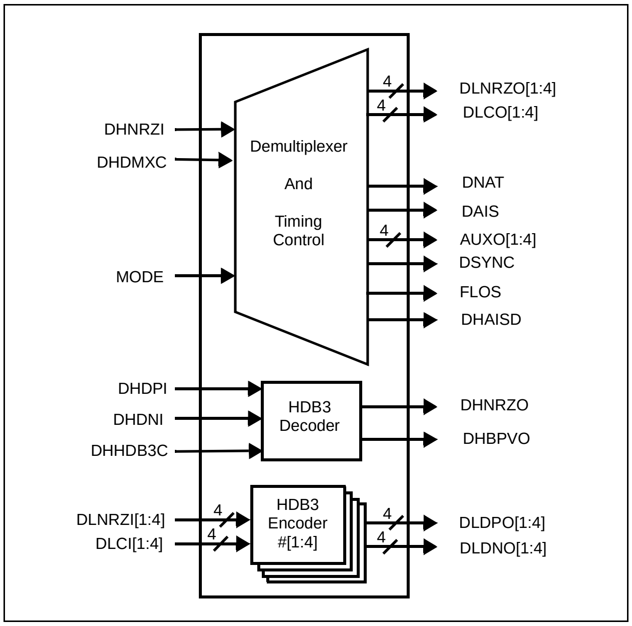
The DNAT and DAIS flag bits are updated for each frame and sent to their dedicated pins. The auxiliary flag bits AUXO*x* are updated when they are available on the frame.

3.5.1 Demultiplexer Alarms

The demultiplexer has two active-high alarms: Frame Loss (FLOS), and Demultiplexer Input AIS Detect (DHAISD).

- FLOS is active at power-up and clears after three consecutive frames are detected. During normal operation FLOS becomes active after missing four consecutive frames.
- DHAISD activates after 768 consecutive 1’s pass through the high speed NRZ data stream. DHAISD will occasionally glitch if four tributaries are all 1’s and the justification of all four channels is identical. This glitch is filtered with a single-pole RC filter.

Figure 6. Demultiplexer Side Block Diagram



4.0 Glossary

AIS Alarm Indication Signal.

AMI Alternate Mark Inversion.

CCITT Consultative Committee for International Telegraph and Telephone (now called the International Telecommunications Union - ITU).

CODEC COder/DECoder; An assembly comprising an encoder and a decoder within the same unit.

HDB3 High Density Bipolar code of order 3, extension of AMI.

E1 The primary European digital rate of 2.048 MHz, or thirty-two 64 KB channels.

E2 The secondary European rate, four E1 channels at 8.448 MHz.

E3 The tertiary European rate, four E2 channels at 34.368 MHz.

FIFO First-in/First-Out Memory.

ITU International Telecommunications Union.

NRZ Non-Return to Zero.

PCB Printed Circuit Board.

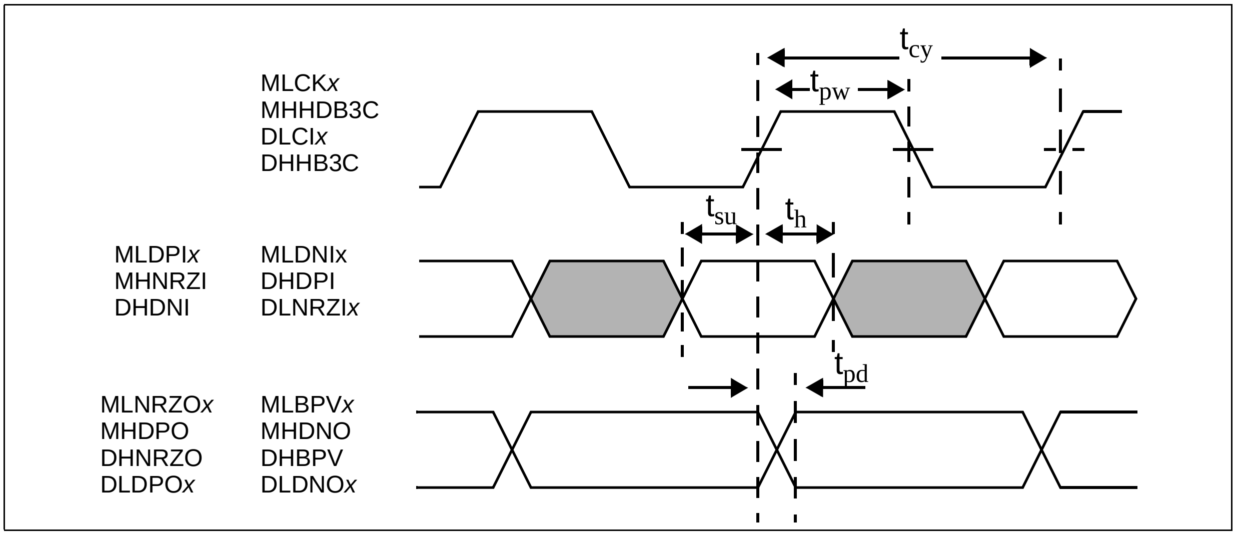
RZ Return to Zero.

5.0 Application Information

5.1 E1/E3 Multiplexer Block Diagram

Figure 7 is a block diagram of the E1/E3 Multiplexer.

Figure 7. E1/E3 Multiplexer Block Diagram



5.1.1 E1 Line Interface

- Receive clocks from the pulse data.
- Pass either HDB3 encoded signals to the E-Rate Multiplexer as clock and RZ data or as NRZ data[1]. (Both positive and negative RZ data.)

5.1.2 LXT6234, E1/E2 Stage

- The LXT6234 may interface with either HDB3 or non-HDB3 coded signals. Data from an LIU that does not perform HDB3 decoding must be connected to the HDB3 inputs on the LXT6234. These are the clock (MLCK*x*) and decoder data input signals (both positive - MLDP*x* and negative - MLDN*x*). When receiving data from an LIU which does perform HDB3 decoding, the NRZ data is connected to the MLNRZx input and the clock connects to the MLCK*x* in on the LXT6234
- The four tributaries are interleaved into a single, intermediary E2 rate data stream. An on-board crystal oscillator drives the data output frequency from the mux at the E2 rate of 8.448 MHz. A bit stuffing algorithm implemented in the LXT6234 ensures tributary rate integrity at the output. The LXT6234 contains elastic store buffers to manage bit-stuffing process.
- The NRZ data is sent to a tributary of the E-Rate Multiplexer, stage E2/E3.

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1. If the HDB3 decoder is on the line interface unit (LIU).

5.1.3 LXT6234, E3 Stage

- The multiplexer portion of the LXT6234 interleaves four asynchronous E2 rate NRZ data streams into a single E3 data stream. Depending on the configuration, either an on-board crystal oscillator or an external reference clock drives the data output frequency from the mux at the rate of 34.368 Mbps. The bit stuffing algorithm implemented in the LXT6234 ensures tributary rate integrity at the output.
- If the LIU provides HDB3 encoding, then the NRZ data and clock are passed to the E3 line interface.
- If the LIU does not provide HDB3 encoding, then encoding is done by the LXT6234 and data is output as positive and negative data. An activity monitor provides tributary fail notification when necessary.

See Application Note 9501 for additional information.

6.0 Test Specifications

Note: Minimum and maximum values in Tables 3 through 9 and Figure 8 through Figure 12 represent the performance specifications of the LXT6234 E-Rate Multiplexer and are guaranteed by test except, where noted, by design.
Typical values are not subject to production testing.

The LXT6234 E-Rate Multiplexer, fabricated with 0.8-micron CMOS technology, is currently available in a 100-pin plastic quad flat pack package (EIAJ standard 100PQFP). All device I/O comply with 5V CMOS standards. A list of input and output signals is provided with this data sheet. There are 46 input signals and 43 output signals. In addition, there are four V_{CC} power pins and four Ground power pins.

A Chip Enable is provided to facilitate board level, in-circuit testing during the PCB manufacturing process. The LXT6234 E-Rate Multiplexer is fully tested before shipment.

Table 3. Absolute Ratings

Parameter	Symbol	Min	Max	Units
DC Supply Voltage	V_{DD}	-0.3	7.0	V
Input Voltage	V_{IN}	0	V_{DD}+ 0.3	V
Input Current	I_{IN}	—	10	µA
Ambient Operating Temperature	T_{AM}	-40	+85	°C
Storage Temperature	T_{STG}	-55	+150	°C
CAUTION: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.				

Table 4. DC Characteristics (TA=-40 to +85×C, Vdd=+5V±5%, GND=0 V)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
High level input voltage	V_{IH}	$0.7V_{DD}$	—	—	V	V_{DD}=5V±5V
Low level input voltage	V_{IL}	—	—	$0.3V_{DD}$	V	CMOS
High level output voltage	V_{OH}	2.4	4.5	—	V	IOH = Rated Current
Low level output voltage	V_{OL}	—	0.2	0.4	V	IOL = Rated Current
Input Current	I_{IN}	-10	1	10	µA	VIN = VDD, VSS
TriState leakage current	I_{OZ}	-10	1	10	µA	VOH = VDD or VSS
Power dissipation 4E1/E2 mode 4E2/E3 mode	PD		 100 500		 mW mW	 VDD = 5.25 V1 VDD = 5.25 V
Static current	I_{DD}	—	1	20	µA	VDD = 5.25 V

7.0 AC Timing Specifications

Note: Unless otherwise specified, all timing specifications are referenced at ambient condition as $T_{Ambient}$ = -40° to 85°C, VDD =+5V±5%, GND = 0V.

Figure 8. HDB3 Encoder and Decoder Timing (Refer to Table 5)

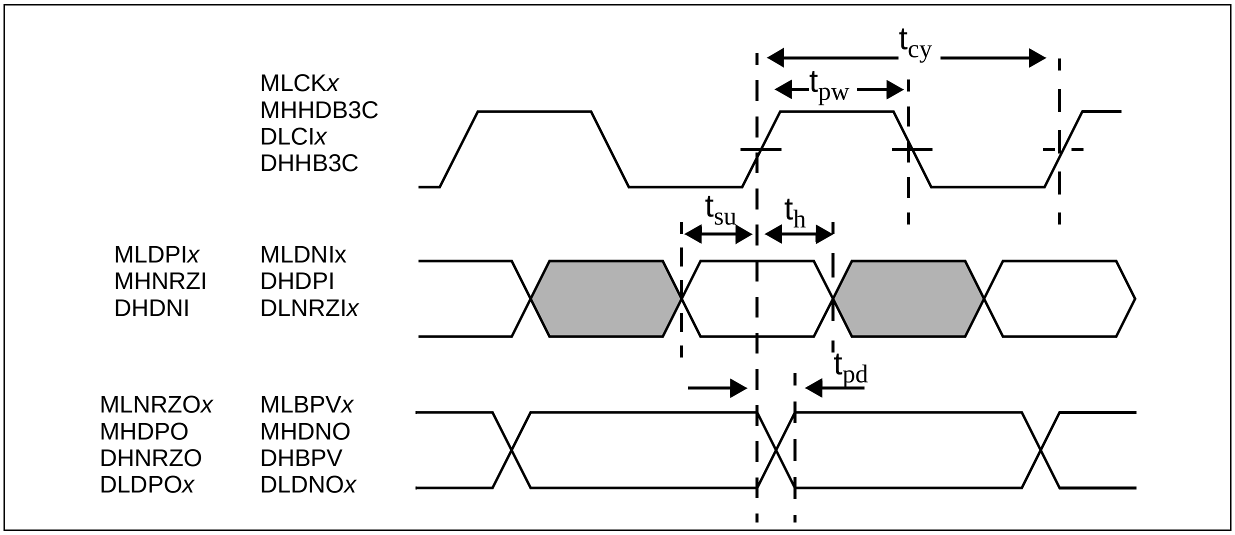

Table 5. HDB3 Encoder and Decoder (Refer to Figure 8)

Parameter	Symbol	Min	Typ	Max	Unit
Clock duty cycle	tPWH	40	—	75	%
Data to clock setup time	tSU	5	—	—	ns
Data to clock hold time	tH	6	—	—	ns
Clock to data propagation time (50pF capacitive load)	tPD	—	15	25	ns

Figure 9. Multiplexer Tributary Input Timing (Refer to Table 6)

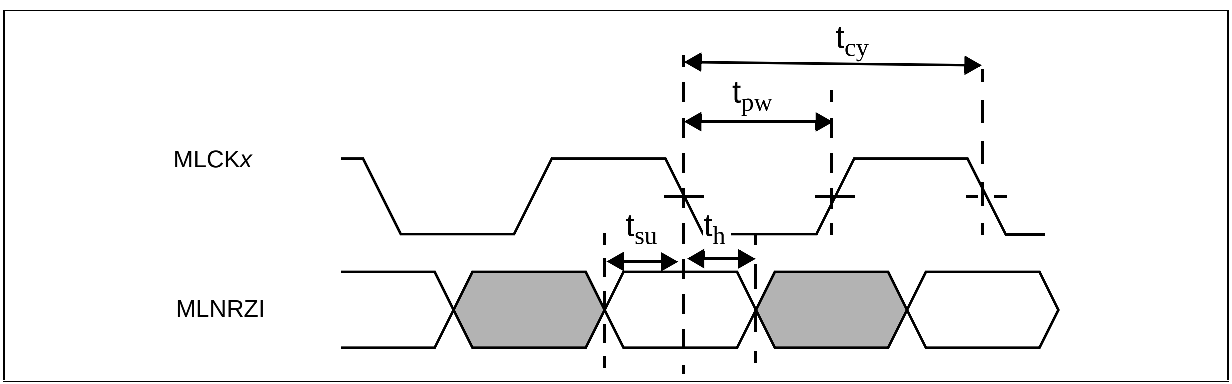

Table 6. Multiplexer Tributary Input (Refer to Figure 9)

Parameter	Symbol	Min	Typ	Max	Unit
Clock duty cycle	t_{PWH}	40	—	60	%
Data to clock setup time (falling edge)	t_{SU}	5	—	—	ns
Data to clock hold time (falling edge)	t_H	5	—	—	ns

Figure 10. High Speed Multiplexer Input & Output Timing (Refer to Table 7)

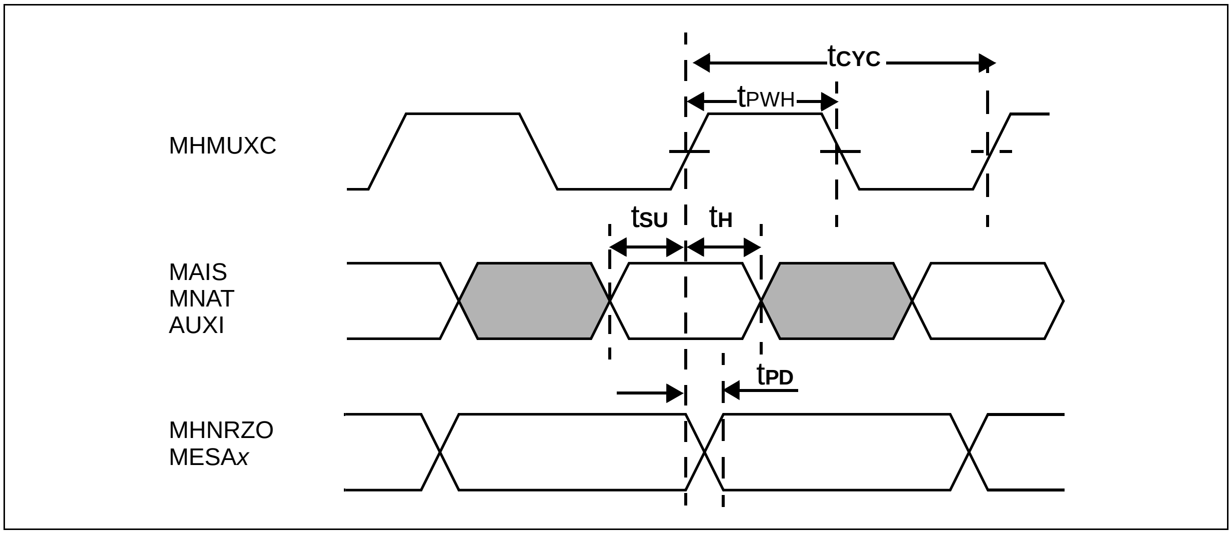

Table 7. High Speed Multiplexer Input & Output (Refer to Figure 10)

Parameter	Symbol	Min	Type	Max	Unit
Clock duty cycle	t_{PWH}	40	—	60	%
Data to clock setup time	t_{SU}	5	—	—	ns
Data to clock hold time	t_H	6	—	—	ns
Clock to data propagation time	t_{PD}	—	20	30	ns

Figure 11. High Speed Demultiplexer Input & Output Timing (Refer to Table 8)

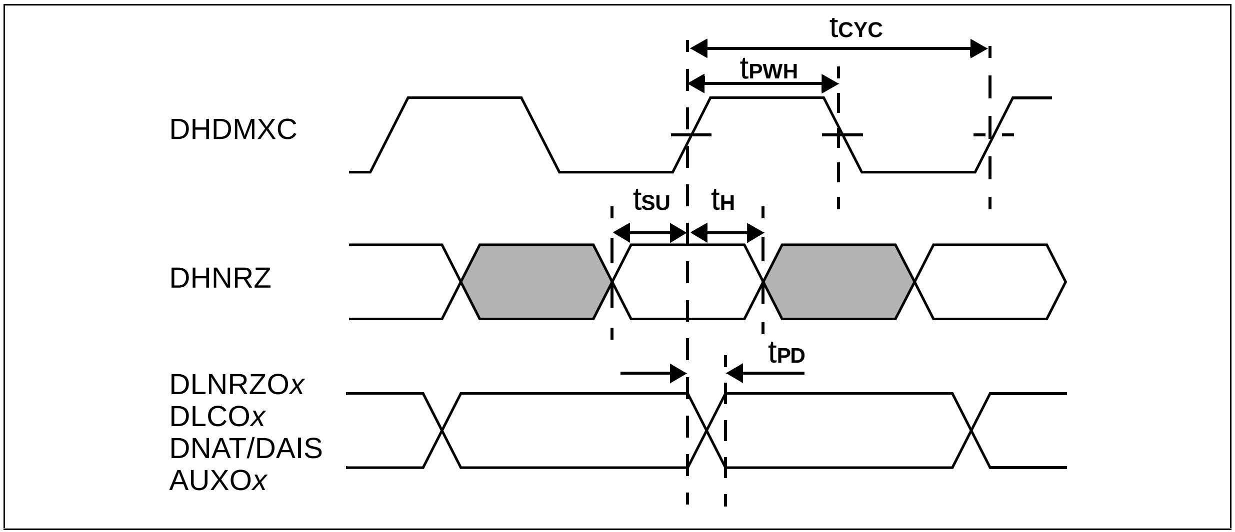

Table 8. High Speed Demultiplexer Input & Output (Refer to Figure 11)

Parameter	Symbol	Min	Type	Max	Unit
Clock duty cycle	tPWH	45	—	75	%
Data to clock setup time	tSU	8	—	—	ns
Data to clock hold time	tH	5	—	—	ns
Clock to data propagation time	tPD	—	20	30	ns

Figure 12. Chip Enable Timing (Refer to Table 9)

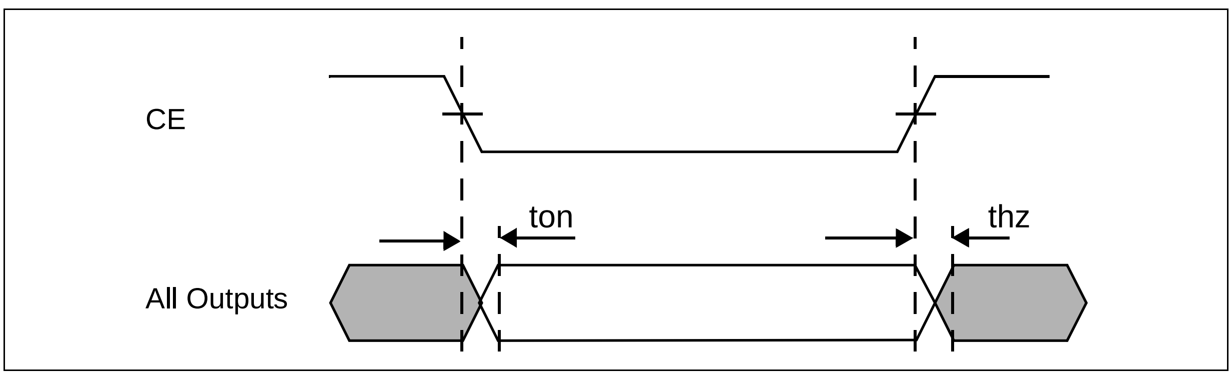

Table 9. Chip Enable (Refer to Figure 12)

Parameter	Symbol	Min	Type	Max	Unit
CE to outputs enabled	tON		20	30	ns
CE to outputs high impedance	tPWH		20	30	ns

Figure 13. Package Specifications

100-Pin PQFP

- Part Number LXT6234QE
- Extended Temperature Range

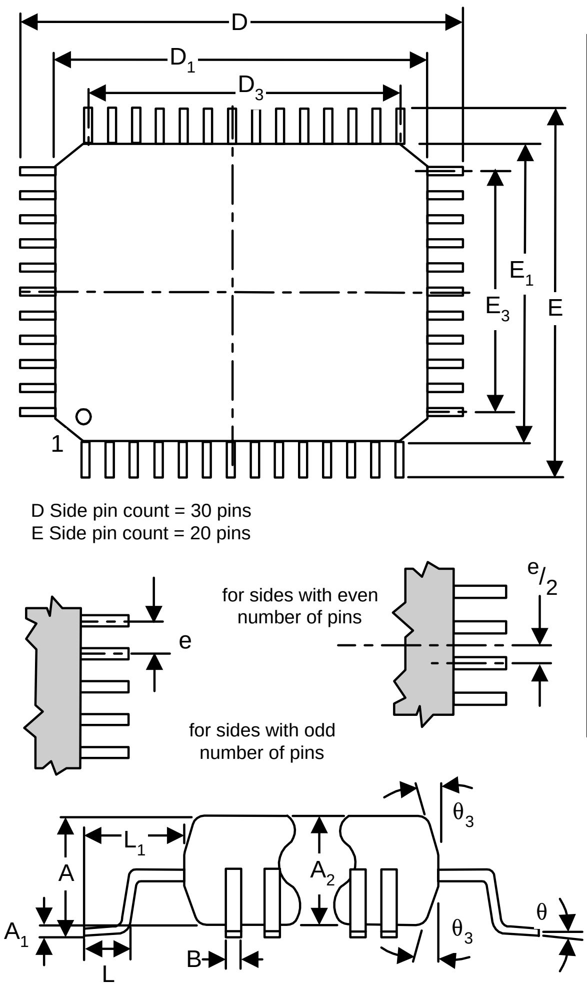

Table 10. 100-Pin Plastic Quad Flat Packs

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.134	–	3.40
A_1	0.010	–	0.25	–
A_2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
D	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10
D_3	0.742 REF		18.85 REF	
E	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10
E_3	0.486 REF		12.35 REF	
e	0.026 BSC (nominal)		0.65 BSC (nominal)	
L	0.026	0.037	0.65	0.95
L_1	0.077 REF		1.95 REF	
q_3	5°	16°	5°	16°
q	0°	7°	0°	7°

BSC—Basic Spacing Between Centers