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FUJITSU

DATA SHEET

CE56 SERIES

0.5 MICRON HIGH PERFORMANCE/LOW POWER CMOS EMBEDDED ARRAYS

DESCRIPTION

The Fujitsu CE56 is a series of high performance CMOS embedded arrays offering diffused high speed RAMS, ROMS and embedded functions. The CE56 series offers density and performance approaching that achievable with standard cell solutions with the time-to-market advantage of a gate array. The CE56 series offers arrays with two metal layers, providing a cost-effective solution ideally suited for complex system designs in markets such as; multimedia, digital video devices, mobile communications, and networking.

The CE56 facilitates complex system-on-chip designs without requiring expensive ceramic packages, heat sinks, or forced air cooling. Featuring true 3V operation, the CE56 features very low power (1.1 microwatt/Mhz) and both a 3.3V and 5.0V compatible I/O interface. This advanced product family is targeted at users who are seeking very high performance and high levels of integration with low power consumption.

CE56 FEATURES

- 0.5 µm drawn channel length; 0.45 µm effective
- Two layer metal
- 45% utilization
- Separate internal cell and I/O supply voltages
- Propogation delay of 210 ps (2-input NAND, F/O=2)
- Low power consumption: 1.1 microwatt/gate/Mhz
- Maximum toggle frequency: 600 MHz
- Comprehensive library with more than 500 logic functions
- Embedded and metalized RAMs available
- Functional macros can be implemented as embedded blocks
- CDDM (Clock Driver Design Methodology) for minimizing clock skew.
- Supports 3.3V and 5.0V I/O interfaces
- Phase Locked Loop (PLL) for interchip clock skew control, clock synthesis, and data recovery
- Wide variety of packages (QFP, SQFP, BGA)
- RAM/ROM compiler supports single and dual-port RAMs
- Supports major third party EDA tools including: Cadence, Mentor, Synopsys

CE56 SERIES PRODUCT SUMMARY

Device Name	Available Gates	I/O Pads
CE56F90	380 K	400
CE56F80	293 K	352
CE56F70	260 K	336
CE56F60	213 K	304
CE56F50	190 K	288
CE56F40	169 K	272
CE56F30	154 K	256
CE56F20	130 K	240
CE56F10	96 K	208
CE56F9	75 K	184
CE56F8	55 K	160

DC CHARACTERISTICS

Measuring conditions: V_{DD} = 3.0V ± 0.3V, V_{SS} = 0V, T_j = 0-100 °C

Parameter	Symbol	Test Conditions		Requirements			Unit
				Min	Typ	Max	
Supply Current	I_{DDS}	$V_{IH} = V_{DDI}$, $V_{IL} = V_{SS}$ Steady state		---	---	3.0[1]	mA
High-level input voltage[2]	V_{IH}	CMOS level	Normal cell	V_{DD} x 0.65	---	V_{DDI}	V
			Schmitt trigger cell	V_{DD} x 0.8	---	V_{DDI}	
Low-level input voltage[3]	V_{IL}	CMOS level	Normal cell	V_{SS}	---	V_{DD} x 0.25	V
			Schmitt trigger cell	V_{SS}	---	V_{DD} x 0.2	
High-level output voltage	V_{OH}	$I_O = I_{OH}$		V_{DDE} -0.5	---	V_{DDE}	V
Low-level output voltage	V_{OL}	$I_O = I_{OL}$		V_{SS}	0	0.4	V
Input leakage current (Tri-state pin input)[3]	I_{LI}, I_{LZ}	V_I = 0 V to V_{DD}		-5	---	5	µA
Input pull-up/pull-down resistor[5]	R_P	Pull-up $V_{IH} = V_{DDI}$		25	50	200	kΩ
	R_N	Pull-down V_{IL} = 0 V					

NOTES:

1. This value does not apply to designs using input buffers with pull-up/pull-down resistance.
2. 5V interface is only for CMOS level.
3. If an input buffer with pull-up/pull-down resistor is used, the input leakage current may exceed the above value.
4. Input buffers and bi-directional buffers may be either no-resistance or pull-up/pull-down resistance.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Requirements		Unit
Supply voltage	V_{DDE}	(External) V_{SS}* -0.5 to 6.0		V
	V_{DDI}	(Internal) V_{SS}* -0.5 to 4.0		
Input voltage	V_I	V_{SS}* -0.5 to V_{DD} +0.5		V
Output voltage	V_O	V_{SS}* -0.5 to V_{DD} +0.5		V
Storage ambient temperature	T_{ST}	Plastic -55 to +125		°C
		Ceramic -65 to +150		
Output current	I_O	Low power-type output buffer I_{OL} = 2 mA	±14	mA
		Normal-type output buffer I_{OL} = 4 mA	± 14	
		Power-type output buffer I_{OL} = 8 mA	± 14	
		High-power type output buffer I_{OL} = 12 mA	± 21	
		Very high-power type output buffer I_{OL} = 24 mA	± 42	

* V_{SS} = 0V

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Requirements			Unit
			Min	Typ	Max	
3.3V Supply voltage (V_{DD} = 3.3V ±3.3V ü± 0.30.3V)		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	3.0	3.3	3.6	
3V Supply voltage (V_{DD} = 3.0V± 0.3V)		V_{DDE}	2.7	3.0	3.3	V
		V_{DDI}	2.7	3.0	3.3	
5V I/O Supply Voltage (V_{DDE5} = 5.0V ± V Supply voltage (VDD = 3.3Vü 3.3V ü ±0.30.3V)0.5V, V_{DDI3}, V_{DDI} = 3.3V ± 0.3V) (for I/0)		V_{DDE5}	4.5	5.0	5.5	V
3V I/O Supply Voltage (V_{DDE5} = 5.0V 0.5W$_{DDI3}$, V_{DDI} = 3.3V ± 0.3V) (for I/0)		V_{DDI3}	2.7	3.0	3.3	V
3V Supply Voltage (V_{DDE5} = 5.0V 0.5W$_{DDI3}$, V_{DDI} = 3.3V ± 0.3V) (for internal cells)		V_{DDI3}	2.7	3.0	3.3	V
High-level input voltage	CMOS Level	V_{IH}	V_{DDI} x 0.65	---	V_{DDE}	V
Low-level input voltage	CMOS Level	V_{IL}	V_{SS}*	---	V_{DDI} x 0.25	V
Junction temperature		T_j	0	---	100	°C

* V_{SS} = 0V

Packaging Options

	CE56 Package Types										
Frame Number (Number of I/O Pads	**F8 (160)**	**F9 (184)**	**F10 (208)**	**F20 (240)**	**F30 (256)**	**F40 (272)**	**F50 (288)**	**F60 (304)**	**F70 (336)**	**F80 (352)**	**F90 (400)**
QFP100	UD	P	P	P	P	P	P				
QFP160	UD	P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C
SQFP80	UD	P	P	P	P						
SQFP100	UD	P	P	P	P	P					
SQFP144	UD	P	P	P	P	P	P	P	P	P	
SQFP176		P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C	
SQFP208			P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C
SQFP 240				P, C	P, C	P, C	P, C	P, C	P, C	P, C	P, C
SQFP256									P, C	P, C	P, C
TQFP100		P	P	P	P	P	P	P	P	P	
BGA256, (Type B)					P	P	P	P	P	P	
BGA352, (Type B)										P	P
BGA352, (Type C)								P	P	P	P

Notes:

C = Ceramic
P = Plastic
UD = Under Development

ASIC Design Kits and EDA Support

ASIC Design Kit		Product Focus	Availability
Verilog	Verilog-XL	Functional and Timing Simulation	Now
	Veritime	Static Timing Analysis	Now
	Verifault	Fault Grading	Now
	Design Compiler	Synthesis	Now
	Sign-off Simulation	Sign-off Quality Libraries	Now
	Documentation	Full Application Documentation	Now
	Sun/Sparc	Sun OS Support	Now
	HP/UX	HP OS Support	Now
Synposys VSS	VSS (VHDL)	Functional and Timing Simulation	Now
	Design Time	Static Timing Analysis	Now
	Design Compiler	Synthesis	Now
	Sign-off Simulation	Sign-off Quality Libraries	Now
	Documentation	Full Application Documentation	Now
	Sun/Sparc	Sun OS Support	Now
	HP/UX	HP OS Support	Now
Mentor	QuickSim2	Functional and Timing Simulation	Now
	AutoLogic2	Synthesis	Now
	Sign-off Simulation	Sign-off Quality Libraries	n/a
	Documentation	Full Application Documentation	Now
	Sun/Sparc	Sun OS Support	Now
	HP/UX	HP OS Support	TBD
3rd Party EDA Tools	Motive	Static Timing Analysis	Now
	Sunrise	ATPG/Fault Grading	Now
	HLD	Floorplanning/Pre-Layout Timing	2Q96
	Preview	Floorplanning	TDB
	DesignPower	Synopsys Power Analysis	2Q96

CLOCK SKEW CONTROL

To maximize performance in high speed, high density arrays, a designer must maintain tight clock skew control. In addition to an available PLL to manage interchip clock skew, Fujitsu's clock driven design methodology (CDDM) offers accurate on chip clock skew control. CDDM offers accurate RC extraction of clock tree parameters and an interactive clock tree implementation. This simplifies trade-offs between clock tree delay and clock skew, early verification of potential design hold time errors, and race conditions.