AS4SD16M72PBG-s/IT,ET,XT

16M x 72, SDR SDRAM MCP

25mm x 32mm, 219 PBGA
1.27mm Pitch

Revision 0.3 (May 31,06) -for new lower ICC limits

Development / ADVANCE Information

Product Information is subject to change or be canceled without notice!

AS4SD16M72PBG-s/IT,ET,XT
16M x 72, SDR SDRAM, 3.3v Core/ 3.3v IO

Features

- Performance: 100MHz, 125MHz and 133MHz
- Core Supply Voltage = 3.3v +/- 0.3v
- IO Supply Voltage = 3.3v +/- 0.3v
- Internal, pipeline, architecture
- Single Clock Input
- Positive edge; Command execution
- DLL for alignment of DQ and DQS transitions
- Four internal banks for concurrent operation
- Data Mask (DM) for masking write data
- Programmable IOL/IOH
- Programmable Burst length: 1,2,4,8 or full page
- Auto Precharge
- Self Refresh Mode on /IT and /ET devices

Silicon Base:

•Micron**:** Die equivalency to MT48LC16M16A2

General Description

Austin Semiconductor's 1.2Gb, Synchronous DRAM is a high speed CMOS MCP and is packaged in a 25mm x 32mm, 219 PBGA with a ball pitch of 1.27mm. This device contains (5) x16 synchronous dynamic random access die, each containing a total density of 268,435,456 bits. The end organization of the MCP is 16M x 80.

Read and Write accesses to the array are burst oriented; accesses start at a selected location and continue for a programmed number of locations, as prescribed by the programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered at the initiation of READ or WRITE are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, 8 or full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

Austin Semiconductor's AS4SD16M72PBG device uses an internal pipeline architecture to achieve high speed operation. This architecture is compatible with the 2n rule of PREFETCH architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. PRECHARGING one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless array access at rated speed.

Initialization

Austin Semiconductor's AS4SD16M72PBG is like all other SDRAM devices and for correct functional operation must be properly initialized in a predefined manor, following the allowable functional modes. Operation of the device outside of the prescribed modes may result in undefined device operation. Once power is applied to VDD and VDDQ and the clock is stable, the device requires a 100us delay prior to issuing a command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100us period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100us delay has been satisfied with at least one COMMAND INHIBIT or NOP, a PRECHARGE command should be applied. All banks must then be PRECHARGED, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Register Definition [MODE REGISTER]

The mode register is used to define the specific mode of operation of the SDRAM MCP. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a WRITE burst mode. The MODE REGISTER is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3

Specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE BURST mode and M10, M11 are reserved for future use. Address A12 (M12) is undefined but should be driven LOW during loading of the MODE REGISTER.

The MODE REGISTER must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

READ and WRITE accesses to the SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1,2,4 and 8 locations are available for both the sequential and the interleaved burst types, and a full page burst is available for the sequential burst mode. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, aas unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst will wrap within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2-A8 (each x16) when the burst length is set to four; and by A3-A8 (each x16) when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of first valid data presented on the Output bus (DQ0-DQ79). The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge N + m. The DQs will start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data will be valid by clock edge n + m. For example, assuming that the clock cycle time is such that all relevant access times are met, If a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will be valid by T2.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test Modes and reserved states should not be used because unknown operation or incompatibility with future version may result.

Write Burst Mode

When M9=0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9=1, the programmed burst length applies to READ bursts, but WRITE accesses are single-location (non-burst) accesses.

Command Inhibit

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS\ is LOW). This prevents unwanted commands from being registered during IDLE or WAIT states. Operations already in progress are not affected.

Load Mode Register

The MODE REGISTER is loaded via inputs A0-A11 (A12 should be driven LOW). See MODE REGISTER heading in the REGISTER DEFINITION section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

Active

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

Read

The read command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 (each x16) selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row will remain open for subsequent accesses. READ data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

Write

The WRITE command is used to initiate a BURST WRITE access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 (each x16) selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be PRECHARGED at the end of the WRITE BURST; if for subsequent accesses input data appearing on the DQs is WRITTEN to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be PRECHARGED, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care”. Once a bank has been PRECHARGED, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

AUTO PRECHARGE is a feature which performs the same individual bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where AUTO PRECHARGE does not apply. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the PRECHARGE is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the PRECHARGE time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type Operation.

Burst Terminate

The BURST TERMINATE command is used to truncate either a fixed-length or full-page burst. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

Auto Refresh

AUTO REFRESH is used during normal operation of the SDRAM MCP and is analogous to CAS\-BEFORE-RAS\ (CBR) REFRESH in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum tRP has been met after the PRECHARGE command.

The addressing is generated by the internal REFRESH controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 256Mb SDRAM MCP requires 8,192 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 7.81us will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), once every 64ms.

Self Refresh

The SELF REFRESH command can be used to retain data in the SDRAM MCP, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM MCP retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM MCP become "Don't Care" with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM MCP must remain in SELF REFRESH mode for a minimum period equal to tRAS and may remain in SELF REFRESH for an indefinite period of time beyond the minimum.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM MCP must have NOP commands issued (a minimum of two clocks) for tXSR because time is required for the completion of any internal REFRESH in progress.

Upon exiting the SELF REFRESH mode, AUTO REFRESH commands must be issued every 7.81us or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

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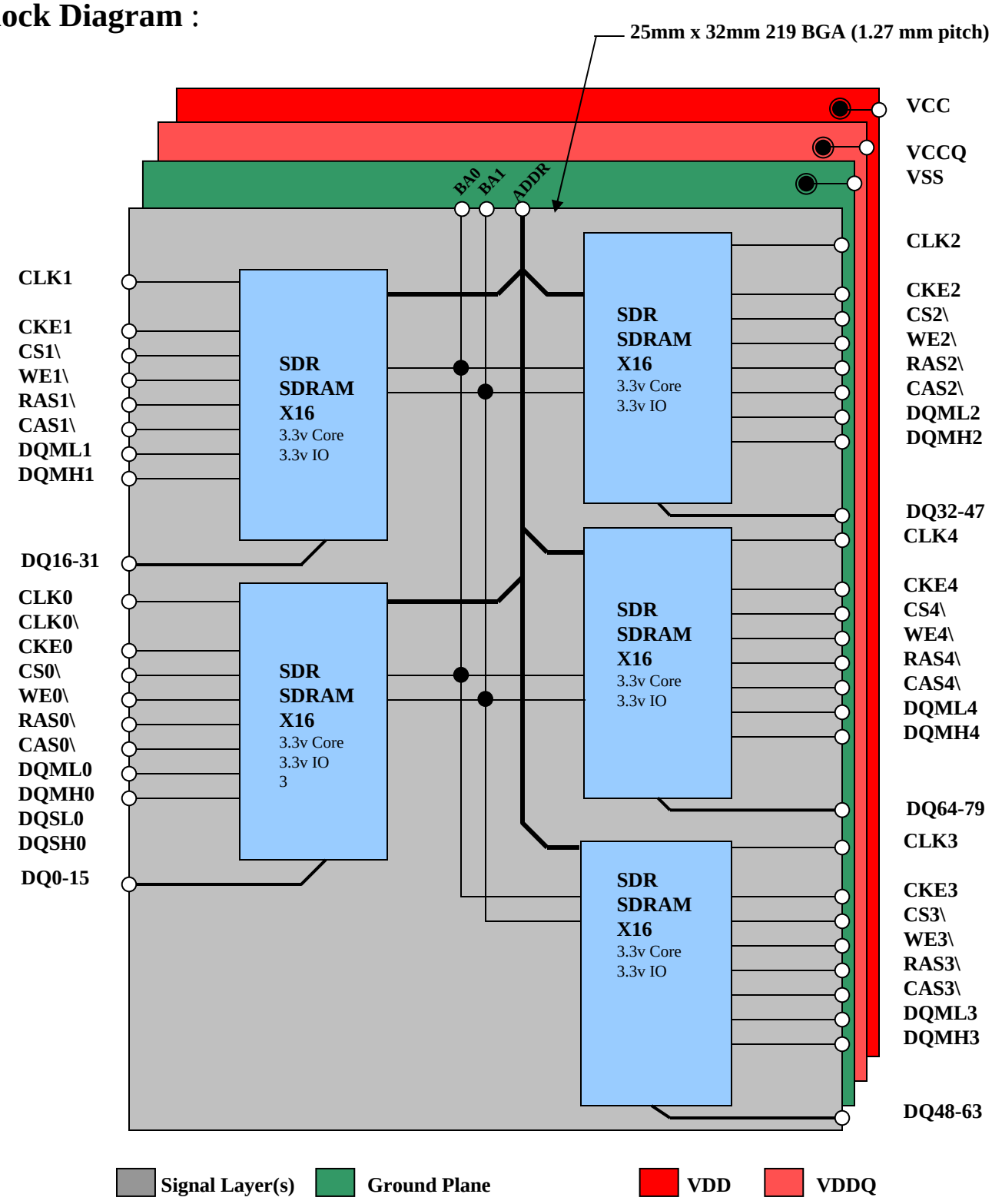
Block Diagram :



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SDRAM-SDR Pinout Top View
Rev. A, 12/04 - X72/X80

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
a		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VCCQ	VCCQ	DQ16	DQ17	DQ31	VSS	a
b	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VCC	VCC	DQ18	DQ19	DQ29	DQ30	b
c	DQ3	DQ4	DQ10	DQ11	VCC	VCC	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	c
d	DQ6	DQ5	DQ8	DQ9	VCCQ	VCCQ	A12	DNU	DNU	DNU	VSS	VSS	DQ22	DQ23	DQ26	DQ25	d
e	DQ7	DQML0	VCC	DQMH0	NC	NC	NC	BA0	BA1	NC	NC	NC	DQML1	VSS	NC	DQ24	e
f	CAS0\	WE0\	VCC	CLK0	NC							RAS1\	WE1\	VSS	DQMH1	CLK1	f
g	CS0\	RAS0\	VCC	CKE0	NC							CAS\	CS1\	VSS	NC	CKE1	g
h	VSS	VSS	VCC	VCCQ	VSS							VCC	VSS	VSS	VCCQ	VCC	h
j	VSS	VSS	VCC	VCCQ	VSS							VCC	VSS	VSS	VCCQ	VCC	j
k	NC	CKE3	VCC	CS3\	NC							NC	CKE2	VSS	RAS2\	CS2\	k
l	NC	CLK3	VCC	CAS3\	RAS3\							NC	CLK2	VSS	WE2\	CAS2\	l
m	DQ56	DQMH3	VCC	WE3\	DQML3	CKE4	DQMH4	CLK4	CAS4\	WE4\	RAS4\	CS4\	DQMH2	VSS	DQML2	DQ39	m
n	DQ57	DQ58	DQ55	DQ54	NC	NC	DQ73	DQ72	DQ71	DQ70	DQML4	NC	DQ41	DQ40	DQ37	DQ38	n
p	DQ60	DQ59	DQ53	DQ52	VSS	VSS	DQ75	DQ74	DQ69	DQ68	VCC	VCC	DQ43	DQ42	DQ36	DQ35	p
r	DQ62	DQ61	DQ51	DQ50	VCC	VCC	DQ77	DQ76	DQ67	DQ66	VSS	VSS	DQ45	DQ44	DQ34	DQ33	r
t	VSS	DQ63	DQ49	DQ48	VCCQ	VCCQ	DQ79	DQ78	DQ65	DQ64	VSS	VSS	DQ47	DQ46	DQ32	VCC	t
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

Ground | Array Power | D/Q Power | Address | Data IO

NC | CNTRL | ADDRESS/ DNU | UNPOPULATED

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Pin Descriptions

BGA Locations	SYMBOL	DESCRIPTION
F4, F16, L2, L13,	CKx	Clock: CKx is the clock input. All address and control input signals are sampled on the crossing of the positive edge of CKx\. Output data (DQ's and DQS) is referenced to rising edge of CLKx
G4, G16, K2, K13 M6	CKEx	Clock Enable: CKE controls the clock inputs. CKE high enables, CKE Low disables the clock input pins. Driving CKE Low provides PRECHARGE POWER-DOWN and SELF REFRESH operations, or ACTIVE POWER-DOWN. CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry CKE is Asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers are disabled during POWER-DOWN Input buffers are disabled during SELF REFRESH.
G1, G13, K4, K16 M12	CSx\	Chip Select: CSx\ enagles the COMMAND register(s) of each of the five (5) contained words. All commands are masked when CSx\ is registered HIGH. CSx\ provides for external bank selection on systems with multiple banks. CSx\ is considered part of the COMMAND CODE.
F4, F16, G5, G15, K1, K12, L2, L13, N7, M9	RASx\, CASx\ WEx\	Command Inputs: RASx, CASx, and Wex\ define the command being entered
G4, G16, K2, K14 M7	DQMLx, DQMHx	Input Data Mask. DM is an input mask signal for write data. Input data is masked when DQMLx or Hx is sampled HIGH at time of a WRITE access. DM is sampled on both edges of DQSLx and DQSHx
E8, E9	BA0, BA1	Bank Address Inputs: BA0, BA1 define which bank an ACTIVE READ, WRITE, or PRECHARGE command is being applied
A7, A8, A9, A10, B7 B8, B9, B10, C7, C8 C9, C10, D7	A0-A11, A12	Address Input: Provide the row address for Active commands, and the column address and auto precharge bit (A10) for READ/WRITE commands to select one location out of the memory array int the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank or all banks. The address inputs also provide the op-code during a MODE RESISTER SET command.

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Pin Descriptions

BGA Locations	SYMBOL	DESCRIPTION
A2, A3, A4, A13, A14 B1, B2, B3, B4, B13 B14, B15, B16, C1, C2,C3,C4,C13,C14, C15,C16,D1,D2,D3, D4,D13,D14,D15,D16 E1,E16,M1,M16,N1 N2,N3,N4,N13,N14, N15,N16,P1,P2,P3, P4,P13,P14,P15,P16 R1,R2,R3,R4,R13, R14,R15,R16,T2,T3, T4,T13,T14,T15,N7, N8,N9,N10,P7,P8,P9 P10,R7,R8,R9,R10 T7,T8,T9,T10	DQ0-79	Data I/O
B11,B12,C5,C6,E3, F3,G3,H3,H12,H16, J3,J12,J16,K3,L3,M3 P11,P12,R5,R6,T16	VCC	Core Power Supply
A11,A12,D5,D6,H4, H15,J4,J15,T5,T6	VCCQ	I/O Power Supply
A5,A6,A16,B5,B6, C11,C12,D11,D12, E14,F14,G14,H1,H2, H5,H13,H14,J1,J2,J5 J13,J14,K14,L14 P5,P6,R11,R12,T1, T11,T12, M14	VSS	Ground (Digital)
E5,E6,E7,E10,E11, E12,E15,F5,G5,G15, K1,K5,K12,L12,N5, N6,N12	NC	Not Connected Internally

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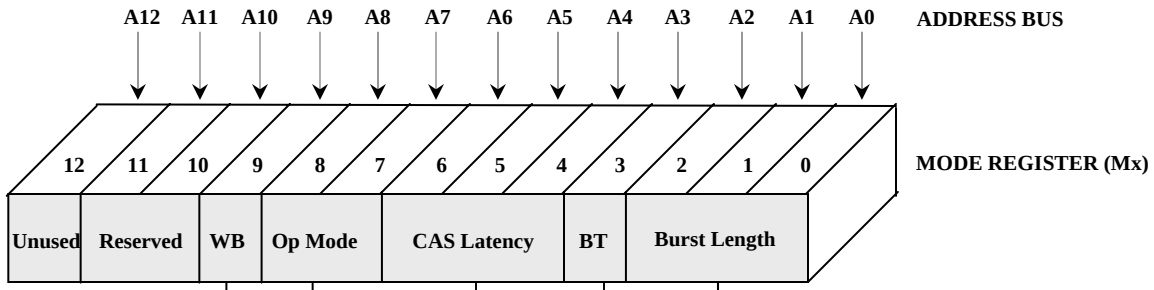
Mode Register Definition



M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

			Burst Length	
M2	M1	M0	M3=0	M3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M8	M7	M6 – M0	Operating Mode
0	0	Valid	Normal Operation
1	0	Valid	Normal Operation / Reset DLL

M9	Operating Mode
0	Normal Operation
1	Single Location Access

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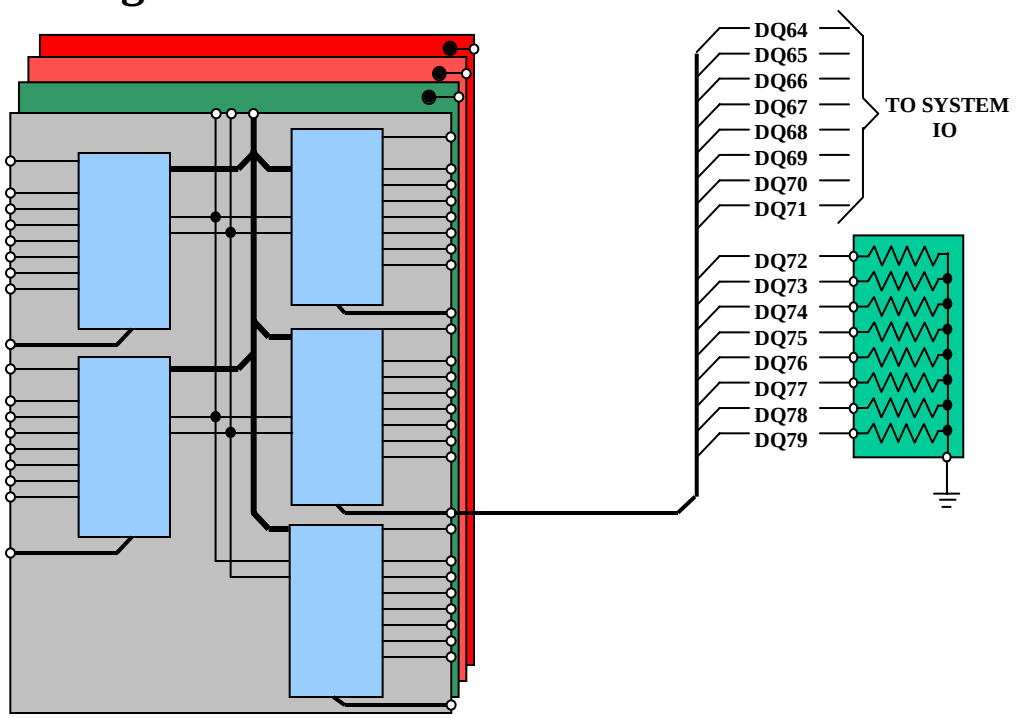
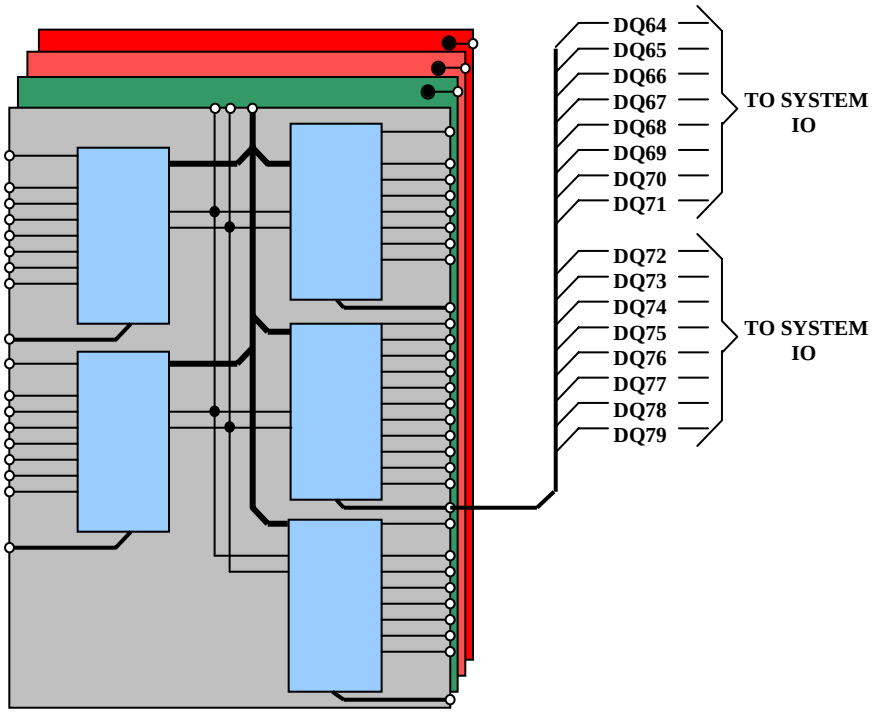
Recommended IO Consideration(s)
X72 Designs



X80 Designs



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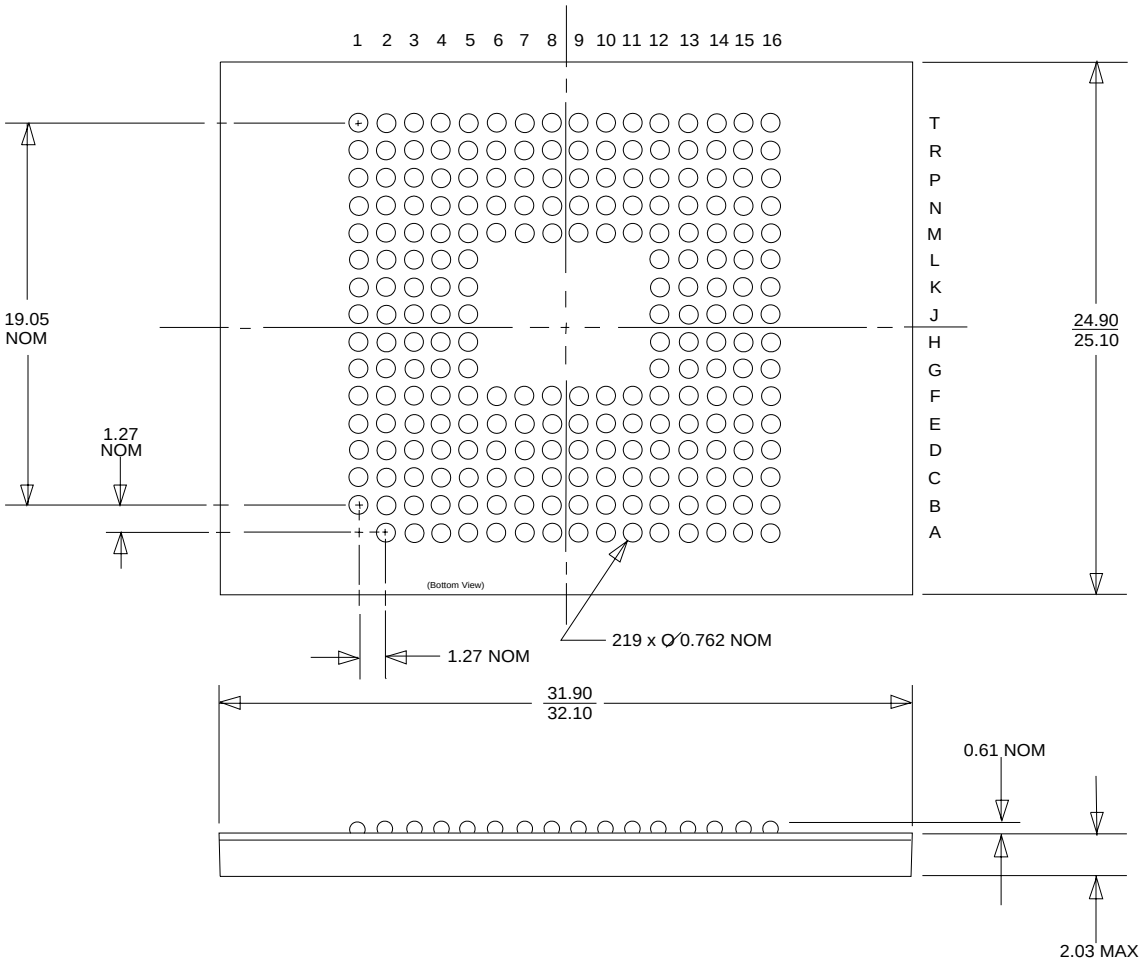
Mechanical :



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DC Electrical Characteristics and Operating Conditions

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	**VDD**	**3.0**	**3.6**	**V**	
I/O Supply Voltage	**VDDQ**	**3.0**	**3.6**	**V**	
Input High (Logic 1) Voltage	**VIH(DC)**	**2.0**	**VDD + 0.3**	**V**	
Input Low (Logic 0) Voltage	**VIL(DC)**	**-0.3**	**0.8**	**V**	
INPUT LEAKAGE (non address)	**II**	**-5**	**5**	**µA**	
INPUT LEAKAGE (address)	**II**	**-25**	**25**	**µA**	
Any input 0V VIN VDD, VREF PIN 0V VIN 1.35V (All other pins not under test = 0V)					
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V VOUT VDDQ)	**IOZ**	**-5**	**5**	**µA**	
OUTPUT LEVELS:					
High Current (VOUT = 2.4V minimum VTT)	**IOH**	**-4.0**	**-**	**mA**	
Low Current (VOUT = 0.4V,	**IOL**	**4.0**	**-**	**mA**	

Capacitance

DESCRIPTIONS	CONDITIONS	Sym	Typ	UNITS	NOTES
Address; A0-A12, BA0, BA1	TA = 25 C; f = 1Mhz	**Ca**	30	pF	
Input / Output		**CIO**	12	pF	
Clocks; CLKx, CLKx\, CKEx		**Cck**	8	pF	
Input Pins: all other input only		**CI**	9	pF	

Note(s): Power calculated with Ouputs unloaded

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PARAMETER/CONDITION	SYMBOL	MAX			UNITS
		-75	-8	-10	
OPERATING CURRENT: Active Mode; Burst = 2, READ or WRITE, tRC = tRC MIN	**ICC1**	**625**	**600**	**550**	**mA**
STANDBY CURRENT: Power-Down Mode; All banks idle, CKE = LOW	**ICC2**	**12**	**12**	**12**	**mA**
STANDBY CURRENT: Active Mode; CKE = HIGH, CS\ = HIGH, All banks active after tRCD met; No accesses in progress	**ICC3**	**200**	**200**	**200**	**mA**
OPERATING CURRENT: Burst Mode; Page Burst; READ or WRITE, All banks Active	**ICC4**	**675**	**625**	**575**	**mA**
AUTO REFRESH CURRENT: tRFC = tRFC MIN CS\ = HIGH, CKE = HIGH	**ICC**	**1350**	**1250**	**1150**	**mA**
AUTO REFRESH CURRENT: tRFC = 7.81us CS\ = HIGH, CKE = HIGH	**ICC6**	**20**	**20**	**20**	**mA**
SELF REFRESH CURRENT: CKE </= 0.2V	**ICC7**	**7.5**	**7.5**	**7.5**	**mA**

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AC Electrical Characteristics

			-75		-8		-10		
Parameter		Symbol	MIN	MAX	MIN	MAX	MIN	MAX	Units
Access time from CLK	CL = 3	tAC		5.4		6		7	ns
	CL = 2	tAC		6		6		7	ns
Address Hold		tAH	1		1		1		ns
Address SetUp		tAS	1.5		1.5		2		ns
CLK High Level width		tCH	2.5		3		3		ns
CLK Low Level width		tCL	2.5		3		3		ns
Clock Cycle Time	CL = 3	tCK	7.5		8		10		ns
	CL = 2	tCK	10		10		13		ns
CKE Hold Time		tCKH	1		1		1		ns
CKE SetUp Time		tCKS	1.5		2		2		ns
CS\, RAS\, CAS\, WE\, DQM Hold Time		tCMH	1		1		1		ns
CS\, RAS\, CAS\, WE\, DQM SetUp Time		tCMS	1.5		2		2		ns
Data-In Hold Time		tDH	1		1		1		ns
Data-In SetUp Time		tDS	1.5		2		2		ns
Data Out High Impedance Time	CL = 3	tHZ		5.4		6		7	ns
	CL = 2	tHZ		6		6		7	ns
Data-Out Low Impedance Time		tLZ	1		1		1		ns
Data-Out Hold Time (under load)		tOH	3		3		3		ns
Data-Out Hold Time (no load)		tOHn	1.8		1.8		1.8		ns
ACTIVE to PRECHARGE command		tRAS	45	120000	50	120000	50	120000	ns
ACTIVE to ACTIVE command period		tRC	70		70		70		ns
ACTIVE to READ or WRITE delay		tRCD	20		20		20		ns
REFRESH period (8,192 rows) Industrial		tREF		64		64		64	ms
REFRESH period (8,192 rows) Enhanced		tREF		32		32		32	ms
REFRESH period (8,192 rows) Extended		tREF		24		24		24	ms
AUTO REFRESH period		tRFC	66		68		70		ns
PRECHARGE command period		rRP	20		20		20		ns
ACTIVE bank a to ACTIVE bank b command		tRRD	20		20		20		ns
Transition Time		tT	0.3	1.2	0.3	1.2	0.3	1.2	ns
WRITE Recovery Time		tWR	1CLK +		1CLK +		1CLK +		
			7ns		7ns		7ns		
			15		15		15		ns
Exit SELF REFRESH to ACTIVE command		tXSR	75		80		80		ns

AS4SD16M72PBG-s/IT.ET,XT
16M x 72, SDR SDRAM, 3.3v Core/ 3.3v IO

Ordering Information

Part Number	Configuration	Technology	Frequency	VCC	Temp
AS4SD16M72PBG-MS	4 x 4M x 72/80	SDRAM; SDR	Non-Functional	3.3	MECH. SAMPLES
AS4SD16M72PBG-ES	4 x 4M x 72/80	SDRAM; SDR	Functional	3.3	ENG. SAMPLES
AS4SD16M72PBG-75/IT	4 x 4M x 72/80	SDRAM; SDR	133MHz	3.3	0C - 70C
AS4SD16M72PBG-8/IT	4 x 4M x 72/80	SDRAM; SDR	125MHz	3.3	0C - 70C
AS4SD16M72PBG-10/IT	4 x 4M x 72/80	SDRAM; SDR	100MHz	3.3	0C - 70C
AS4SD16M72PBG-75/ET	4 x 4M x 72/80	SDRAM; SDR	133MHz	3.3	-40C - 105C
AS4SD16M72PBG-8/ET	4 x 4M x 72/80	SDRAM; SDR	125MHz	3.3	-40C - 105C
AS4SD16M72PBG-10/ET	4 x 4M x 72/80	SDRAM; SDR	100MHz	3.3	-40C - 105C
AS4SD16M72PBG-75/XT	4 x 4M x 72/80	SDRAM; SDR	133MHz	3.3	-40C - 125C
AS4SD16M72PBG-8/XT	4 x 4M x 72/80	SDRAM; SDR	125MHz	3.3	-40C - 125C
AS4SD16M72PBG-10/XT	4 x 4M x 72/80	SDRAM; SDR	100MHz	3.3	-40C - 125C

SHADED Consult Factory for Availability