



**VITELIC**

**V55C100 FAMILY**  
**HIGH PERFORMANCE, LOW POWER,**  
**1M x 1 BIT, FAST PAGE MODE,**  
**CMOS DYNAMIC RAM**

**ADVANCED**

**Features**

- Separate I/O
- 60 ns  $\overline{\text{RAS}}$  access time
- 45 ns Fast Page mode cycle time
- 512 refresh cycles each 8 ms
- Low power, CMOS standby current
  - V55C100—1.5 mA
- Space saving
  - 18-pin 300 mil Plastic DIP
  - 26/20-pin 300 mil SOJ
- On-substrate bias generator

**Description**

The V55C100 is a fast page mode, 1048,576 word by one bit dynamic RAM. It is designed to operate from a single, 5 V  $\pm 10\%$  tolerance power supply. Fabricated using an advanced CMOS technology, the device provides both high performance and high reliability over its operating range. Because it utilizes static circuitry, and its flow-through column address latches allow address pipelining, many critical system timing requirements are relaxed. These features make the V55C100 ideally suited for high performance, low power applications.

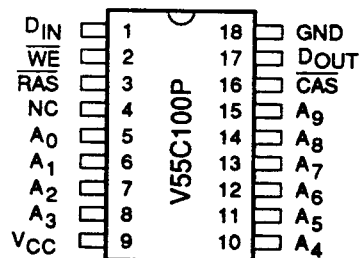
Multiplexed address inputs and 1.0 micrometer design rules permit the V55C100 to be packaged in standard 300 mil plastic 18-pin DIPs and 300 mil plastic 26/20-pin SOJs.

Refreshing can be accomplished by using  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$ ,  $\overline{\text{RAS}}$ -only, or normal read or write cycles.

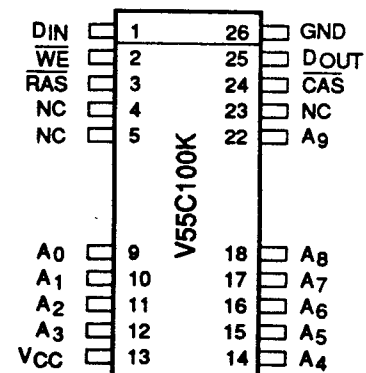
An internal address counter obviates the need for externally supplied addresses during the  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh mode. Externally supplied addresses are required during  $\overline{\text{RAS}}$ -only, or normal read or write cycles.

**Pin Configurations**

**18-Pin Plastic DIP**



**26/20-Pin Plastic SOJ**



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