Unity-Gain Video Buffer

Features

- −3 dB-Bandwidth: 730 MHz
- Low Differential Gain: 0.1%
- Low Differential Phase: 0.01°
- Low Power—P_D: 150 mW
- Fast Settling: 0.2% in 5 ns
- Low Distortion: −65 dBc at 20 MHz

Benefits

- Flat Frequency Response
- High Color Fidelity
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Improved Transmission Accuracy

Applications

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Systems
- Line Drivers

Description

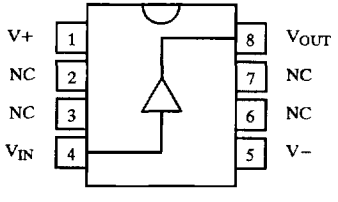
The Si581 is a monolithic closed-loop unity-gain video buffer with a very wide −3-dB bandwidth (730 MHz). Its unique design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si581 features low power dissipation (150 mW, typical), fast settling (0.2% in 5 ns), without signal degradation. Distortion is typically −65 dBc at 20 MHz, gain flatness is less than 0.4 dB from dc to 50 MHz. These performance specifications allow the designer to improve system bandwidth while reducing power dissipation, board space and design complexity. The output is protected against short circuits to ground.

The Si581 uses a complementary bipolar IC process to achieve excellent high frequency performance. All performance is specified and rated for operation with ±5-V supplies, reducing power consumption compared with traditional ±15-V designs.

Functional Block Diagrams and Pin Configurations

Dual-In-Line and SOIC



Top View

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	8-Pin Plastic DIP	Si581DJ
	8-Pin Narrow SOIC	Si581DY

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Absolute Maximum Ratings

Supply Voltage ..... ±7 V
Input Voltage Range ..... V− to V+
Output Short Circuit Duration ..... Continuous
Output Current ..... 70 mA

Storage Temperature ..... −65 to 150°C
Lead Temperature (Soldering 10s) ..... 300°C
Junction Temperature: T_J ..... 175°C

Specifications

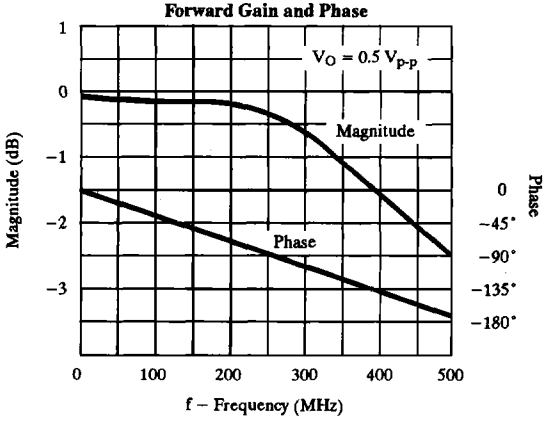
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V, R_L = 100 Ω, R_S = 50 Ω		Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Frequency Domain[h]								
−3-dB Bandwidth[d]	SSBW	V_{OUT} <0.5 V_{p-p}		Room Full	400 300	730		MHz
	MSBW	V_{OUT} = <1 V_{p-p}		Room		450		
	LSBW	V_{OUT} = 5 V_{p-p}		Room Full	55 50	90		
Gain Flatness Peaking[e, g]	GFPH	V_{OUT} <0.5 V_{p-p}, dc to 200 MHz		Room Full		0	0.5 0.8	dB
Gain Flatness Roll Off[e]	GFRH			Room Full		0	0.8 1.2	
Linear Phase Deviation[e]	LPD	dc to 200 MHz		Room Full		0.7	1.5 2	deg
Differential Phase	DP	R_L = 150 Ω $V_{Carrier}$ = 280 mV	f = 3.58 MHz	Room		0.01		
			f = 4.43 MHz	Room		0.01		
Differential Gain	DG	f = 4.43 MHz $V_{Carrier}$ = 280 mV	R_L = 150 Ω	Room		0.1		%
			R_L = 1 kΩ	Room		0.07		
Time Domain[d, h]								
Rise and Fall Time	t_{RS}	V_{IN} = 0.5 V Step Input Rise/Fall time = 300 ps		Room Full		0.4	1 1.4	ns
	t_{RL}	V_{IN} = 5 V Step Input Rise/Fall time ≤ 1 ns		Room Full		4.5	7.5 8.5	
Settling Time	t_{SP}	To ±0.2 %, V_{IN} = 2 V Step		Full		5	10	
Slew Rate	SR			Room Full	500 450	800		V/µs
Distortion and Noise								
2nd Harmonic Distortion[g]	HD_2	V_{IN} = 2 V_{p-p}, f_{IN} = 20 MHz		Room Full		−65	−55 −48	dBc
3rd Harmonic Distortion[g]	HD_3			Full		−65	−55	
Equivalent Input Noise Floor[d]	SNF	f >100 kHz		Room Full		−158	−155 −154	dBm (1 Hz)
Equivalent Input Integrated Noise[d]	INV	100 kHz < f <200 MHz		Room Full		40	57 63	µV
Static, dc								
Small Signal Gain[d]	GA			Room Full	0.96 0.95	0.97		V/V
Integral Endpoint Linearity[d]	ILIN	±2 V Full Scale		Room Full		0.2	0.4 0.8	%FS
Input Offset Voltage[f]	VIO			Room Full		2	8 16	mV
Input Offset Voltage Average Temperature Coefficient[d]	DVIO			Room Full		20	– 100	µV/°C
Input Bias Current[f]	IBN			Room Full		±20	±50 ±100	µA
Input Bias Current Average Temperature Coefficient[d]	DIBN			Room Full		200	– 700	nA/°C
Power Supply Rejection Ratio[g]	PSRR			Full	45	50		dB
Supply Current[f]	I+	No Load		Full		15	20	mA

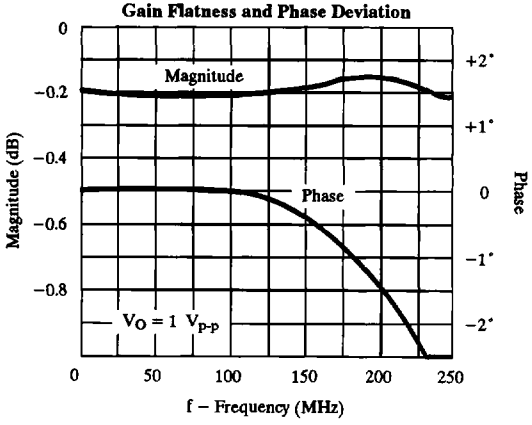
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_S = 50 Ω	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Miscellaneous[d]							
Input Resistance	R_{IN}		Room Full	100 50	160		kΩ
Input Capacitance	C_{IN}		Room Full		1.6	2.2 2.5	pF
Output Impedance	R_O	At dc	Room Full		2	3 3.5	Ω
Output Voltage Range	V_O		Room Full	−3.2 −3	±4	3.2 3	V
Output Current	I_O		Room Full	−50 −45	±70	50 45	mA

Notes:
a. Room = 25°C, Full = −40 to 85°C.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. Gain flatness tests are performed from 0.1 MHz to 200 MHz.
f. Parameter is 100% tested at 25°C and sample tested at 85°C.
g. Parameter is sample tested at 25°C.
h. AC performance is very dependent on layout. Specifications apply only in a 50-Ω microstrip environment.

Typical Characteristics: V_{SUP} = ±5 V, R_L = 100 Ω, R_S = 50 Ω





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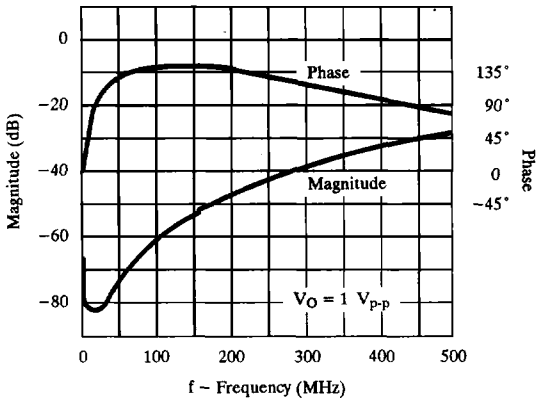
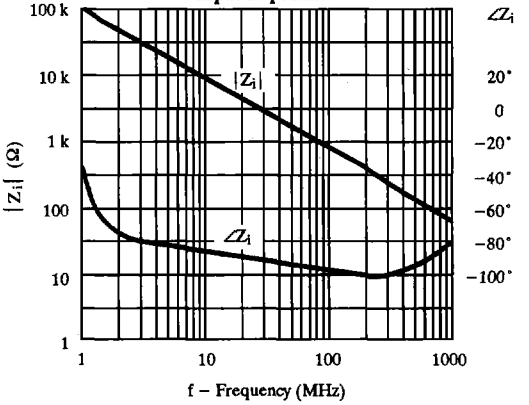
Typical Characteristics: $V_{SUP} = \pm 5$ V, $R_L = 100\ \Omega$, $R_S = 50\ \Omega$ (Cont'd)

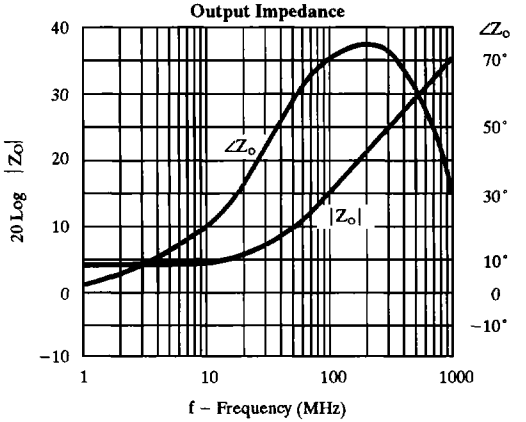
Reverse Gain and Phase



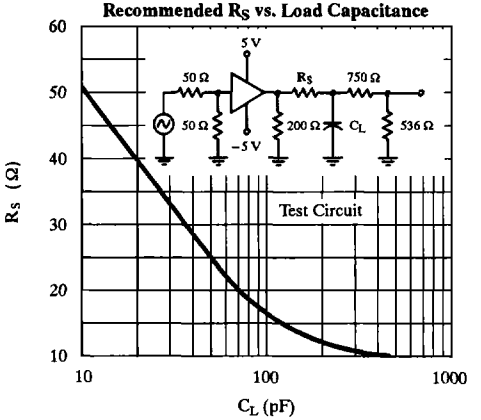
Input Impedance



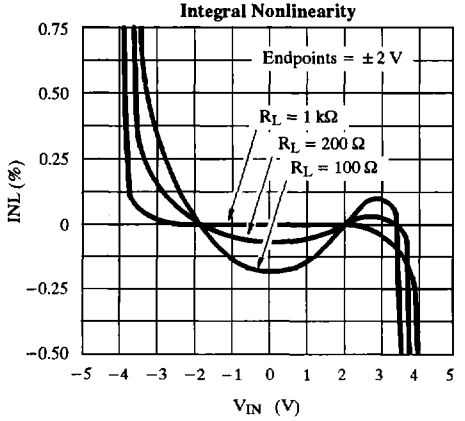
Output Impedance



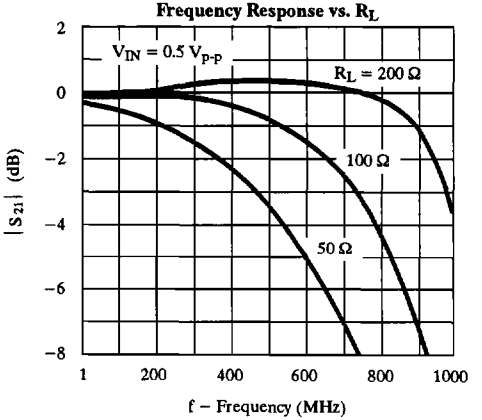
Recommended R_S vs. Load Capacitance



Integral Nonlinearity

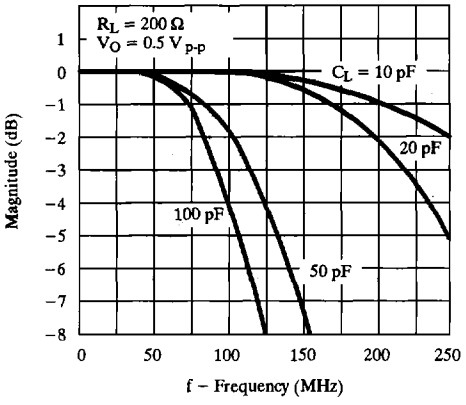


Frequency Response vs. R_L

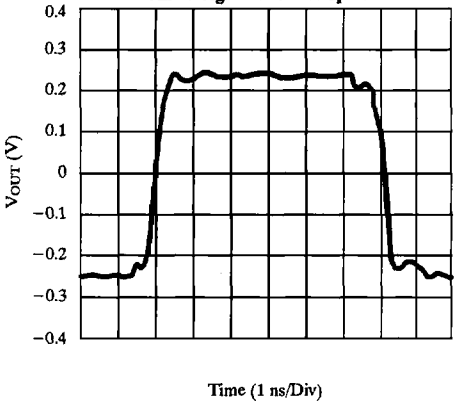


Typical Characteristics: $V_{SUP} = \pm 5$ V, $R_L = 100\ \Omega$, $R_S = 50\ \Omega$ (Cont'd)

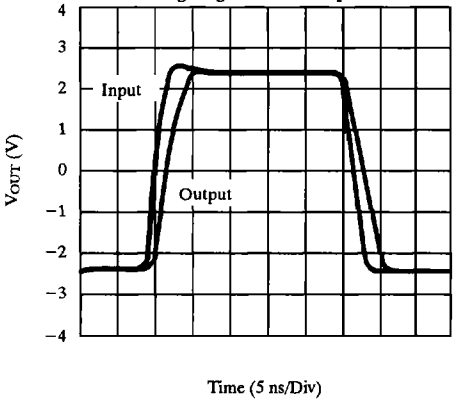
Forward Gain vs. C_L with Recommended R_S



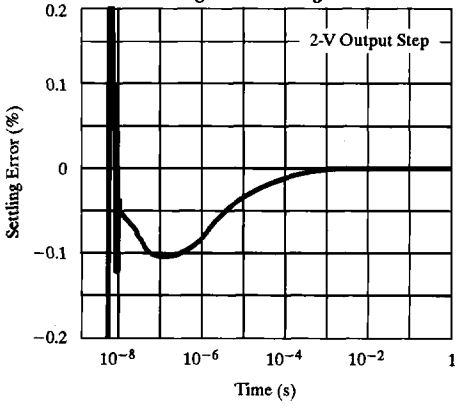
Small Signal Pulse Response



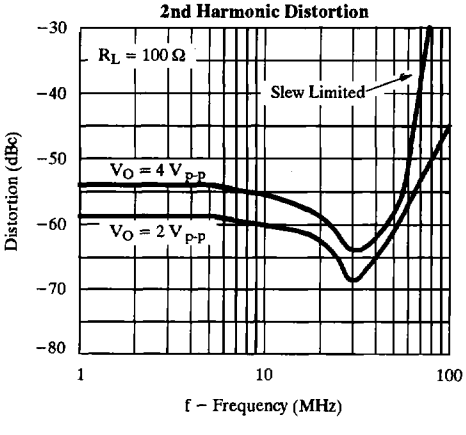
Large Signal Pulse Response



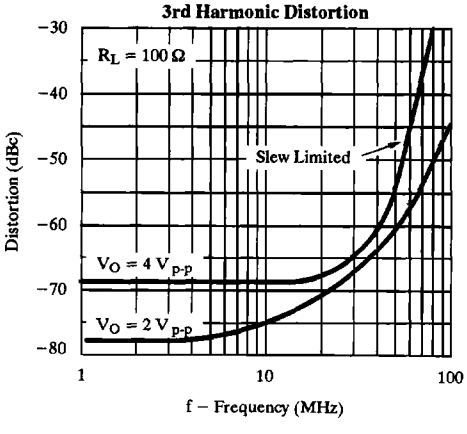
Long-Term Settling Time



2nd Harmonic Distortion



3rd Harmonic Distortion



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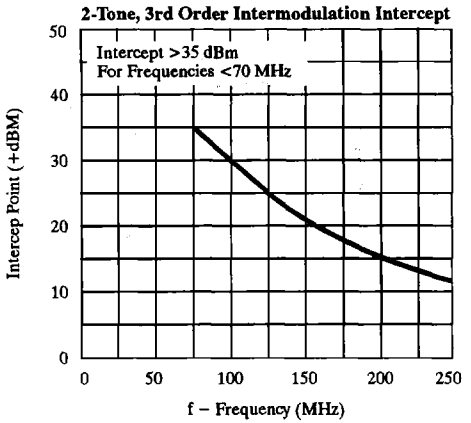
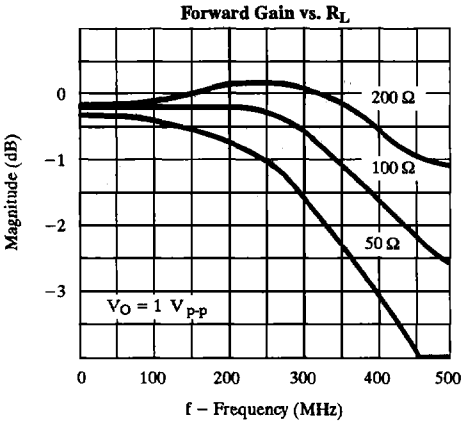
Typical Characteristics: $V_{SUP} = \pm 5$ V, $R_L = 100\ \Omega$, $R_S = 50\ \Omega$ (Cont'd)





Applications

The Si581 provides the accuracy of a closed-loop amplifier plus unmatched dynamic performance.

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the Si581 which has a typical bandwidth of 730 MHz.

To minimize capacitive feedthrough, the pins which are not connected internally (pins 2, 3, 6, and 7) should be connected to the ground plane. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the Si581. On a 0.065-inch epoxy PCB material, a 50-Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing. The ferrite beads are optional and are recommended only where additional isolation from high-frequency (>400 MHz) resonances of the power supply is needed.

Parasitic or load capacitance directly on the output of the Si581 will introduce additional phase shift in the device, which can lead to decreased phase margin and frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The typical characteristic curves illustrate the required resistor value and the resulting performance vs. capacitance.

Precision resistors with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed metal film resistors will work, though they will cause a degradation of ac performance due to their reactive nature at high frequencies.

Applications (Cont'd)

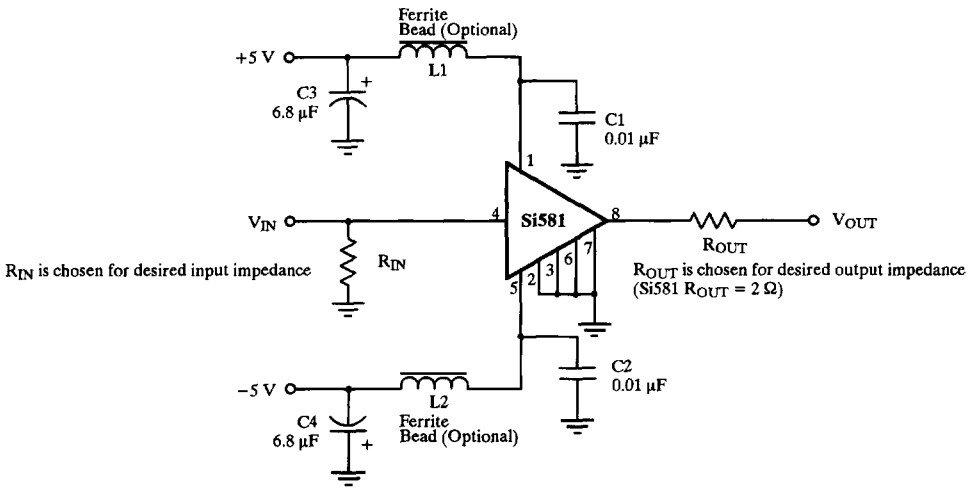


Figure 1. Recommended Decoupling

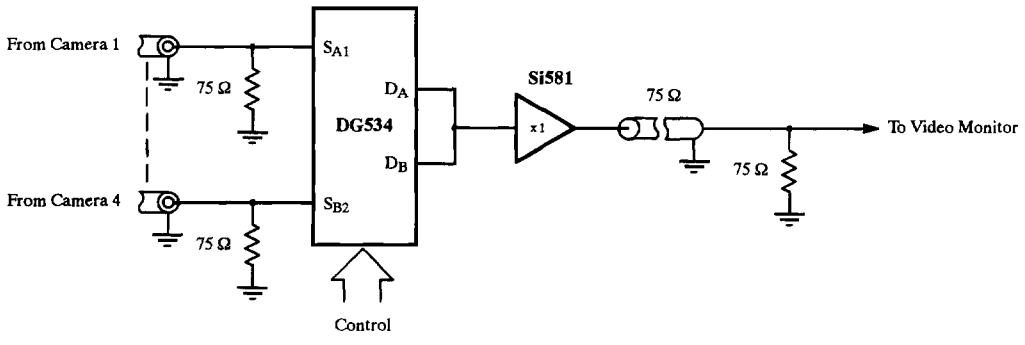


Figure 2. Four Camera High-Definition Closed Circuit TV System

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