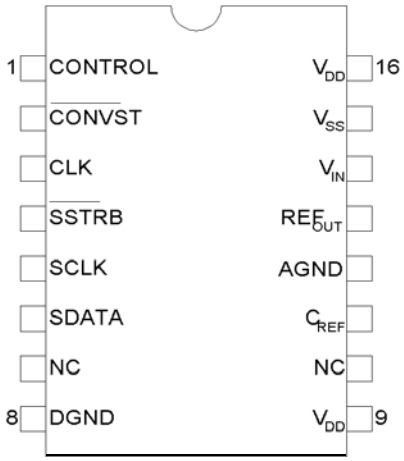
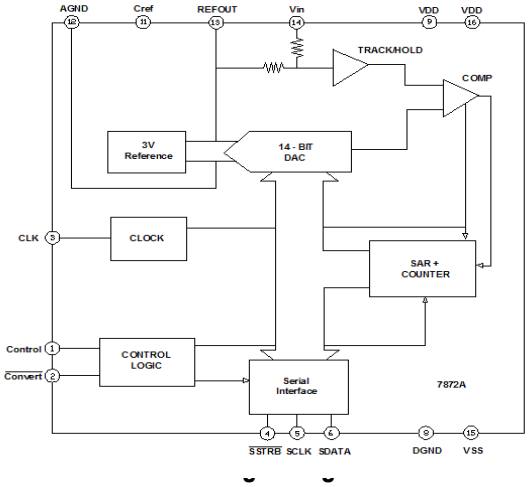
7872A
14-Bit A/D Converter





FEATURES:

- 14-bit resolution and accuracy
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Single event effects:
  - SEL > 104 MeV/mg/cm^2
  - SEU_{TH} = 1.4 MeV/mg/cm^2
  - SEU_{Sat} = 1E-3 cm^2/Device
- Package:
  - 16 pin RAD-PAK® flat package
  - 16 pin RAD-PAK® dual-in-line package
- Fast Conversion Times: 10 µs
- Low 50 mW typical power consumption
- High speed LC^{2}MOS technology
  - Analog input range of ±3V
  - 83 KSPS throughput rate
  - Operates with +5V/-5V power supplies
  - 80 dB SNR at 10 kHz input frequency
  - Serial output

DESCRIPTION:

DDC's 7872A high-speed 14-bit ADC microcircuit features a greater than 100 krad (Si) total dose tolerance; depending upon orbit. The 7872A consists of a track/hold amplifier, successive-approximation ADC, 3V buried Zener reference and versatile interface logic. It features a self-contained, laser- trimmed internal clock, so no external clock timing components are required. To achieve the minimum noise possible, the on-chip clock may be overridden to synchronize the device operation to the digital system. The 7872A is a serial output device. It is capable of interfacing to all modern microprocessors and digital signal processors. The 7872A operates from ±5V power supplies, accepts bipolar input signals of ±3V and is able to convert full power signals up to 41.5 kHz. It is also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

DDC's patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to DDC's self-defined Class S.

(631) 567-5600

TABLE 1. 7872A PIN DESCRIPTION

PIN	SIGNAL	DESCRIPTION
1	CONTROL	Control Function
2	$\overline{\text{CONVST}}$	Convert Start
3	CLK	Clock Input
4	$\overline{\text{SSTRB}}$	Serial Strobe
5	SCLK	Serial Clock
6	SDATA	Serial Data
7	NC	Non Connect
8	DGND	Digital Ground
9	V_{DD}	Positive Supply
10	NC	No Connect
11	C_{REF}	Reference Capacitor
12	AGND	Analog Ground
13	REF_{OUT}	Voltage Reference Output
14	V_{IN}	Analog Input
15	V_{SS}	Negative Supply
16	V_{DD}	Positive Supply

TABLE 2. 7872A ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Positive Supply Voltage; Relative to GND	V_{DD}	-0.3	7.0	V
Negative Supply Voltage; Relative to GND	V_{SS}	+0.3	-7.0	V
AGND to DGND; Relative to GND	--	-0.3	V_{DD} +0.3	V
REF_{OUT}, C_{REF} to AGND	--	0	V_{DD}	V
V_{IN} to AGND	--	V_{SS} -0.3	V_{DD} +0.3	V
Digital Input Voltage	V_{IN}	-0.3	V_{DD} +0.3	V
Digital Output Voltage	V_{OUT}	-0.3	V_{DD} +0.3	V
Weight		--	2.0	Grams
Thermal Impedance	Θ_{JC}	--	2.44	°C/W
Storage Temperature Range	T_S	-65	150	°C
Operating Temperature Range	T_A	-55	125	°C

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{DD}	±10%
I_{SS}	±10%

1. Parameters are measured and recorded as Deltas per MIL-STD-883 for Class S Devices, specified in Table 10.

TABLE 4. 7872A DC ELECTRICAL CHARACTERISTICS FOR DYNAMIC PERFORMANCE [1]

(V_{DD} = 5 V ± 5%, V_{SS} = -5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2 MHz EXTERNAL, f_{SAMPLE} = 83 kHz, -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Signal to Noise Ratio V_{IN} = 10kHz Sine Wave, T_{MIN} to T_{MAX}; SNR is typically 82dB for V_{IN} < 41.5kHz [2]	SNR	4, 5, 6	79	--	--	dB
Total Harmonic Distortion V_{IN} = 10kHz Sine Wave	THD	4, 5, 6	--	-86	--	dB
Peak Harmonic or Spurious Noise	--	4, 5, 6	--	-86	--	dB
Intermodulation Distortion Second Order Terms: f_a = 9 kHz, f_b = 9.5 kHz, f_{SAMPLE} = 50 kHz Third Order Terms: f_a = 9 kHz, f_b = 9.5 kHz, f_{SAMPLE}= 50 kHz	IMD	4, 5, 6	 -- --	 -86 -86	 -- --	dB
Track/Hold Acquisition Time	--	9, 10, 11	--	--	2	µs

1. V_{IN} = ± 3 V. Guaranteed by design.
2. SNR calculation includes distortion and noise components.

TABLE 5. 7872A DC ELECTRICAL CHARACTERISTICS FOR ACCURACY

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Resolution	RES	7, 8A, 8B	14	--	--	Bits
Resolution for Which No Missing Codes are Guaranteed	NMC	7, 8A, 8B	14	--	--	Bits
Integral Nonlinearity @ 25 °C	INL	1, 2, 3	--	±1	--	LSB
Integral Nonlinearity T_{MIN} to T_{MAX}	INL	1, 2, 3	--	--	±2	LSB
Bipolar Zero Error	BZE	1, 2, 3	--	--	±12	LSB
Positive Gain Error [1]	PGE	1, 2, 3	--	--	±12	LSB
Negative Gain Error [1]	NGE	1, 2, 3	--	--	±12	LSB

1. Measured with respect to internal reference.

TABLE 6. 7872A DC ELECTRICAL CHARACTERISTICS FOR ANALOG INPUT

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Input Voltage Range	--	1, 2, 3	-3	3	V
Input Current	--	1, 2, 3	-500	500	µA

TABLE 7. 7872A DC ELECTRICAL CHARACTERISTICS FOR REFERENCE OUTPUT

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
REF_{OUT} @ +25 ˚C	--	1	2.99	3.01	V
REF_{OUT} T_{MIN} to T_{MAX}	--	2, 3	2.98	3.02	V
REF_{OUT} Tempco: Typically 35ppm[1]	--	1, 2, 3	--	±40	ppm/ºC
Reference Load Sensitivity ($DREF_{OUT}$/DI) Reference Load Current Change (0-300 µA); Reference Load Should Not Be Changed During Conversion	--	1, 2, 3	--	1.2	mV

1) Characterized, Not 100% Tested

TABLE 8. 7872A DC ELECTRICAL CHARACTERISTICS FOR LOGIC INPUTS

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Input High Voltage: V_{DD} 5 V ± 5%[2]	V_{INH}	1, 2, 3	2.4	--	V
Input Low Voltage: V_{DD} 5 V ± 5% [2]	V_{INL}	1, 2, 3	--	0.8	V
Input Current: (CONVST) V_{IN} = 0 V to V_{DD}	I_{IN}	1, 2, 3	-10	10	µA
Input Current: (Control, Clk) V_{IN} = V_{SS} to V_{DD}	I_{IN}	1, 2, 3	-10	10	µA
Input Capacitance[1]	C_{IN}	1, 2, 3	--	10	pF

1) Not Tested

2) Application of Signal

TABLE 9. 7872A DC ELECTRICAL CHARACTERISTICS FOR LOGIC OUTPUTS

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Output Low Voltage I_{SINK} = 1.6 mA	V_{OL}	1, 2, 3	--	0.4	V

TABLE 10. 7872A DC ELECTRICAL CHARACTERISTICS FOR CONVERSION TIME

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
External Clock[1]	--	9, 10, 11	--	10	µs
Internal Clock: Nominal Value = 2 MHz	--	9, 10, 11	--	11	µs

1) Application of Signal

TABLE 11. 7872A DC ELECTRICAL CHARACTERISTICS FOR POWER REQUIREMENTS

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	CONDITIONS	SUBGROUPS	REQUIREMENTS	UNITS
Positive Supply Voltage	V_{DD}	5% for Specified Performance	--	5	V
Negative Supply Voltage	V_{SS}	5% for Specified Performance	--	-5	V
Positive Supply Current	I_{DD}	Typically 6mA	1, 2, 3	13	mA max
Negative Supply Current	I_{SS}	Typically 4mA	1, 2, 3	6	mA max
Power Dissipation	P_D	Typically 50mW	1, 2, 3	95	mW max

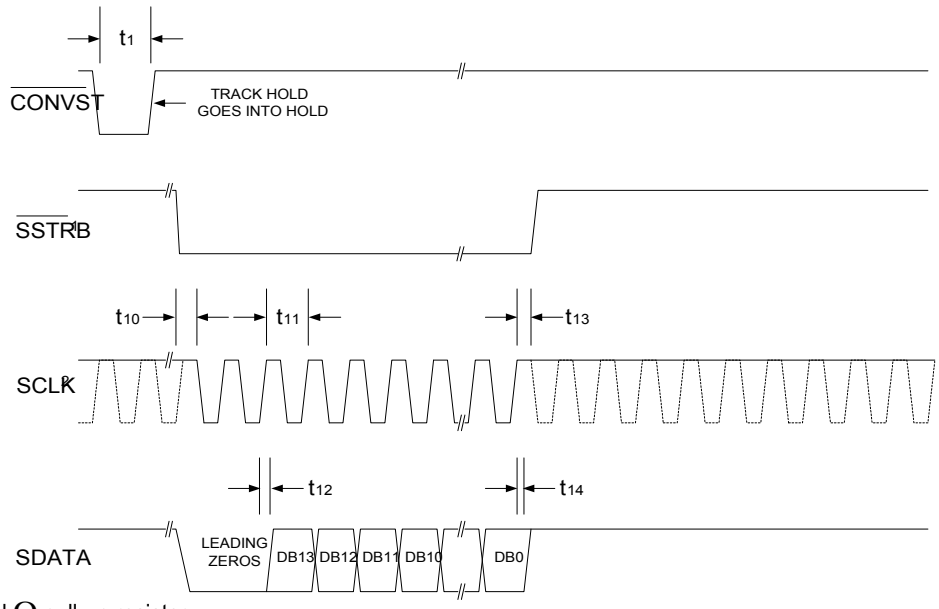
TABLE 12. 7872A TIMING CHARACTERISTICS [1,2]

(V_{DD} = 5V ±5%, V_{SS} = -5 V ± 5%, T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

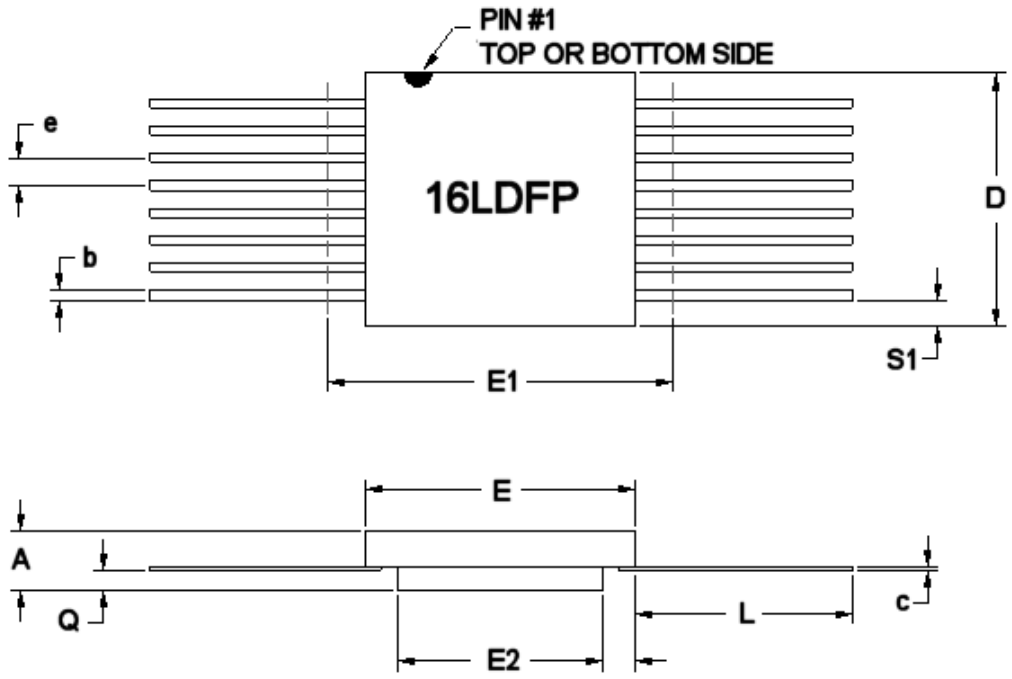
PARAMETER/CONDITION	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
$\overline{\text{CONVST}}$ Pulse Width	t_1	9, 10, 11	50	--	ns
$\overline{\text{SSTRB}}$ to SCLK Falling Edge Setup Time	t_{10}	9, 10, 11	100	--	ns
SCLK Cycle Time [3]	t_{11}	9, 10, 11	440	--	ns
SCLK to Valid Data Delay: C_L = 35 pF [4]	t_{12}	9, 10, 11	--	155	ns
SCLD Rising Edge to $\overline{\text{SSTRB}}$	t_{13}	9, 10, 11	20	150	ns
Bus Relinquish Time After SCLK	t_{14}	9, 10, 11	4	100	ns

1. All input signals are specified with tr = tr = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
2. Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{\text{SSTRB}}$ and a 2 kΩ pull-up resistor on SCLK. The capacitance on all three outputs is 35 pF.
3. SCLK mark/space ration (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
4. SDATA will drive higher capacitive loads, but this will add to t_{12} since it increases the external RC time constant (4.7kΩ/C_L) and hence, the time to reach 2.4 V.

FIGURE 1. MODE 1 TIMING DIAGRAM SERIAL



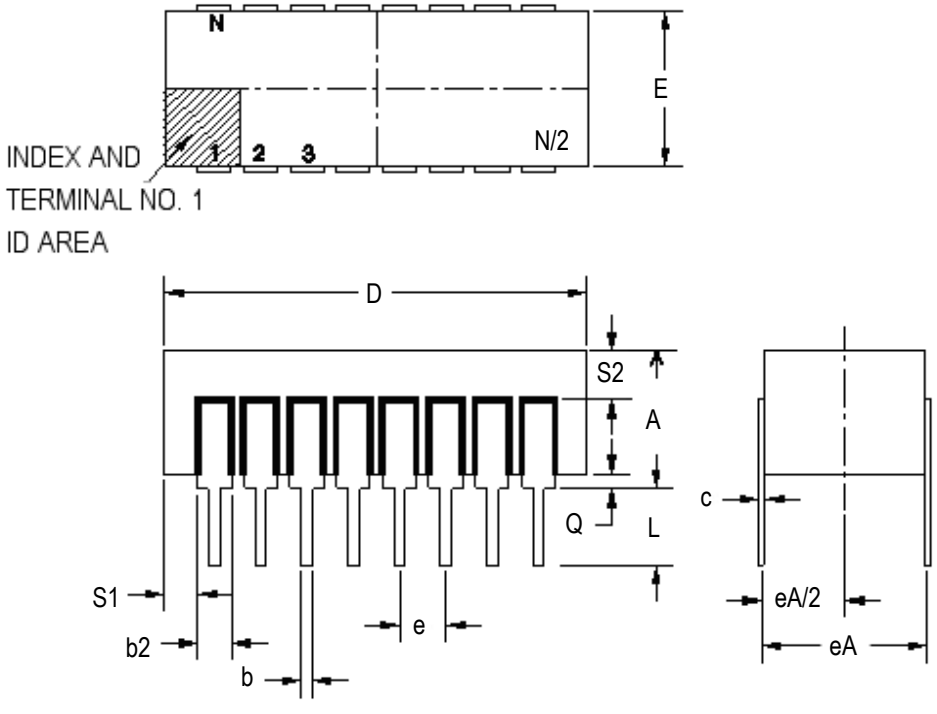
1. External 4.7 kΩ pull-up resistor.
2. External 2 kΩ pull-up resistor continuos SCLK (DASHED LINE) when 14/8/CLK (CONTROL) = -5 V; noncontinuous when 14/8/CLK (CONTROL) = 0 V.



16 Pin Rad-Pak® Flat Package

Symbol	Dimension		
	Min	Nom	Max
A	0.115	0.135	0.150
b	0.015	0.017	0.019
c	0.004	0.005	0.007
D	0.407	0.415	0.423
E	0.275	0.280	0.285
E1	--	--	0.500
E2	0.150	0.156	0.162
E3	0.030	0.062	--
e		0.050 BSC	
L	0.325	0.335	0.345
Q	0.020	0.033	0.045
S1	0.005	0.024	0.045
N		16	

Note: All dimensions in inches
The top and bottom of the package connected to -V.



16 Pin Rad-Pak® Dual In Line Package

Symbol	Dimension		
	Min	Nom	Max
A	--	0.157	0.200
b	0.014	0.018	0.026
b2	0.045	0.047	0.065
c	0.008	0.010	0.018
D	--	0.800	0.840
E	0.220	0.295	0.310
eA	0.300 BSC		
eA/2	0.150 BSC		
e	0.100 BSC		
L	0.135	0.145	0.155
Q	0.000	0.002	0.060
S1	0.005	0.027	--
S2	0.005	--	--
N	16		

Note: All dimensions in inches
The top and bottom of the package connected to -V.

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. DDC verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and DDC assumes no responsibility for the use of this information.

DDC's products are not authorized for use as critical components in life support devices or systems without express written approval from DDC.

Any claim against DDC must be made within 90 days from the date of shipment from DDC.
DDC liability shall be limited to replacement of defective parts.

Product Ordering Options