440GRx

Preliminary Data Sheet

PowerPC 440GRx Embedded Processor

Features

- PowerPC® 440 processor operating up to 667 MHz with 32 KB I-cache and D-cache with parity checking.
- 16 KB of on-chip SRAM.
- Selectable processor:bus clock ratios of N:1, N:2.
- Dual bridged Processor Local Buses (PLBs) with 64- and 128-bit widths.
- Double Data Rate 2/1 (DDR2/1) Synchronous DRAM (SDRAM) interface operating up to 166 MHz (333 MHz data transfer rate) with optional ECC.
- DMA support for external peripherals, internal UART and memory.
- PCI V2.2 interface (3.3 V only). Thirty-two bits at up to 66 MHz.
- Programmable interrupt controller supports interrupts from a variety of sources.
- Programmable General Purpose Timers (GPT).
- Two Ethernet 10/100/1000 Mbps half- or full-duplex interfaces. Operational modes supported are with packet reject, Jumbo frames, and interrupt coalescing.
- Up to four serial ports (16750 compatible UART).
- External peripheral bus (32-bit data) for up to six devices with external mastering.
- Two IIC interfaces (one with bootstrap capability).
- NAND Flash interface.
- SPI interface.
- General Purpose I/O (GPIO) interface.
- JTAG interface for board level testing.
- Boot from PCI memory, NOR Flash on the external peripheral bus, or NAND Flash on the NAND Flash interface.
- Optional security feature (PPC440GRx-S).
- Available in RoHS compliant, lead-free package.

Description

Designed specifically to address high-end embedded applications, the PowerPC 440GRx (PPC440GRx) provides a high-performance, low-power solution that interfaces to a wide range of peripherals and incorporates on-chip power management features.

This chip contains a high-performance RISC processor, on-chip SRAM, DDR2/1 SDRAM controller, PCI bus interface, control for external ROM and peripherals, DMA with scatter/gather support, Ethernet ports, serial ports, IIC interfaces, SPI interface, NAND Flash interface, an optional security feature (PPC440GRx-A), and general purpose I/O.

Technology: CMOS Cu-11, 0.13 µm.

Package: 35 mm, 680-ball thermally enhanced plastic ball grid array (TE-PBGA). RoHS compliant package available.

Typical power (estimated): Approximately 3.3 W at 533 MHz.

Supply voltages required: 3.3 V, 2.5 V, 1.8 V (DDR2) or 2.5 V (DDR1), 1.5 V.

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Ordering and PVR Information

For information on the availability of the following parts, contact your local AMCC sales office. For additional information on the part number structure see *Figure 1*.

Product Name	Order Part Number (see **Notes**)	Package	Revision Level	PVR Value	JTAG ID
PPC440GRx	PPC440GRx-SpAfffTs	35mm, 680 TE-PBGA	A	0x216218D0	0x0440F1E1
PPC440GRx	PPC440GRx-NpAfffTs	35mm, 680 TE-PBGA	A	0x216218D4	0x0440F1E1

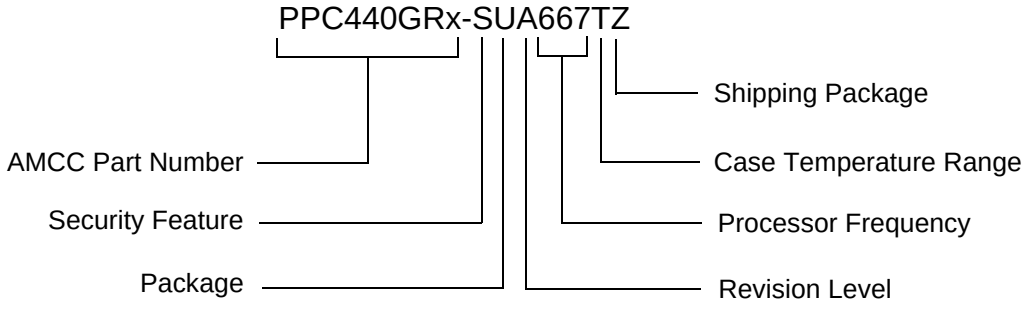
Notes: Characters following the dash (-):

1. S = Security feature present, N = Security feature not present
2. p = Package type: U = lead-free (RoHS compliant), T = contains lead
3. A = Chip revision level A
4. fff = Processor frequency: 400 = 400MHz, 533 = 533MHz, 667 = 667MHz
5. T = Case temperature range of –40°C to +100°C
6. s = Shipping package type: Z = tape-and-reel. Blank = tray

Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. Refer to the *PPC440GRx User's Manual* for details on accessing these registers.

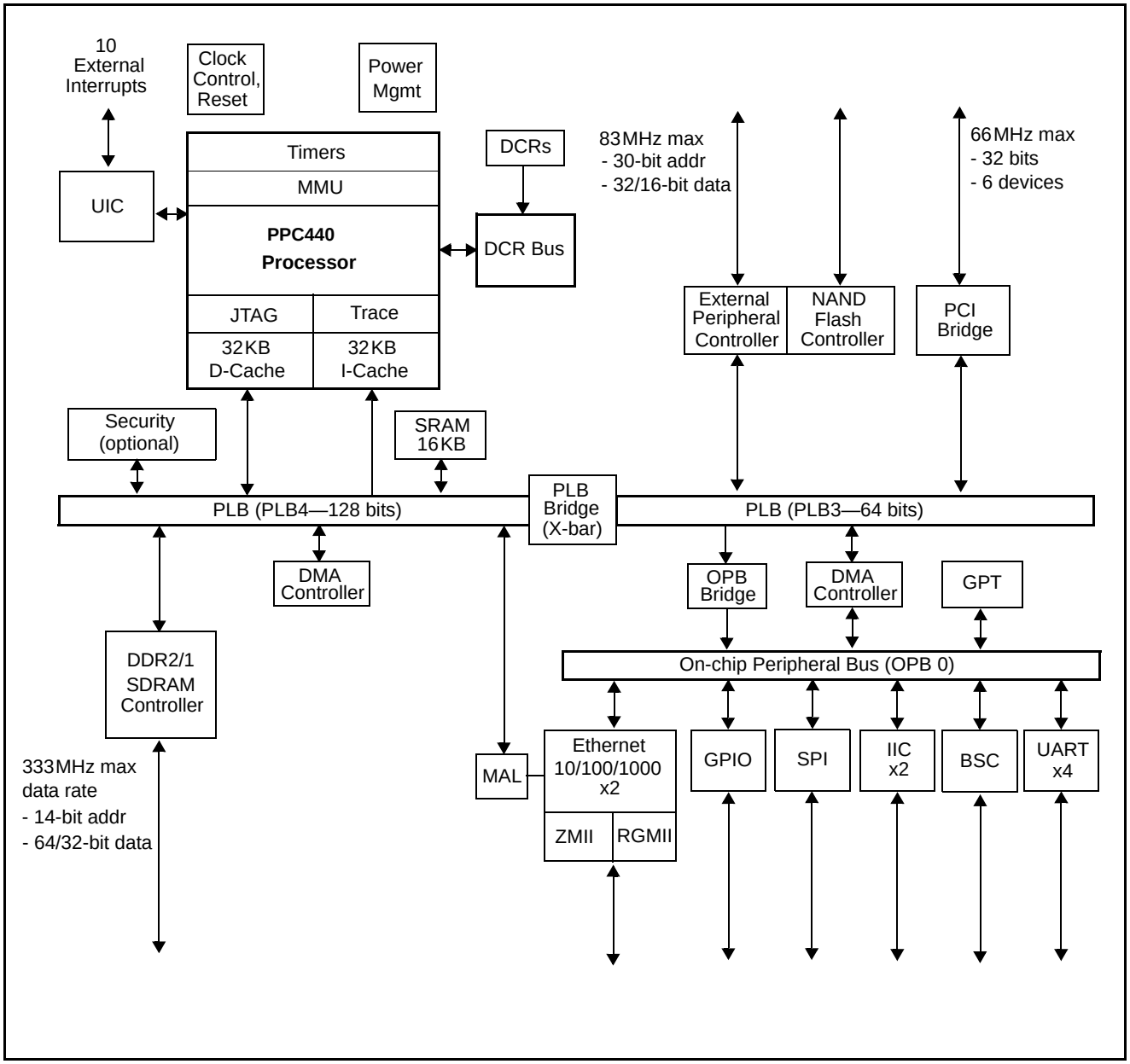
Figure 1. Order Part Number Key



Note: The example P/N above contains the security feature, is lead-free, is capable of running at 667 MHz, and is shipped in tape-and-reel packaging.

Block Diagram

Figure 2. PPC440GRx Functional Block Diagram



The PPC440GRx is a system on a chip (SOC) using IBM CoreConnect Bus™ Architecture.

Address Maps

The PPC440GRx incorporates two address maps. The first is a fixed processor System Memory Address Map. This address map defines the possible contents of various address regions which the processor can access. The second is the DCR Address Map for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC440GRx processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (Sheet 1 of 2)

Function	Sub Function	Start Address	End Address	Size
Total System Memory Address Space		0 0000 0000	1 FFFF FFFF	8GB
Local Memory	DDR SDRAM	0 0000 0000	0 7FFF FFFF	2GB
	Reserved	0 8000 0000	0 E000 FFFF	
On-Chip Memory	SRAM	0 E001 0000	0 E001 3FFF	16KB
	Reserved	0 E001 4000	0 E00F FFFF	
Security (PPC440GRx-S)	Security Function	0 E010 0000	0 E017 FFFF	512KB
	KASUMI Algorithm	0 E018 0000	0 E018 07FF	2KB
	Reserved	0 E018 0800	1 7FFF FFFF	
PCI [1]	Memory	1 8000 0000	1 BFFF FFFF	1GB
EBC [1]	Controller	1 C000 0000	1 DFFF FFFF	512MB
	Reserved	1 E000 0000	1 E7FF FFFF	
PCI [1]	I/O	1 E800 0000	1 E800 FFFF	64KB
	Reserved	1 E801 0000	1E87F FFFF	
	I/O	1 E880 0000	1 EBFF FFFF	56MB
	Reserved	1 EC00 0000	1 EEBF FFFF	
	Configuration Registers	1 EEC0 0000	1 EEC0 0007	8B
	Reserved	1 EEC0 0008	1 EECF FFFF	
	Interrupt Ack/Special Cycle	1 EED0 0000	1 EED0 0003	4B
	Reserved	1 EED0 0004	1 EF3F FFFF	
	Local Configuration Registers	1 EF40 0000	1 EF40 003F	64B
	Reserved	1 EF40 0040	1 EF4F FFFF	

Table 1. System Memory Address Map (Sheet 2 of 2)

Function	Sub Function	Start Address	End Address	Size
Internal Peripherals	Reserved	1 EF50 0000	1 EF5F FFFF	
	General Purpose Timer	1 EF60 0000	1 EF60 01FF	512B
	Reserved	1 EF60 0200	1 EF60 02FF	
	UART0	1 EF60 0300	1 EF60 0307	8B
	Reserved	1 EF60 0308	1 EF60 03FF	
	UART1	1 EF60 0400	1 EF60 0407	8B
	Reserved	1 EF60 0408	1 EF60 04FF	
	UART2	1 EF60 0500	1 EF60 0507	8B
	Reserved	1 EF60 0508	1 EF60 05FF	
	UART3	1 EF60 0600	1 EF60 0607	8B
	Reserved	1 EF60 0608	1 EF60 06FF	
	IIC0	1 EF60 0700	1 EF60 071F	32B
	Reserved	1 EF60 0720	1 EF60 07FF	
	IIC1	1 EF60 0800	1 EF60 081F	32B
	Reserved	1 EF60 0820	1 EF60 08FF	
	SPI	1 EF60 0900	1 EF60 0906	6B
	Reserved	1 EF60 0907	1 EF60 09FF	
	OPB0 Arbiter	1 EF60 0A00	1 EF60 0A3F	64B
	Reserved	1 EF60 0A40	1 EF60 0AFF	
	GPIO0 Controller	1 EF60 0B00	1 EF60 0B7F	128B
	Reserved	1 EF60 0B80	1 EF60 0BFF	
	GPIO1 Controller	1 EF60 0C00	1 EF60 0C7F	128B
	Reserved	1 EF60 0C80	1 EF60 0CFF	
	Ethernet PHY ZMII	1 EF60 0D00	1 EF60 0D0F	16B
	Reserved	1 EF60 0D10	1 EF60 0DFF	
	Ethernet 0 Controller	1 EF60 0E00	1 EF60 0E77	120B
	Reserved	1 EF60 0E78	1 EF60 0EFF	
	Ethernet 1 Controller	1 EF60 0F00	1 EF60 0F77	120B
	Reserved	1 EF60 0F78	1 EF60 0FFF	
	Ethernet PHY RGMII	1 EF60 1000	1 EF60 1103	264B
	Reserved	1 EF60 1080	1 EFFF FFFF	
EBC [1]		1 F000 0000	1 FFDF FFFF	254MB
Boot space	EBC Bank 0 or PCI	1 FFE0 0000	1 FFFF FFFF	2MB

Notes:

1. EBC and PCI are relocatable, but this map reflects the suggested configuration.

Table 2. DCR Address Map

Function	Start Address	End Address	Size
Total DCR Address Space[1]	000	3FF	1KW (4KB)[1]
By function:			
Reserved	000	00B	
Clocking Power On Reset (CPR0)	00C	00D	2W
System DCRs (SDR0)	00E	00F	2W
Memory Controller (SDRAM0)	010	011	2W
External Bus Controller (EBC0)	012	013	2W
Reserved	014	01F	
PLB4-to-PLB3 Bridge Out	020	02F	16W
PLB3-to-PLB4 Bridge In	030	03F	16W
Reserved	040	06F	
PLB3 Arbiter	070	07F	16W
PLB4 Arbiter	080	08F	16W
PLB3-to-OPB0 Bridge	090	09F	16W
Reserved	0A0	0AF	
Power Management	0B0	0B7	8W
Reserved	0B8	0BF	
Interrupt Controller 0	0C0	0CF	16W
Interrupt Controller 1	0D0	0DF	16W
Interrupt Controller 2	0E0	0EF	16W
Power Management 1	0F0	0F7	8W
Reserved	0F8	0FF	
DMA-to-PLB3 Controller	100	13F	64W
Reserved	140	17F	
Ethernet MAL	180	1FF	128W
Reserved	200	2FF	
DMA-to-PLB4 Controller	300	33F	64W
Reserved	340	37F	
On Chip Memory (SRAM Controller)	380	38F	16W
Reserved	390	3FF	

Notes:

1. DCR addresses are 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register. One kiloword (1024W) equals 4KB (4096 B).

PowerPC 440 Processor

The PowerPC 440 processor is designed for high-end applications: RAID controllers, SAN, iSCSI, routers, switches, printers, set-top boxes, etc. It implements the Book E PowerPC embedded architecture and uses the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- Up to 667 MHz operation
- PowerPC Book E architecture
- 32 KB I-cache, 32 KB D-cache
  - UTLB Word Wide parity on data and tag address parity with exception force
- Three logical regions in D-cache: locked, transient, normal
- D-cache full line flush capability
- 41-bit virtual address, 36-bit (64 GB) physical address
- Superscalar, out-of-order execution
- 7-stage pipeline
- 3 execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB with optional parity
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- 24 DSP instructions
  - Single cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply
  - 16 x 16 -> 32-bit MAC

SRAM Controller

The internal SRAM controller (ISC) supports the following features:

- One bank (Bank 0) of 16 KB configurable as 4 KB, 8 KB or 16 KB (128 bits wide)
- 128-bit slave attachment addressable by any PLB master
- Transfers by PLB slave cycles:
  - Single-beat read and write (1 to 8 bytes for 64-bit masters, 1 to 16 bytes for 128-bit masters)
  - 4-word line read and write
  - 8-word line read and write
  - Double word read and write bursts for 64-bit masters
  - Quadword read and write bursts for 128-bit masters
  - Slave-terminated double word and quadword fixed length bursts
  - Master-terminated variable length bursts
- Guarded memory access on 4 KB boundaries
- Data parity checking
- Data transfers occur at PLB bus speeds.
- Power management

Internal Buses

The PowerPC 440GRx features four standard internal buses: two Processor Local Buses (PLBs), one On-Chip Peripheral Buses (OPBs), and the Device Control Register Bus (DCR). The high performance, high bandwidth cores such as the PowerPC 440 processor, the DDR SDRAM memory controller, and the PCI bridge connect to the PLBs. OPB0 hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor and the other on-chip cores.

Features include:

- PLB4 (128-bit)
  - 128-bit implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 36-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte-enable capability supporting unaligned transfers
  - 32- and 64-byte burst transfers
  - 166MHz, maximum 5.3GB/s (simultaneous read and write)
  - Processor:bus clock ratios of N:1 and N:2
- PLB3 (64-bit)
  - 64-bit implementation of the PLB architecture
  - 32-bit address
  - 166MHz (1:1 ratio with PLB4), maximum 1.3GB/s (no simultaneous read and write)
- OPBs (OPB0)
  - 32-bit data path
  - 32-bit address
  - 83MHz
- DCR
  - 32-bit data path
  - 10-bit address

Security Function (optional)

The built-in security function (PPC440GRx-S only) is a cryptographic engine attached to the 128-bit PLB with built-in DMA and interrupt controllers.

Features include:

- Federal Information Processing Standard (FIPS) 140-2 design
- Support for an unlimited number of Security Associations (SA)
- Different SA formats for each supported protocol (IPsec/SSL/TLS/sRTP)
- Internet Protocol Security (IPSec) features
  - Full packet transforms (ESP & AH)
  - Complete header and trailer processing (IPv4 and IPv6)
  - Multi-mode automatic padding
  - "Mutable bit" handler for AH, including IPv4 option and IPv6 extension headers
- Secure Socket Layer (SSL) and Transport Layer Security (TLS) features
  - Packet transforms
  - One-pass hash-then-encrypt for SSL and TLS packet transforms for inbound packet using Stream Cipher
- Secure Real-Time Protocol (sRTP) features
  - Packet transforms
  - ROC removal and TAG insertion
  - Variable bypass offset of header length per packet
- IPsec/SSL security acceleration engine
- DES, 3DES, AES, ARC-4 encryption
- MD-5, SHA-1 hashing, HMAC encrypt-hash and hash-decrypt, and KASUMI

- Public key acceleration for RSA, DSA and Diffie-Hellman
- True or pseudo random number generators
  - Non-deterministic true random numbers
  - Pseudo random numbers with lengths of 8B or 16B
  - ANSI X9.17 Annex C compliant using a DES algorithm
- Interrupt controller
  - Fifteen programmable, maskable interrupts
  - Initiate commands via an input interrupt
  - Sixteen programmable interrupts indicating completion of certain operations
  - All interrupts mapped to one level- or edge-sensitive programmable interrupt output
- DMA controller
  - Autonomous, 4-channel
  - 1024-words (32 bits/word) per DMA transfer
  - Scatter/gather capability with byte aligned addressing

KASUMI Algorithm (optional)

- Key scheduling hardware
- *f8* and *f9* algorithm support
- Automatic data padding mechanism for *f9* algorithm
- KASUMI encryption and decryption modes
- 32-bit slave interface
- Fully synchronous to PLB clock

PCI Controller

The PCI interface allows connection of PCI devices to the PowerPC processor and local memory. This interface is designed to Version 2.2 of the PCI Specification and supports 32- bit PCI devices.

Reference Specifications:

- PowerPC CoreConnect Bus (PLB) Specification Version 3.1
- PCI Specification Version 2.2
- PCI Bus Power Management Interface Specification Version 1.1

Features include:

- PCI 2.2
  - Frequency to 66MHz
  - 32-bit bus
- PCI Host Bus Bridge or an Adapter Device's PCI interface
- Internal PCI arbitration function, supporting up to six external devices, that can be disabled for use with an external arbiter
- Support for Message Signaled Interrupts
- Simple message passing capability
- Asynchronous to the PLB
- PCI Power Management 1.1
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI bus memory
- Error tracking/status
- Supports initiation of transfers of the following types:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (type 0 and type 1)
  - Single beat special cycles

DDR2/1 SDRAM Memory Controller

The Double Data Rate 2/1 (DDR2/1) SDRAM memory controller supports industry standard discrete devices that are compatible with both the DDR1 or DDR2 specifications. The correct I/O supply voltage must be provided for the two types of DDR devices: DDR1 devices require +2.5V and DDR2 devices require +1.8V.

Global memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:
- 32-bit memory interface for DDR1
- 32- or 64-bit memory interface for DDR2
- Optional Error Checking and Correcting (ECC)
- 2.6-GB/s peak data rate
- Two memory banks of up to 1 GB each
- Maximum capacity of 2GB
- Support for 256-Mb, 512-Mb, and 1-Gb DDR devices, with CAS latencies of 2 or 3
- Support for DDR266/333 and DDR2-266/333.
  (Faster parts may be used but must be clocked no faster than 166MHz)
- Page mode accesses (up to 16 open pages) with configurable paging policy
- Programmable address mapping and timing
- Software initiated self-refresh
- Power management (self-refresh, suspend, sleep)
- One or two chip selects

External Peripheral Bus Controller (EBC)

Features include:
- Up to six ROM, EPROM, SRAM, Flash memory, and slave peripheral I/O banks supported
- Up to 83MHz operation
- Burst and non-burst devices
- 32-bit byte-addressable data bus
- Data parity
- 30-bit address
- Peripheral Device pacing with external “Ready”
- Latch data on Ready, synchronous or asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- External DMA Slave Support
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for access

Ethernet Controller

Ethernet support provided by the PPC440GRx interfaces to the physical layer but the PHY is not included on the chip:

- Two 10/100/1000 interfaces running in full- and half-duplex modes providing:
  - One Gigabit Media Independent Interface (GMII)
  - One Media Independent Interface (MII)
  - Two Reduced Gigabit MII (RGMII)
  - Two Serial MII (SMII) at 100/10 Mbps.
  - Packet reject support
  - Jumbo frame support
  - DMA capability
  - Interrupt coalescence

DMA-to-PLB3 (64-bit) Controller

This DMA controller provides a DMA interface between OPB0 and PLB3.

Features include:

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 32-byte buffer
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

Serial Ports (UART)

Features include:

- Up to four ports in the following combinations:
  - One 8-pin (UART0)
  - Two 4-pin (UART0 and UART1)
  - One 4-pin (UART0) and two 2-pin (UART1 and UART2)
  - Four 2-pin (UART0, UART1, UART2, and UART3)
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA function on PLB3

IIC Bus Controller

Features include:

- Two IIC interfaces provided
- Support for Philips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocols
- Programmable error recovery
- Includes an integrated bootstrap controller (BSC) that is multiplexed with the second IIC interface

Serial Peripheral Controller (SPI/SCP)

The Serial Peripheral Interface (also known as the Serial Communications Port) is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other serial devices. The SCP is a master on the serial port supporting a 3-wire interface (receive, transmit, and clock), and is a slave on the OPB.

Features include:

- Three-wire serial port interface
- Full-duplex synchronous operation
- SCP bus master
- OPB bus slave
- Programmable clock rate divider
- Clock inversion
- Reverse data
- Local data loop back for test

NAND Flash Controller

The NAND Flash controller provides a simple interface between the EBC and up to four separate external NAND Flash devices. It provides both direct command, address, and data access to the external device as well as a memory-mapped linear region that generates data accesses. NAND Flash data is transferred on the peripheral data bus.

Features include:

- One to four banks supported on EBC
- Direct interface to:
  - Discrete NAND Flash devices (up to four devices)
  - SmartMedia Card socket (22-pins)
- Device sizes:
  - 4MB and larger supported for read/write access
  - 4MB to 256MB for boot-from-NAND flash (size supported depends on addressing mode)
- (512 + 16)-B or (2K + 64)-B page sizes supported
- Boot-from-NAND
  - Execute up to 4KB of boot code out of first block.
  - Automatic page read accesses performed based on device configuration and addressing mode.
- ECC provides single-bit error correction and double-bit error detection in each 256B of stored data

General Purpose Timers (GPT)

Provides a separate time base counter and additional system timers in addition to those defined in the processor.

Features include:
- 32-bit Time Base Counter driven by the OPB bus clock
- Seven 32-bit compare timers

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses.
- 64 GPIOs are multiplexed with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is separately programmable to emulate an open drain driver (that is, drives to zero, tri-stated if output bit is 1).

Universal Interrupt Controller (UIC)

Two Universal Interrupt Controllers (UIC) are employed. They provide control, status, and communications necessary between the external and internal sources of interrupts and the on-chip PowerPC processor.

Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

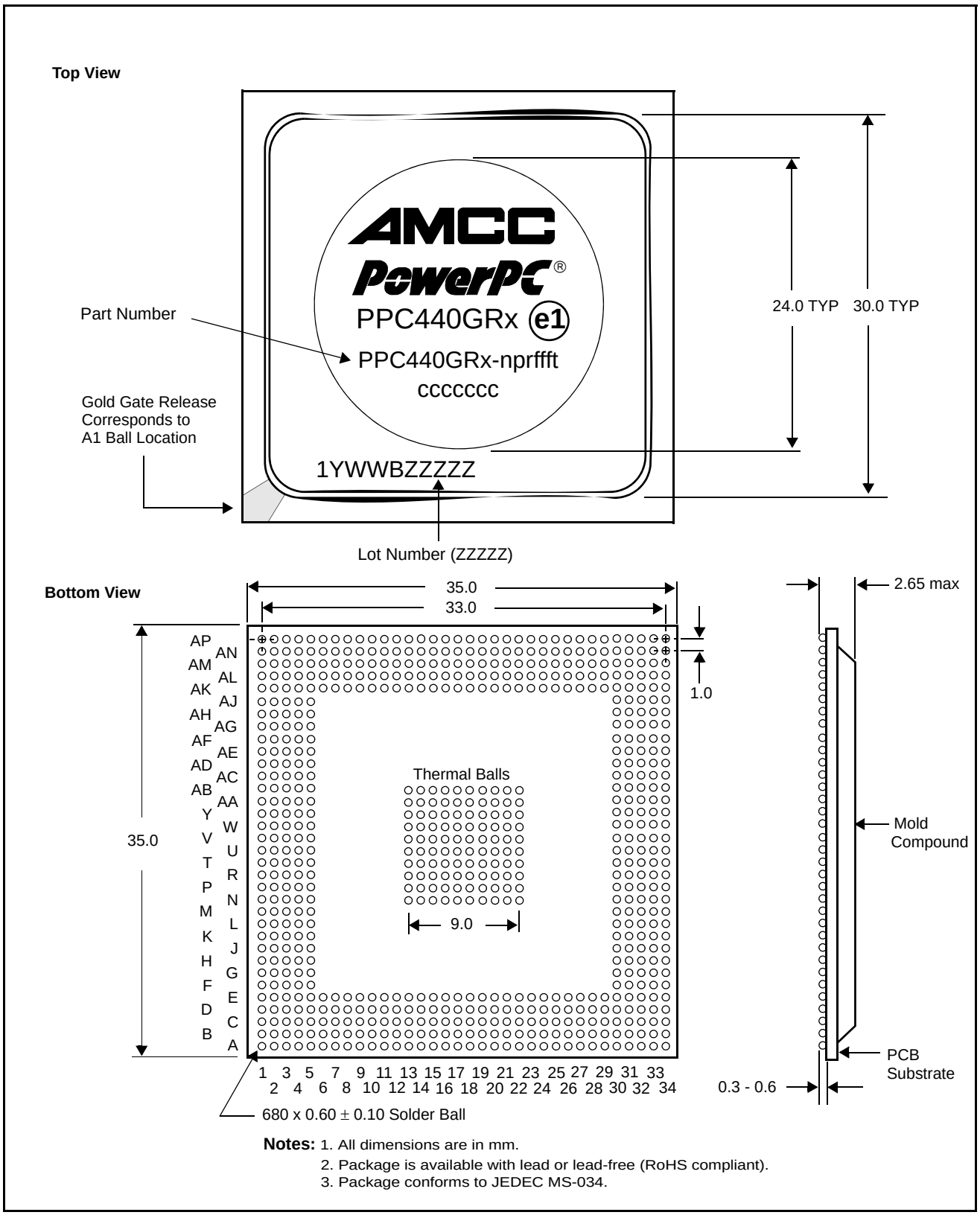
Features include:
- 10 external interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to the on-chip processor
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

JTAG

Features include:
- IEEE 1149.1 Test Access Port
- JTAG Boundary Scan Description Language (BSDL)
- Refer to **http://www.amcc.com/Embedded/Partners** for a list of AMCC partners supplying probes for use with this port.

Package Diagram

Figure 3. 35mm, 680-Ball TE-PBGA Package



Assembly Recommendations

Table 3. Recommended Reflow Soldering Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb Free Reflow Assembly
Average ramp-up rate	3°C/second max	3°C/second max
Preheat • Temperature Min • Temperature Max • Time (min to max)	 100°C 150°C 60-120 Seconds	 150°C 180°C 60-120 Seconds
Time Maintained Above: • Temperature • Time	 183°C 60-150 Seconds	 230°C 30-50 Seconds
Peak Temperature	225 +0/-5°C	260 +5/-0°C
Time within 5°C of Actual Peak Temperature	10-30 Seconds	10-20 Seconds
Ramp-down Rate	6°C/Second Max	6°C/Second Max
Time 25°C to Peak Temperature	6 Minutes Max	8 Minutes Max

Table 4. JEDEC Moisture Sensitivity Level and Ball Composition

	Sn-Pb Eutectic Assembly	Pb Free Reflow Assembly
MSL Level	3	3
Solder Ball Metallurgy	63Sn/37Pb	Sn/4Ag/05Cu

Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and alternate signals in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in *Table 9* on page 56 where the signals in the indicated interface group begin. In cases where signals in the same interface group (for example, Ethernet) have different names to distinguish variations in the mode of operation, the names are separated by a comma with the primary mode name appearing first. In cases where the signals have the same function but are associated with different ports (for example, UART), the signals are separated by a slash (/). These signals are listed only once, and appear alphabetically by the primary mode or primary port name.

Alphabetical Signal List

Table 5. Signals Listed Alphabetically (Sheet 1 of 26)

Signal Name	Ball	Interface Group	Page
AGND	AP25	Power	63
AV_{DD}	AP24		
BA0	AJ03	DDR SDRAM	57
BA1	AK03		
BA2	AP08		
$\overline{\text{BankSel0}}$	AH02	DDR SDRAM	57
$\overline{\text{BankSel1}}$	AH01		
[BusReq]GPIO31	P04	External Master Peripheral	60
$\overline{\text{CAS}}$	AH04	DDR SDRAM	57
ClkEn	AN09	DDR SDRAM	57
DM0	AL21	DDR SDRAM	57
DM1	AM18		
DM2	AP15		
DM3	AL14		
DM4	AE04		
DM5	AB03		
DM6	Y01		
DM7	U03		
DM8	AN10		
[DMAAck0][IRQ8]GPIO47	T34	External Slave Peripheral	59
[DMAAck1][IRQ4]GPIO44	V32		
[DMAAck2][PerAddr06]GPIO01	C25		
[DMAAck3][PerAddr03]GPIO04	D26		
[DMAReq0][IRQ7]GPIO46	U32	External Slave Peripheral	59
[DMAReq1]IRQ5[ModeCtrl]	W34		
[DMAReq2][PerAddr07]GPIO00	B25		
[DMAReq3][PerAddr04]GPIO03	A26		

Table 5. Signals Listed Alphabetically (Sheet 2 of 26)

Signal Name	Ball	Interface Group	Page
DQS0	AM21	DDR SDRAM	57
DQS1	AM19		
DQS2	AL16		
DQS3	AM13		
DQS4	AE03		
DQS5	AB04		
DQS6	W04		
DQS7	U04		
DQS8	AP10		
DrvrInh1	R02	System	62
[DrvrInh2]$\overline{\text{Halt}}$	E32		
EAGND	AP27	Power	63
EAV_{DD}	AP28		
ECC0	AM11	DDR SDRAM	57
ECC1	AL11		
ECC2	AM09		
ECC3	AL09		
ECC4	AP11		
ECC5	AN11		
ECC6	AM10		
ECC7	AP09		
[EOT0/TC0][IRQ9]GPIO48	T32	External Slave Peripheral	59
[EOT1/TC1][IRQ6]GPIO45	U33		
[EOT2/TC2][PerAddr05]GPIO02	D25		
[EOT3/TC3][PerAddr02]GPIO05	C26		
EOV_{DD}	AA22	Power	63
EOV_{DD}	AB21		
EOV_{DD}	AC33		
EOV_{DD}	AF30		
EOV_{DD}	AH30		
EOV_{DD}	AJ30		
EOV_{DD}	AK26		
EOV_{DD}	AK28		
EOV_{DD}	AK29		
EOV_{DD}	AK33		
EOV_{DD}	AN23		
EOV_{DD}	AN30		
[$\overline{\text{ExtAck}}$]GPIO30	M03	External Master Peripheral	60

Table 5. Signals Listed Alphabetically (Sheet 3 of 26)

Signal Name	Ball	Interface Group	Page
[$\overline{\text{ExtReq}}$]GPIO27	A04	External Master Peripheral	60
$\overline{\text{ExtReset}}$	D06	External Master Peripheral	60
GMCCD, GMC1RxClk	AJ32	Ethernet	58
GMCCrs, GMC1TxClk	AK32		
GMCGTxClk, GMC0TxClk	AM27		
GMCMDClk	AL34		
GMCMDIO	AK34		
GMCRefClk, SMIIRefClk	AJ33		
GMCRxClk, GMC0RxClk SMIISync	AN28		
GMCRxD0, GMC0RxD0, TBIRxD0, RTBI0RxD0, SMII0RxD	AL28		
GMCRxD1, GMC0RxD1 SMII1RxD	AP29		
GMCRxD2, GMC0RxD2	AM28		
GMCRxD3, GMC0RxD3	AN29		
GMCRxD4, GMC1RxD0	AM29		
GMCRxD5, GMC1RxD1	AP30		
GMCRxD6, GMC1RxD22	AP31		
GMCRxD7, GMC1RxD3	AM30		
GMCRxDV, GMC0RxCtl	AJ31		
GMCRxEr, GMC1RxCtl	AL33		
GMCTxClk	AL27		
GMCTxD0, GMC0TxD0 SMII0TxD	AL24		
GMCTxD1, GMC0TxD, SMII1TxD	AN25		
[GMCTxD2, GMC0TxD2] GPIO24	AM25		
[GMCTxD3, GMC0TxD3] GPIO25	AL25		
[GMCTxD4, GMC1TxD0] GPIO16	AP26		
[GMCTxD5, GMC1TxD1] GPIO17	AL26		
[GMCTxD6, GMC1TxD2] GPIO18	AN26		
[GMCTxD7, GMC1TxD3] GPIO19	AM26		
GMCTxEr, GMC1TxCtl	AM24		
GMCTxEn, GMC0TxCtl	AN24		

Table 5. Signals Listed Alphabetically (Sheet 4 of 26)

Signal Name	Ball	Interface Group	Page
GND	A01		
GND	A02		
GND	A03		
GND	A28		
GND	A32		
GND	A33		
GND	A34		
GND	B01		
GND	B02		
GND	B03		
GND	B04		
GND	B08		
GND	B16		
GND	B19		
GND	B26		
GND	B27		
GND	B31		
GND	B32		
GND	B33	Power	63
GND	B34		
GND	C02		
GND	C03		
GND	C04		
GND	C31		
GND	C32		
GND	C33		
GND	C34		
GND	D03		
GND	D04		
GND	D05		
GND	D30		
GND	D31		
GND	D32		
GND	D33		
GND	E05		
GND	E08		
GND	E10		

Table 5. Signals Listed Alphabetically (Sheet 5 of 26)

Signal Name	Ball	Interface Group	Page
GND	E16		
GND	E18		
GND	E19		
GND	E25		
GND	E27		
GND	E30		
GND	E31		
GND	H01		
GND	H02		
GND	H05		
GND	H30		
GND	H33		
GND	K01		
GND	K04		
GND	K05		
GND	K30		
GND	J03		
GND	M01		
GND	M04	Power	63
GND	N01		
GND	N04		
GND	N13		
GND	N15		
GND	N17		
GND	N18		
GND	N20		
GND	N22		
GND	P14		
GND	P15		
GND	P17		
GND	P18		
GND	P20		
GND	P21		
GND	R13		
GND	R14		
GND	R15		
GND	R16		

Table 5. Signals Listed Alphabetically (Sheet 6 of 26)

Signal Name	Ball	Interface Group	Page
GND	R17		
GND	R18		
GND	R19		
GND	R20		
GND	R21		
GND	R22		
GND	T02		
GND	T05		
GND	T15		
GND	T16		
GND	T17		
GND	T18		
GND	T19		
GND	T20		
GND	T30		
GND	T33		
GND	U05		
GND	U13		
GND	U14	Power	63
GND	U15		
GND	U16		
GND	U17		
GND	U18		
GND	U19		
GND	U20		
GND	U21		
GND	U22		
GND	V13		
GND	V14		
GND	V15		
GND	V16		
GND	V17		
GND	V18		
GND	V19		
GND	V20		
GND	V21		
GND	V22		

Table 5. Signals Listed Alphabetically (Sheet 7 of 26)

Signal Name	Ball	Interface Group	Page
GND	V30		
GND	W02		
GND	W05		
GND	W15		
GND	W16		
GND	W17		
GND	W18		
GND	W19		
GND	W20		
GND	W30		
GND	W33		
GND	Y13		
GND	Y14		
GND	Y15		
GND	Y16		
GND	Y17		
GND	Y18		
GND	Y19		
GND	Y20	Power	63
GND	Y21		
GND	Y22		
GND	AA14		
GND	AA15		
GND	AA17		
GND	AA18		
GND	AA20		
GND	AA21		
GND	AB13		
GND	AB15		
GND	AB17		
GND	AB18		
GND	AB20		
GND	AB22		
GND	AD01		
GND	AE05		
GND	AE30		
GND	AG02		

Table 5. Signals Listed Alphabetically (Sheet 8 of 26)

Signal Name	Ball	Interface Group	Page
GND	AG05		
GND	AG30		
GND	AG33		
GND	AJ01		
GND	AK04		
GND	AK05		
GND	AK08		
GND	AK10		
GND	AK16		
GND	AK17		
GND	AK19		
GND	AK25		
GND	AK27		
GND	AK30		
GND	AK31		
GND	AL03		
GND	AL04		
GND	AL05		
GND	AL06	Power	63
GND	AL29		
GND	AL30		
GND	AL31		
GND	AL32		
GND	AM01		
GND	AM02		
GND	AM03		
GND	AM04		
GND	AM31		
GND	AM32		
GND	AM33		
GND	AM34		
GND	AN01		
GND	AN02		
GND	AN03		
GND	AN04		
GND	AN08		
GND	AN16		

Table 5. Signals Listed Alphabetically (Sheet 9 of 26)

Signal Name	Ball	Interface Group	Page
GND	AN19	Power	63
GND	AN27		
GND	AN31		
GND	AN32		
GND	AN33		
GND	AN34		
GND	AP01		
GND	AP02		
GND	AP03		
GND	AP32		
GND	AP33		
GND	AP34		

Table 5. Signals Listed Alphabetically (Sheet 10 of 26)

Signal Name	Ball	Interface Group	Page
GPIO00[PerAddr07][DMAReq2]	B25	System	62
GPIO01[PerAddr06][DMAAck2]	C25		
GPIO02[PerAddr05][EOT2/TC2]	D25		
GPIO03[PerAddr04][DMAReq3]	A26		
GPIO04[PerAddr03][DMAAck3]	D26		
GPIO05[PerAddr02][EOT3/TC3]	C26		
GPIO06[$\overline{\text{PerCS1}}$][$\overline{\text{NFCE1}}$]	B09		
GPIO07[$\overline{\text{PerCS2}}$][$\overline{\text{NFCE2}}$]	D09		
GPIO08[$\overline{\text{PerCS3}}$][$\overline{\text{NFCE3}}$]	D08		
GPIO09[$\overline{\text{PerCS4}}$]	A09		
GPIO10[$\overline{\text{PerCS5}}$]	A08		
GPIO11[PerErr]	C07		
GPIO12[$\overline{\text{NFREn}}$]	D17		
GPIO13[$\overline{\text{NFWEn}}$]	A16		
GPIO14[NFCLE]	A18		
GPIO15[NFALE]	B17		
GPIO16[GMCTxD4, GMC1TxD0]	AP26		
GPIO17[GMCTxD5, GMC1TxD1]	AL26		
GPIO18[GMCTxD6, GMC1TxD2]	AN26		
GPIO19[GMCTxD7, GMC1TxD3]	AM26		
GPIO20[RejectPkt0]	AM23		
GPIO21[RejectPkt1]	AL23		
GPIO22[$\overline{\text{NFRdyBusy}}$]	A17		
GPIO23[SCPDO]	AB31		
GPIO24[GMCTxD2, GMC0TxD2]	AM25		
GPIO25[GMCTxD3, GMC0TxD3]	AL25		
[GPIO26]IIC0SData	AB33		
GPIO27[USB2RxErr][$\overline{\text{ExtReq}}$]	A04		
GPIO28[USB2TxVal]	C06		
GPIO29[USB2Susp][HoldAck]	C05		
GPIO30[USB2XcvrSel][$\overline{\text{ExtAck}}$]	M03		
GPIO31[USB2TermSel][BusReq]	P04		

Table 5. Signals Listed Alphabetically (Sheet 11 of 26)

Signal Name	Ball	Interface Group	Page
GPIO32[USB2OM0][PerDataPar2]	R03	System	62
GPIO33[USB2OM1][PerDataPar3]	R04		
GPIO34[$\overline{\text{UART0_DCD}}$/$\overline{\text{UART1_CTS}}$/UART2_Tx]	C28		
GPIO35[$\overline{\text{UART0_DSR}}$/$\overline{\text{UART1_RTS}}$/UART2_Rx]	C29		
GPIO36[$\overline{\text{UART0_CTS}}$/UART3_Rx][PerDataPar0]	A29		
GPIO37[$\overline{\text{UART0_RTS}}$/UART3_Tx][PerDataPar1]	B29		
GPIO38[$\overline{\text{UART0_DTR}}$/UART1_Tx]	D28		
GPIO39[$\overline{\text{UART0_RI}}$/UART1_Rx]	B28		
GPIO40[IRQ0]	AD33		
GPIO41[IRQ1]	AC31		
GPIO42[IRQ2]	AD34		
GPIO43[IRQ3]	U34		
GPIO44[IRQ4][DMAAck1]	V32		
GPIO45[IRQ6][EOT1/TC1]	U33		
GPIO46[IRQ7][DMAReq0]	U32		
GPIO47[IRQ8[DMAAck0]	T34		
GPIO48[IRQ9][EOT0/TC0]	T32		
GPIO49[TrcBS0]	AE34		
GPIO50[TrcBS1]	AE32		
GPIO51[TrcBS2]	AE33		
GPIO52[TrcES0]	AE31		
GPIO53[TrcES1]	AF34		
GPIO54[TrcES2]	AF33		
GPIO55[TrcES3]	AF32		
GPIO56[TrcES4]	AF31		
GPIO57[TrcTS0]	AG34		
GPIO58[TrcTS1]	AG31		
GPIO59[TrcTS2]	AH33		
GPIO60[TrcTS3]	AH34		
GPIO61[TrcTS4]	AH32		
GPIO62[TrcTS5]	AJ34		
GPIO63[TrcTS6]	AH31		
$\overline{\text{Halt}}$[DrvrInh2]	E32	System	62
[HoldAck]GPIO29	C05	External Master Peripheral	60
HoldPri[LeakTest]	P01		
HoldReq[RcvrInh]	D07		
IIC0SClk	AB32	IIC0 Peripheral	60
IIC0SData[GPIO26]	AB33		

Table 5. Signals Listed Alphabetically (Sheet 12 of 26)

Signal Name	Ball	Interface Group	Page
[IIC1SClk]SCPClkOut	AC34	IIC1 Peripheral	60
[IIC1SData]SCPDI	AC32		
[IRQ0]GPIO40	AD33	Interrupts	61
[IRQ1]GPIO41	AC31		
[IRQ2]GPIO42	AD34		
[IRQ3]GPIO43	U34		
[IRQ4]GPIO44[DMAAck1]	V32		
IRQ5[ModeCtrl][DMAReq1]	W34		
[IRQ6]GPIO45[EOT1/TC1]	U33		
[IRQ7]GPIO46[DMAReq0]	U32		
[IRQ8]GPIO47[DMAAck0]	T34		
[IRQ9]GPIO48[EOT0/TC0]	T32		
[LeakTest]HoldPri	P01	System	62
LeakTest2	C08		
MemAddr00	AM05	DDR SDRAM	57
MemAddr01	AP04		
MemAddr02	AP05		
MemAddr03	AM06		
MemAddr04	AP06		
MemAddr05	AN06		
MemAddr06	AL07		
MemAddr07	AN07		
MemAddr08	AM07		
MemAddr09	AP07		
MemAddr10	AL02		
MemAddr11	AL08		
MemAddr12	AM08		
MemAddr13	AG04		
MemClkOut	AL01	DDR SDRAM	57
$\overline{\text{MemClkOut}}$	AK01		

Table 5. Signals Listed Alphabetically (Sheet 13 of 26)

Signal Name	Ball	Interface Group	Page
MemData00	AN22	DDR SDRAM	57
MemData01	AP22		
MemData02	AM20		
MemData03	AL20		
MemData04	AL22		
MemData05	AM22		
MemData06	AN21		
MemData07	AP21		
MemData08	AP20		
MemData09	AL18		
MemData10	AN17		
MemData11	AP17		
MemData12	AN20		
MemData13	AP19		
MemData14	AN18		
MemData15	AP18		
MemData16	AM16		
MemData17	AP16		
MemData18	AL15		
MemData19	AP14		
MemData20	AL17		
MemData21	AM17		
MemData22	AN15		
MemData23	AM15		
MemData24	AP13		
MemData25	AN13		
MemData26	AP12		
MemData27	AL12		
MemData28	AM14		
MemData29	AN14		
MemData30	AL13		
MemData31	AM12		

Table 5. Signals Listed Alphabetically (Sheet 14 of 26)

Signal Name	Ball	Interface Group	Page
MemData32	AF03	DDR SDRAM	57
MemData33	AF01		
MemData34	AD04		
MemData35	AD03		
MemData36	AG03		
MemData37	AF02		
MemData38	AE02		
MemData39	AE01		
MemData40	AC03		
MemData41	AC01		
MemData42	AA04		
MemData43	AA03		
MemData44	AD02		
MemData45	AC04		
MemData46	AB01		
MemData47	AB02		
MemData48	Y03		
MemData49	Y02		
MemData50	V04		
MemData51	V03		
MemData52	AA02		
MemData53	AA01		
MemData54	W03		
MemData55	W01		
MemData56	U01		
MemData57	U02		
MemData58	T04		
MemData59	R01		
MemData60	V02		
MemData61	V01		
MemData62	T01		
MemData63	T03		
MemODT0	AH03	DDR SDRAM	57
MemODT1	AG01		
[ModeCtrl]IRQ5[DMAReq1]	W34	System	62

Table 5. Signals Listed Alphabetically (Sheet 15 of 26)

Signal Name	Ball	Interface Group	Page
[NFALE]GPIO15	B17	NAND Flash	61
[$\overline{\text{NFCE0}}$]$\overline{\text{PerCS0}}$	D10		
[$\overline{\text{NFCE1}}$][$\overline{\text{PerCS1}}$]GPIO06	B09		
[$\overline{\text{NFCE2}}$][$\overline{\text{PerCS2}}$]GPIO07	D09		
[$\overline{\text{NFCE3}}$][$\overline{\text{PerCS3}}$]GPIO08	D08		
[NFCLE]GPIO14	A18		
[$\overline{\text{NFRdyBusy}}$]GPIO22	A17		
[$\overline{\text{NFREn}}$]GPIO12	D17		
[$\overline{\text{NFWEn}}$]GPIO13	A16		

Table 5. Signals Listed Alphabetically (Sheet 16 of 26)

Signal Name	Ball	Interface Group	Page
No ball	F06–F29	A physical ball does not exist at these ball coordinates.	NA
No ball	G06–G29		
No ball	H06–H29		
No ball	J06–J29		
No ball	K06–K29		
No ball	L06–L29		
No ball	M06–M29		
No ball	N06–N12		
No ball	N23–N29		
No ball	P06–P12		
No ball	P23–P29		
No ball	R06–R12		
No ball	R23–R29		
No ball	T06–T12		
No ball	T23–T29		
No ball	U06–U12		
No ball	U23–U29		
No ball	V06–V12		
No ball	V23–V29		
No ball	W06–W12		
No ball	W23–W29		
No ball	Y06–Y12		
No ball	Y23–Y29		
No ball	AA06–AA12		
No ball	AA23–AA29		
No ball	AB06–AB12		
No ball	AB23–AB29		
No ball	AC06–AC29		
No ball	AD06–AD29		
No ball	AE06–AE29		
No ball	AF06–AF29		
No ball	AG06–AG29		
No ball	AH06–AH29		
No ball	AJ06–AJ29		

Table 5. Signals Listed Alphabetically (Sheet 17 of 26)

Signal Name	Ball	Interface Group	Page
OV_{DD}	B05	Power	63
OV_{DD}	B12		
OV_{DD}	B23		
OV_{DD}	B30		
OV_{DD}	E02		
OV_{DD}	E06		
OV_{DD}	E07		
OV_{DD}	E09		
OV_{DD}	E17		
OV_{DD}	E26		
OV_{DD}	E28		
OV_{DD}	E29		
OV_{DD}	E33		
OV_{DD}	F05		
OV_{DD}	F30		
OV_{DD}	G05		
OV_{DD}	G30		
OV_{DD}	J04		
OV_{DD}	J05		
OV_{DD}	J30		
OV_{DD}	L01		
OV_{DD}	L02		
OV_{DD}	L04		
OV_{DD}	M02		
OV_{DD}	M33		
OV_{DD}	N14		
OV_{DD}	N21		
OV_{DD}	P13		
OV_{DD}	P22		
OV_{DD}	U30		

Table 5. Signals Listed Alphabetically (Sheet 18 of 26)

Signal Name	Ball	Interface Group	Page
PCIAD00	D29	PCI	56
PCIAD01	A30		
PCIAD02	C30		
PCIAD03	A31		
PCIAD04	D34		
PCIAD05	F31		
PCIAD06	E34		
PCIAD07	F32		
PCIAD08	F33		
PCIAD09	F34		
PCIAD10	G31		
PCIAD11	G33		
PCIAD12	G34		
PCIAD13	H31		
PCIAD14	H32		
PCIAD15	H34		
PCIAD16	L31		
PCIAD17	L33		
PCIAD18	M32		
PCIAD19	M31		
PCIAD20	M34		
PCIAD21	N31		
PCIAD22	N33		
PCIAD23	N32		
PCIAD24	P31		
PCIAD25	P33		
PCIAD26	P32		
PCIAD27	P34		
PCIAD28	R31		
PCIAD29	R32		
PCIAD30	R33		
PCIAD31	R34		
PCIC0/$\overline{\text{BE0}}$	G32	PCI	56
PCIC1/$\overline{\text{BE1}}$	J31		
PCIC2/$\overline{\text{BE2}}$	L34		
PCIC3/$\overline{\text{BE3}}$	N34		
PCIClk	AA32	PCI	56
$\overline{\text{PCIDevSel}}$	K32	PCI	56
$\overline{\text{PCIFrame}}$	L32	PCI	56

Table 5. Signals Listed Alphabetically (Sheet 19 of 26)

Signal Name	Ball	Interface Group	Page
PCIGnt0/Req	Y34	PCI	56
PCIGnt1	Y33		
PCIGnt2	Y32		
PCIGnt3	Y31		
PCIGnt4	AA33		
PCIGnt5	AA34		
PCIIDSel	T31	PCI	56
PCIINT	AB34	PCI	56
PCIIRDY	K33	PCI	56
PCIPar	J32	PCI	56
PCIPErr	J33	PCI	56
PCIReq0/Gnt	V34	PCI	56
PCIReq1	U31		
PCIReq2	V33		
PCIReq3	V31		
PCIReq4	W32		
PCIReq5	W31		
PCIReset	AA31	PCI	56
PCISErr	J34	PCI	56
PCIStop	K31	PCI	56
PCITRDY	K34	PCI	56

Table 5. Signals Listed Alphabetically (Sheet 20 of 26)

Signal Name	Ball	Interface Group	Page
[PerAddr02]GPIO05[EOT3/TC3]	C26	External Slave Peripheral	59
[PerAddr03]GPIO04[DMAAck3]	D26		
[PerAddr04]GPIO03[DMAReq3]	A26		
[PerAddr05]GPIO02[EOT2/TC2]	D25		
[PerAddr06]GPIO01[DMAAck2]	C25		
[PerAddr07]GPIO00[DMAReq2]	B25		
PerAddr08	A25		
PerAddr09	C24		
PerAddr10	D24		
PerAddr11	B24		
PerAddr12	D23		
PerAddr13	A24		
PerAddr14	C23		
PerAddr15	A23		
PerAddr16	D22		
PerAddr17	C22		
PerAddr18	A22		
PerAddr19	D21		
PerAddr20	C21		
PerAddr21	B21		
PerAddr22	A21		
PerAddr23	D20		
PerAddr24	C20		
PerAddr25	B20		
PerAddr26	D19		
PerAddr27	C19		
PerAddr28	A19		
PerAddr29	D18		
PerAddr30	C18		
PerAddr31	B18		
$\overline{\text{PerBLast}}$	B07	External Slave Peripheral	59
PerClk	A07	External Master Peripheral	60
$\overline{\text{PerCS0}}$[$\overline{\text{NFCE0}}$]	D10	External Slave Peripheral	59
[$\overline{\text{PerCS1}}$][$\overline{\text{NFCE1}}$]GPIO06	B09		
[$\overline{\text{PerCS2}}$][$\overline{\text{NFCE2}}$]GPIO07	D09		
[$\overline{\text{PerCS3}}$][$\overline{\text{NFCE3}}$]GPIO08	D08		
[$\overline{\text{PerCS4}}$]GPIO09	A09		
[$\overline{\text{PerCS5}}$]GPIO10	A08		

Table 5. Signals Listed Alphabetically (Sheet 21 of 26)

Signal Name	Ball	Interface Group	Page
PerData00	C14	External Slave Peripheral	59
PerData01	D14		
PerData02	A13		
PerData03	B13		
PerData04	C13		
PerData05	D13		
PerData06	A12		
PerData07	C12		
PerData08	A11		
PerData09	D12		
PerData10	B11		
PerData11	C11		
PerData12	D11		
PerData13	A10		
PerData14	B10		
PerData15	C10		
PerData16	E03		
PerData17	C01		
PerData18	D02		
PerData19	E04		
PerData20	D01		
PerData21	E01		
PerData22	F04		
PerData23	F03		
PerData24	F02		
PerData25	F01		
PerData26	G03		
PerData27	G04		
PerData28	G02		
PerData29	G01		
PerData30	H04		
PerData31	H03		
[PerDataPar0]GPIO36[$\overline{\text{UART0_CTS}}$/UART3_Rx]	A29		
[PerDataPar1]GPIO37[$\overline{\text{UART0_RTS}}$//UART3_Tx]	B29		
[PerDataPar2]GPIO32	R03		
[PerDataPar3]GPIO33	R04		
[PerErr]GPIO11	C07	External Master Peripheral	59
$\overline{\text{PerOE}}$	B14	External Slave Peripheral	59
PerReady	C17	External Slave Peripheral	59

Table 5. Signals Listed Alphabetically (Sheet 22 of 26)

Signal Name	Ball	Interface Group	Page
PerR/$\overline{W}$	A14	External Slave Peripheral	59
$\overline{PerWBE0}$	A15	External Slave Peripheral	59
$\overline{PerWBE1}$	B15		
$\overline{PerWBE2}$	C15		
$\overline{PerWBE3}$	D15		
PSROOut	A20	System	62
$\overline{RAS}$	AJ04	DDR SDRAM	57
[RcvrInh]HoldReq	D07	System	62
RefEn	B06	System	62
[RejectPkt0]GPIO20	AM23	Ethernet	58
[RejectPkt1]GPIO21	AL23		
Reserved	A05	Reserved	63
Reserved	J01		
Reserved	J02		
Reserved	L03		
Reserved	N02		
Reserved	N03		
SCPClkOut[IIC1SClk]	AC34	Serial Peripheral (SPI)	61
SCPDI[IIC1SData]	AC32		
[SCPDO]GPIO23	AB31		
SOV_{DD}	V05	Power	63
SOV_{DD}	AA13		
SOV_{DD}	AB14		
SOV_{DD}	AC02		
SOV_{DD}	AF05		
SOV_{DD}	AH05		
SOV_{DD}	AJ05		
SOV_{DD}	AK02		
SOV_{DD}	AK06		
SOV_{DD}	AK07		
SOV_{DD}	AK09		
SOV_{DD}	AK18		
SOV_{DD}	AN05		
SOV_{DD}	AN12		

Table 5. Signals Listed Alphabetically (Sheet 23 of 26)

Signal Name	Ball	Interface Group	Page
SV_{REF1A}	Y04	DDR SDRAM	57
SV_{REF1B}	AL10		
SV_{REF2A}	AF04		
SV_{REF2B}	AL19		
SysClk	AP23	System	62
SysErr	AD32	System	62
$\overline{\text{SysReset}}$	AD31	System	62
TCK	P02	JTAG	61
TDI	K03	JTAG	61
TDO	B22	JTAG	61
TestEn	C09	System	62
TherMonA	C16	System	62
TherMonB	D16		
TmrClk	P03	System	62
TMS	K02	JTAG	61
[TrcBS0]GPIO49	AE34	Trace	63
[TrcBS1]GPIO50	AE32		
[TrcBS2]GPIO51	AE33		
TrcClk	AG32	Trace	63
[TrcES0]GPIO52	AE31	Trace	63
[TrcES1]GPIO53	AF34		
[TrcES2]GPIO54	AF33		
[TrcES3]GPIO55	AF32		
[TrcES4]GPIO56	AF31		
[TrcTS0]GPIO57	AG34	Trace	63
[TrcTS1]GPIO58	AG31		
[TrcTS2]GPIO59	AH33		
[TrcTS3]GPIO60	AH34		
[TrcTS4]GPIO61	AH32		
[TrcTS5]GPIO62	AJ34		
[TrcTS6]GPIO63	AH31		
$\overline{\text{TRST}}$	A06	JTAG	61

Table 5. Signals Listed Alphabetically (Sheet 24 of 26)

Signal Name	Ball	Interface Group	Page
[UART0_CTS/UART3_Rx]GPIO36[PerDataPar0]	A29	UART Peripheral	60
[UART0_DCD/UART1_CTS/UART2_Tx]GPIO34	C28		
[UART0_DSR/UART1_RTS/UART2_Rx]GPIO35	C29		
[UART0_DTR/UART1_Tx]GPIO38	D28		
[UART0_RI/UART1_Rx]GPIO39	B28		
[UART0_RTS/UART3_Tx]GPIO37[PerDataPar1]	B29		
UART0_Rx	C27		
UARTSerClk	A27		
UART0_Tx	D27		

Table 5. Signals Listed Alphabetically (Sheet 25 of 26)

Signal Name	Ball	Interface Group	Page
V_{DD}	E11	Power	63
V_{DD}	E12		
V_{DD}	E13		
V_{DD}	E14		
V_{DD}	E15		
V_{DD}	E20		
V_{DD}	E21		
V_{DD}	E22		
V_{DD}	E23		
V_{DD}	E24		
V_{DD}	L05		
V_{DD}	L30		
V_{DD}	M05		
V_{DD}	M30		
V_{DD}	N05		
V_{DD}	N16		
V_{DD}	N19		
V_{DD}	N30		
V_{DD}	P05		
V_{DD}	P16		
V_{DD}	P19		
V_{DD}	P30		
V_{DD}	R05		
V_{DD}	R30		
V_{DD}	T13		
V_{DD}	T14		
V_{DD}	T21		
V_{DD}	T22		
V_{DD}	W13		
V_{DD}	W14		
V_{DD}	W21		
V_{DD}	W22		
V_{DD}	Y05		
V_{DD}	Y30		

Table 5. Signals Listed Alphabetically (Sheet 26 of 26)

Signal Name	Ball	Interface Group	Page
V_{DD}	AA05	Power	63
V_{DD}	AA16		
V_{DD}	AA19		
V_{DD}	AA30		
V_{DD}	AB05		
V_{DD}	AB16		
V_{DD}	AB19		
V_{DD}	AB30		
V_{DD}	AC05		
V_{DD}	AC30		
V_{DD}	AD05		
V_{DD}	AD30		
V_{DD}	AK11		
V_{DD}	AK12		
V_{DD}	AK13		
V_{DD}	AK14		
V_{DD}	AK15		
V_{DD}	AK20		
V_{DD}	AK21		
V_{DD}	AK22		
V_{DD}	AK23		
V_{DD}	AK24		
$\overline{WE}$	AJ02	DDR SDRAM	57

Signals in Ball Assignment Order

In the following table, only the primary (default) signal name is shown for each ball. Multiplexed or multifunction signals are marked with an asterisk (*). To determine what other signals or functions are on those balls, look up the primary signal name in *Table 5* on page 19.

Table 6. Signals Listed by Ball Assignment (Sheet 1 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	GND	C01	PerData17	D01	PerData20
A02	GND	B02	GND	C02	GND	D02	PerData18
A03	GND	B03	GND	C03	GND	D03	GND
A04	GPIO27*	B04	GND	C04	GND	D04	GND
A05	Reserved	B05	OV_{DD}	C05	GPIO29*	D05	GND
A06	$\overline{TRST}$	B06	RefEn	C06	GPIO28*	D06	$\overline{ExtReset}$
A07	PerClk	B07	$\overline{PerBLast}$	C07	GPIO11*	D07	HoldReq*
A08	GPIO10*	B08	GND	C08	LeakTest2	D08	GPIO08*
A09	GPIO09*	B09	GPIO06*	C09	TestEn	D09	GPIO07*
A10	PerData13	B10	PerData14	C10	PerData15	D10	$\overline{PerCS0}$*
A11	PerData08	B11	PerData10	C11	PerData11	D11	PerData12
A12	PerData06	B12	OV_{DD}	C12	PerData07	D12	PerData09
A13	PerData02	B13	PerData03	C13	PerData04	D13	PerData05
A14	PerR/$\overline{W}$	B14	$\overline{PerOE}$	C14	PerData00	D14	PerData01
A15	$\overline{PerWBE0}$	B15	$\overline{PerWBE1}$	C15	$\overline{PerWBE2}$	D15	$\overline{PerWBE3}$
A16	GPIO13*	B16	GND	C16	TherMonA	D16	TherMonB
A17	GPIO22*	B17	GPIO15*	C17	PerReady	D17	GPIO12*
A18	GPIO14*	B18	PerAddr31	C18	PerAddr30	D18	PerAddr29
A19	PerAddr28	B19	GND	C19	PerAddr27	D19	PerAddr26
A20	PSROOut	B20	PerAddr25	C20	PerAddr24	D20	PerAddr23
A21	PerAddr22	B21	PerAddr21	C21	PerAddr20	D21	PerAddr19
A22	PerAddr18	B22	TDO	C22	PerAddr17	D22	PerAddr16
A23	PerAddr15	B23	OV_{DD}	C23	PerAddr14	D23	PerAddr12
A24	PerAddr13	B24	PerAddr11	C24	PerAddr09	D24	PerAddr10
A25	PerAddr08	B25	GPIO00*	C25	GPIO01*	D25	GPIO02*
A26	GPIO03*	B26	GND	C26	GPIO05*	D26	GPIO04*
A27	UARTSerClk	B27	GND	C27	UART0_Rx*	D27	UART0_Tx*
A28	GND	B28	GPIO39*	C28	GPIO34*	D28	GPIO38*
A29	GPIO36*	B29	GPIO37*	C29	GPIO35*	D29	PCIAD00
A30	PCIAD01	B30	OV_{DD}	C30	PCIAD02	D30	GND
A31	PCIAD03	B31	GND	C31	GND	D31	GND
A32	GND	B32	GND	C32	GND	D32	GND
A33	GND	B33	GND	C33	GND	D33	GND
A34	GND	B34	GND	C34	GND	D34	PCIAD04

Table 6. Signals Listed by Ball Assignment (Sheet 2 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	PerData21	F01	PerData25	G01	PerData29	H01	GND
E02	OV_{DD}	F02	PerData24	G02	PerData28	H02	GND
E03	PerData16	F03	PerData23	G03	PerData26	H03	PerData31
E04	PerData19	F04	PerData22	G04	PerData27	H04	PerData30
E05	GND	F05	OV_{DD}	G05	OV_{DD}	H05	GND
E06	OV_{DD}	F06	No Ball	G06	No Ball	H06	No Ball
E07	OV_{DD}	F07	No Ball	G07	No Ball	H07	No Ball
E08	GND	F08	No Ball	G08	No Ball	H08	No Ball
E09	OV_{DD}	F09	No Ball	G09	No Ball	H09	No Ball
E10	GND	F10	No Ball	G10	No Ball	H10	No Ball
E11	V_{DD}	F11	No Ball	G11	No Ball	H11	No Ball
E12	V_{DD}	F12	No Ball	G12	No Ball	H12	No Ball
E13	V_{DD}	F13	No Ball	G13	No Ball	H13	No Ball
E14	V_{DD}	F14	No Ball	G14	No Ball	H14	No Ball
E15	V_{DD}	F15	No Ball	G15	No Ball	H15	No Ball
E16	GND	F16	No Ball	G16	No Ball	H16	No Ball
E17	OV_{DD}	F17	No Ball	G17	No Ball	H17	No Ball
E18	GND	F18	No Ball	G18	No Ball	H18	No Ball
E19	GND	F19	No Ball	G19	No Ball	H19	No Ball
E20	V_{DD}	F20	No Ball	G20	No Ball	H20	No Ball
E21	V_{DD}	F21	No Ball	G21	No Ball	H21	No Ball
E22	V_{DD}	F22	No Ball	G22	No Ball	H22	No Ball
E23	V_{DD}	F23	No Ball	G23	No Ball	H23	No Ball
E24	V_{DD}	F24	No Ball	G24	No Ball	H24	No Ball
E25	GND	F25	No Ball	G25	No Ball	H25	No Ball
E26	OV_{DD}	F26	No Ball	G26	No Ball	H26	No Ball
E27	GND	F27	No Ball	G27	No Ball	H27	No Ball
E28	OV_{DD}	F28	No Ball	G28	No Ball	H28	No Ball
E29	OV_{DD}	F29	No Ball	G29	No Ball	H29	No Ball
E30	GND	F30	OV_{DD}	G30	OV_{DD}	H30	GND
E31	GND	F31	PCIAD05	G31	PCIAD10	H31	PCIAD13
E32	$\overline{\text{Halt}}$*	F32	PCIAD07	G32	PCIC0/$\overline{\text{BE0}}$	H32	PCIAD14
E33	OV_{DD}	F33	PCIAD08	G33	PCIAD11	H33	GND
E34	PCIAD06	F34	PCIAD09	G34	PCIAD12	H34	PCIAD15

Table 6. Signals Listed by Ball Assignment (Sheet 3 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	Reserved	K01	GND	L01	OV_{DD}	M01	GND
J02	Reserved	K02	TMS	L02	OV_{DD}	M02	OV_{DD}
J03	GND	K03	TDI	L03	Reserved	M03	GPIO30*
J04	OV_{DD}	K04	GND	L04	OV_{DD}	M04	GND
J05	OV_{DD}	K05	GND	L05	V_{DD}	M05	V_{DD}
J06	No Ball	K06	No Ball	L06	No Ball	M06	No Ball
J07	No Ball	K07	No Ball	L07	No Ball	M07	No Ball
J08	No Ball	K08	No Ball	L08	No Ball	M08	No Ball
J09	No Ball	K09	No Ball	L09	No Ball	M09	No Ball
J10	No Ball	K10	No Ball	L10	No Ball	M10	No Ball
J11	No Ball	K11	No Ball	L11	No Ball	M11	No Ball
J12	No Ball	K12	No Ball	L12	No Ball	M12	No Ball
J13	No Ball	K13	No Ball	L13	No Ball	M13	No Ball
J14	No Ball	K14	No Ball	L14	No Ball	M14	No Ball
J15	No Ball	K15	No Ball	L15	No Ball	M15	No Ball
J16	No Ball	K16	No Ball	L16	No Ball	M16	No Ball
J17	No Ball	K17	No Ball	L17	No Ball	M17	No Ball
J18	No Ball	K18	No Ball	L18	No Ball	M18	No Ball
J19	No Ball	K19	No Ball	L19	No Ball	M19	No Ball
J20	No Ball	K20	No Ball	L20	No Ball	M20	No Ball
J21	No Ball	K21	No Ball	L21	No Ball	M21	No Ball
J22	No Ball	K22	No Ball	L22	No Ball	M22	No Ball
J23	No Ball	K23	No Ball	L23	No Ball	M23	No Ball
J24	No Ball	K24	No Ball	L24	No Ball	M24	No Ball
J25	No Ball	K25	No Ball	L25	No Ball	M25	No Ball
J26	No Ball	K26	No Ball	L26	No Ball	M26	No Ball
J27	No Ball	K27	No Ball	L27	No Ball	M27	No Ball
J28	No Ball	K28	No Ball	L28	No Ball	M28	No Ball
J29	No Ball	K29	No Ball	L29	No Ball	M29	No Ball
J30	OV_{DD}	K30	GND	L30	V_{DD}	M30	V_{DD}
J31	PCIC1/$\overline{BE1}$	K31	$\overline{PCIStop}$	L31	PCIAD16	M31	PCIAD19
J32	PCIPar	K32	$\overline{PCIDevSel}$	L32	$\overline{PCIFrame}$	M32	PCIAD18
J33	$\overline{PCIPErr}$	K33	$\overline{PCIIRDY}$	L33	PCIAD17	M33	OV_{DD}
J34	$\overline{PCISErr}$	K34	$\overline{PCITRDY}$	L34	PCIC2/$\overline{BE2}$	M34	PCIAD20

Table 6. Signals Listed by Ball Assignment (Sheet 4 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	GND	P01	HoldPri*	R01	MemData59	T01	MemData62
N02	Reserved	P02	TCK	R02	DrvrInh1	T02	GND
N03	Reserved	P03	TmrClk	R03	GPIO32*	T03	MemData63
N04	GND	P04	GPIO31*	R04	GPIO33*	T04	MemData58
N05	V_{DD}	P05	V_{DD}	R05	V_{DD}	T05	GND
N06	No Ball	P06	No Ball	R06	No Ball	T06	No Ball
N07	No Ball	P07	No Ball	R07	No Ball	T07	No Ball
N08	No Ball	P08	No Ball	R08	No Ball	T08	No Ball
N09	No Ball	P09	No Ball	R09	No Ball	T09	No Ball
N10	No Ball	P10	No Ball	R10	No Ball	T10	No Ball
N11	No Ball	P11	No Ball	R11	No Ball	T11	No Ball
N12	No Ball	P12	No Ball	R12	No Ball	T12	No Ball
N13	GND	P13	OV_{DD}	R13	GND	T13	V_{DD}
N14	OV_{DD}	P14	GND	R14	GND	T14	V_{DD}
N15	GND	P15	GND	R15	GND	T15	GND
N16	V_{DD}	P16	V_{DD}	R16	GND	T16	GND
N17	GND	P17	GND	R17	GND	T17	GND
N18	GND	P18	GND	R18	GND	T18	GND
N19	V_{DD}	P19	V_{DD}	R19	GND	T19	GND
N20	GND	P20	GND	R20	GND	T20	GND
N21	OV_{DD}	P21	GND	R21	GND	T21	V_{DD}
N22	GND	P22	OV_{DD}	R22	GND	T22	V_{DD}
N23	No Ball	P23	No Ball	R23	No Ball	T23	No Ball
N24	No Ball	P24	No Ball	R24	No Ball	T24	No Ball
N25	No Ball	P25	No Ball	R25	No Ball	T25	No Ball
N26	No Ball	P26	No Ball	R26	No Ball	T26	No Ball
N27	No Ball	P27	No Ball	R27	No Ball	T27	No Ball
N28	No Ball	P28	No Ball	R28	No Ball	T28	No Ball
N29	No Ball	P29	No Ball	R29	No Ball	T29	No Ball
N30	V_{DD}	P30	V_{DD}	R30	V_{DD}	T30	GND
N31	PCIAD21	P31	PCIAD24	R31	PCIAD28	T31	PCIIDSel
N32	PCIAD23	P32	PCIAD26	R32	PCIAD29	T32	GPIO48*
N33	PCIAD22	P33	PCIAD25	R33	PCIAD30	T33	GND
N34	PCIC3/$\overline{BE3}$	P34	PCIAD27	R34	PCIAD31	T34	GPIO47*

Table 6. Signals Listed by Ball Assignment (Sheet 5 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	MemData56	V01	MemData61	W01	MemData55	Y01	DM6
U02	MemData57	V02	MemData60	W02	GND	Y02	MemData49
U03	DM7	V03	MemData51	W03	MemData54	Y03	MemData48
U04	DQS7	V04	MemData50	W04	DQS6	Y04	SV_{REF1A}
U05	GND	V05	SOV_{DD}	W05	GND	Y05	V_{DD}
U06	No Ball	V06	No Ball	W06	No Ball	Y06	No Ball
U07	No Ball	V07	No Ball	W07	No Ball	Y07	No Ball
U08	No Ball	V08	No Ball	W08	No Ball	Y08	No Ball
U09	No Ball	V09	No Ball	W09	No Ball	Y09	No Ball
U10	No Ball	V10	No Ball	W10	No Ball	Y10	No Ball
U11	No Ball	V11	No Ball	W11	No Ball	Y11	No Ball
U12	No Ball	V12	No Ball	W12	No Ball	Y12	No Ball
U13	GND	V13	GND	W13	V_{DD}	Y13	GND
U14	GND	V14	GND	W14	V_{DD}	Y14	GND
U15	GND	V15	GND	W15	GND	Y15	GND
U16	GND	V16	GND	W16	GND	Y16	GND
U17	GND	V17	GND	W17	GND	Y17	GND
U18	GND	V18	GND	W18	GND	Y18	GND
U19	GND	V19	GND	W19	GND	Y19	GND
U20	GND	V20	GND	W20	GND	Y20	GND
U21	GND	V21	GND	W21	V_{DD}	Y21	GND
U22	GND	V22	GND	W22	V_{DD}	Y22	GND
U23	No Ball	V23	No Ball	W23	No Ball	Y23	No Ball
U24	No Ball	V24	No Ball	W24	No Ball	Y24	No Ball
U25	No Ball	V25	No Ball	W25	No Ball	Y25	No Ball
U26	No Ball	V26	No Ball	W26	No Ball	Y26	No Ball
U27	No Ball	V27	No Ball	W27	No Ball	Y27	No Ball
U28	No Ball	V28	No Ball	W28	No Ball	Y28	No Ball
U29	No Ball	V29	No Ball	W29	No Ball	Y29	No Ball
U30	OV_{DD}	V30	GND	W30	GND	Y30	V_{DD}
U31	$\overline{\text{PCIReq1}}$	V31	$\overline{\text{PCIReq3}}$	W31	$\overline{\text{PCIReq5}}$	Y31	$\overline{\text{PCIGnt3}}$
U32	GPIO46*	V32	GPIO44*	W32	$\overline{\text{PCIReq4}}$	Y32	$\overline{\text{PCIGnt2}}$
U33	GPIO45*	V33	$\overline{\text{PCIReq2}}$	W33	GND	Y33	$\overline{\text{PCIGnt1}}$
U34	GPIO43*	V34	$\overline{\text{PCIReq0}}$/$\overline{\text{Gnt}}$	W34	IRQ5*	Y34	$\overline{\text{PCIGnt0}}$/$\overline{\text{Req}}$

Table 6. Signals Listed by Ball Assignment (Sheet 6 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	MemData53	AB01	MemData46	AC01	MemData41	AD01	GND
AA02	MemData52	AB02	MemData47	AC02	SOV_{DD}	AD02	MemData44
AA03	MemData43	AB03	DM5	AC03	MemData40	AD03	MemData35
AA04	MemData42	AB04	DQS5	AC04	MemData45	AD04	MemData34
AA05	V_{DD}	AB05	V_{DD}	AC05	V_{DD}	AD05	V_{DD}
AA06	No Ball	AB06	No Ball	AC06	No Ball	AD06	No Ball
AA07	No Ball	AB07	No Ball	AC07	No Ball	AD07	No Ball
AA08	No Ball	AB08	No Ball	AC08	No Ball	AD08	No Ball
AA09	No Ball	AB09	No Ball	AC09	No Ball	AD09	No Ball
AA10	No Ball	AB10	No Ball	AC10	No Ball	AD10	No Ball
AA11	No Ball	AB11	No Ball	AC11	No Ball	AD11	No Ball
AA12	No Ball	AB12	No Ball	AC12	No Ball	AD12	No Ball
AA13	SOV_{DD}	AB13	GND	AC13	No Ball	AD13	No Ball
AA14	GND	AB14	SOV_{DD}	AC14	No Ball	AD14	No Ball
AA15	GND	AB15	GND	AC15	No Ball	AD15	No Ball
AA16	V_{DD}	AB16	V_{DD}	AC16	No Ball	AD16	No Ball
AA17	GND	AB17	GND	AC17	No Ball	AD17	No Ball
AA18	GND	AB18	GND	AC18	No Ball	AD18	No Ball
AA19	V_{DD}	AB19	V_{DD}	AC19	No Ball	AD19	No Ball
AA20	GND	AB20	GND	AC20	No Ball	AD20	No Ball
AA21	GND	AB21	EOV_{DD}	AC21	No Ball	AD21	No Ball
AA22	EOV_{DD}	AB22	GND	AC22	No Ball	AD22	No Ball
AA23	No Ball	AB23	No Ball	AC23	No Ball	AD23	No Ball
AA24	No Ball	AB24	No Ball	AC24	No Ball	AD24	No Ball
AA25	No Ball	AB25	No Ball	AC25	No Ball	AD25	No Ball
AA26	No Ball	AB26	No Ball	AC26	No Ball	AD26	No Ball
AA27	No Ball	AB27	No Ball	AC27	No Ball	AD27	No Ball
AA28	No Ball	AB28	No Ball	AC28	No Ball	AD28	No Ball
AA29	No Ball	AB29	No Ball	AC29	No Ball	AD29	No Ball
AA30	V_{DD}	AB30	V_{DD}	AC30	V_{DD}	AD30	V_{DD}
AA31	$\overline{\text{PCIReset}}$	AB31	GPIO23*	AC31	GPIO41*	AD31	$\overline{\text{SysReset}}$
AA32	PCIClk	AB32	IIC0SClk	AC32	SCPDI*	AD32	SysErr
AA33	$\overline{\text{PCIGnt4}}$	AB33	GPIO26*	AC33	EOV_{DD}	AD33	GPIO40*
AA34	$\overline{\text{PCIGnt5}}$	AB34	$\overline{\text{PCIINT}}$	AC34	SCPClkOut*	AD34	GPIO42*

Table 6. Signals Listed by Ball Assignment (Sheet 7 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AE01	MemData39	AF01	MemData33	AG01	MemODT1	AH01	$\overline{\text{BankSel1}}$
AE02	MemData38	AF02	MemData37	AG02	GND	AH02	$\overline{\text{BankSel0}}$
AE03	DQS4	AF03	MemData32	AG03	MemData36	AH03	MemODT0
AE04	DM4	AF04	SV_{REF2A}	AG04	MemAddr13	AH04	$\overline{\text{CAS}}$
AE05	GND	AF05	SOV_{DD}	AG05	GND	AH05	SOV_{DD}
AE06	No Ball	AF06	No Ball	AG06	No Ball	AH06	No Ball
AE07	No Ball	AF07	No Ball	AG07	No Ball	AH07	No Ball
AE08	No Ball	AF08	No Ball	AG08	No Ball	AH08	No Ball
AE09	No Ball	AF09	No Ball	AG09	No Ball	AH09	No Ball
AE10	No Ball	AF10	No Ball	AG10	No Ball	AH10	No Ball
AE11	No Ball	AF11	No Ball	AG11	No Ball	AH11	No Ball
AE12	No Ball	AF12	No Ball	AG12	No Ball	AH12	No Ball
AE13	No Ball	AF13	No Ball	AG13	No Ball	AH13	No Ball
AE14	No Ball	AF14	No Ball	AG14	No Ball	AH14	No Ball
AE15	No Ball	AF15	No Ball	AG15	No Ball	AH15	No Ball
AE16	No Ball	AF16	No Ball	AG16	No Ball	AH16	No Ball
AE17	No Ball	AF17	No Ball	AG17	No Ball	AH17	No Ball
AE18	No Ball	AF18	No Ball	AG18	No Ball	AH18	No Ball
AE19	No Ball	AF19	No Ball	AG19	No Ball	AH19	No Ball
AE20	No Ball	AF20	No Ball	AG20	No Ball	AH20	No Ball
AE21	No Ball	AF21	No Ball	AG21	No Ball	AH21	No Ball
AE22	No Ball	AF22	No Ball	AG22	No Ball	AH22	No Ball
AE23	No Ball	AF23	No Ball	AG23	No Ball	AH23	No Ball
AE24	No Ball	AF24	No Ball	AG24	No Ball	AH24	No Ball
AE25	No Ball	AF25	No Ball	AG25	No Ball	AH25	No Ball
AE26	No Ball	AF26	No Ball	AG26	No Ball	AH26	No Ball
AE27	No Ball	AF27	No Ball	AG27	No Ball	AH27	No Ball
AE28	No Ball	AF28	No Ball	AG28	No Ball	AH28	No Ball
AE29	No Ball	AF29	No Ball	AG29	No Ball	AH29	No Ball
AE30	GND	AF30	EOV_{DD}	AG30	GND	AH30	EOV_{DD}
AE31	GPIO52*	AF31	GPIO56*	AG31	GPIO58*	AH31	GPIO63*
AE32	GPIO50*	AF32	GPIO55*	AG32	TrcClk	AH32	GPIO61*
AE33	GPIO51*	AF33	GPIO54*	AG33	GND	AH33	GPIO59*
AE34	GPIO49*	AF34	GPIO53*	AG34	GPIO57*	AH34	GPIO60*

Table 6. Signals Listed by Ball Assignment (Sheet 8 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AJ01	GND	AK01	$\overline{\text{MemClkOut}}$	AL01	MemClkOut	AM01	GND
AJ02	$\overline{\text{WE}}$	AK02	SOV_{DD}	AL02	MemAddr10	AM02	GND
AJ03	BA0	AK03	BA1	AL03	GND	AM03	GND
AJ04	$\overline{\text{RAS}}$	AK04	GND	AL04	GND	AM04	GND
AJ05	SOV_{DD}	AK05	GND	AL05	GND	AM05	MemAddr00
AJ06	No Ball	AK06	SOV_{DD}	AL06	GND	AM06	MemAddr03
AJ07	No Ball	AK07	SOV_{DD}	AL07	MemAddr06	AM07	MemAddr08
AJ08	No Ball	AK08	GND	AL08	MemAddr11	AM08	MemAddr12
AJ09	No Ball	AK09	SOV_{DD}	AL09	ECC3	AM09	ECC2
AJ10	No Ball	AK10	GND	AL10	SV_{REF1B}	AM10	ECC6
AJ11	No Ball	AK11	V_{DD}	AL11	ECC1	AM11	ECC0
AJ12	No Ball	AK12	V_{DD}	AL12	MemData27	AM12	MemData31
AJ13	No Ball	AK13	V_{DD}	AL13	MemData30	AM13	DQS3
AJ14	No Ball	AK14	V_{DD}	AL14	DM3	AM14	MemData28
AJ15	No Ball	AK15	V_{DD}	AL15	MemData18	AM15	MemData23
AJ16	No Ball	AK16	GND	AL16	DQS2	AM16	MemData16
AJ17	No Ball	AK17	GND	AL17	MemData20	AM17	MemData21
AJ18	No Ball	AK18	SOV_{DD}	AL18	MemData09	AM18	DM1
AJ19	No Ball	AK19	GND	AL19	SV_{REF2B}	AM19	DQS1
AJ20	No Ball	AK20	V_{DD}	AL20	MemData03	AM20	MemData02
AJ21	No Ball	AK21	V_{DD}	AL21	DM0	AM21	DQS0
AJ22	No Ball	AK22	V_{DD}	AL22	MemData04	AM22	MemData05
AJ23	No Ball	AK23	V_{DD}	AL23	GPIO21*	AM23	GPIO20*
AJ24	No Ball	AK24	V_{DD}	AL24	GMCTxD0*	AM24	GMCTxEr*
AJ25	No Ball	AK25	GND	AL25	GPIO25*	AM25	GPIO24*
AJ26	No Ball	AK26	EOV_{DD}	AL26	GPIO17*	AM26	GPIO19*
AJ27	No Ball	AK27	GND	AL27	GMCTxClk*	AM27	GMCGTxClk*
AJ28	No Ball	AK28	EOV_{DD}	AL28	GMCRxD0*	AM28	GMCRxD2*
AJ29	No Ball	AK29	EOV_{DD}	AL29	GND	AM29	GMCRxD4*
AJ30	EOV_{DD}	AK30	GND	AL30	GND	AM30	GMCRxD7*
AJ31	GMCRxDV*	AK31	GND	AL31	GND	AM31	GND
AJ32	GMCCD*	AK32	GMCCrs*	AL32	GND	AM32	GND
AJ33	GMCRefClk*	AK33	EOV_{DD}	AL33	GMCRxEr*	AM33	GND
AJ34	GPIO62*	AK34	GMCMDIO	AL34	GMCMDClk	AM34	GND

Table 6. Signals Listed by Ball Assignment (Sheet 9 of 9)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AN01	GND	AP01	GND				
AN02	GND	AP02	GND				
AN03	GND	AP03	GND				
AN04	GND	AP04	MemAddr01				
AN05	SOV_{DD}	AP05	MemAddr02				
AN06	MemAddr05	AP06	MemAddr04				
AN07	MemAddr07	AP07	MemAddr09				
AN08	GND	AP08	BA2				
AN09	ClkEn	AP09	ECC7				
AN10	DM8	AP10	DQS8				
AN11	ECC5	AP11	ECC4				
AN12	SOV_{DD}	AP12	MemData26				
AN13	MemData25	AP13	MemData24				
AN14	MemData29	AP14	MemData19				
AN15	MemData22	AP15	DM2				
AN16	GND	AP16	MemData17				
AN17	MemData10	AP17	MemData11				
AN18	MemData14	AP18	MemData15				
AN19	GND	AP19	MemData13				
AN20	MemData12	AP20	MemData08				
AN21	MemData06	AP21	MemData07				
AN22	MemData00	AP22	MemData01				
AN23	EOV_{DD}	AP23	SysClk				
AN24	GMCTxEn*	AP24	AV_{DD}				
AN25	GMCTxD1*	AP25	AGND				
AN26	GPIO18*	AP26	GPIO16*				
AN27	GND	AP27	EAGND				
AN28	GMCRxClk*	AP28	EAV_{DD}				
AN29	GMCRxD3*	AP29	GMCRxD1*				
AN30	EOV_{DD}	AP30	GMCRxD5*				
AN31	GND	AP31	GMCRxD6*				
AN32	GND	AP32	GND				
AN33	GND	AP33	GND				
AN34	GND	AP34	GND				

Signal Descriptions

The PPC440GRx embedded controller is packaged in a 456-ball enhanced plastic ball grid array (E-PBGA). The following tables describe the package level pinout.

Table 7. Pin Summary

Group	No. of Pins
Signal pins, non-multiplexed	268
Signal pins, multiplexed	93
Total Signal Pins	**361**
AV_{DD}	1
AGND	1
EAV_{DD}	1
EAGND	1
OV_{DD}	30
SOV_{DD}	14
EOV_{DD}	12
V_{DD}	56
GND	197
Total Power Pins	**313**
Reserved	6
Total Pins	**680**

In the *Table 9* on page 56, each I/O signal is listed along with a short description of its function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. Please see *Table 5* on page 19 for the pin (ball) number to which each signal is assigned.

Multiplexed Signals

Some signals are multiplexed on the same pin so that the pin can be used for different functions. In most cases, the signal names shown in this table are not accompanied by signal names that may be multiplexed on the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in *Table 5* on page 19. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Note: Signals multiplexed with GPIO default to GPIO receivers and float after reset. Initialization software must configure the GPIO registers for the desired function as described in the GPIO chapter of the user's manual. Any of these signals requiring a particular state prior to running initialization code must be terminated wit pull ups or pull downs.

Multipurpose Signals

In addition to multiplexing, some pins are also multi-purpose. For example, the EBC peripheral controller address pins (PerAddr) are used as outputs by the PPC440GRx to broadcast an address to external slave devices when the PPC440GRx has control of the external bus. When during normal operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC440GRx. In this example, the pins are also bidirectional, serving both as inputs and outputs.

Multimode Signals

In some cases (for example, Ethernet) the function of a pin may vary with different modes of operation. When a pin has multiple signal names assigned to distinguish different modes of operation, all of the names are shown.

Strapping Pins

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 86). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

Reserved Pins

The pins classified as Reserved are not functional and must be connected as shown in Table 8.

Table 8. Reserved Pin Connections

Pin	Connection
A05	GND
J01	Open
J02	Open
L03	OV_{DD}
N02	GND
N03	GND

Unused I/Os

Termination of unused receivers is generally required; however, there are some exceptions that reduce or eliminate the need for termination.

Signals Multiplexed with GPIO:

By default after reset, signals shared with GPIO pins are configured as GPIO receivers. Termination however, is not needed if the GPIO during initialization are configured as outputs. To configure as drivers, set and clear the appropriate bits in the GPIOx_ODR, GPIOx_TCR and GPIOx_OR registers as described in the GPIO chapter of the user’s manual.

PCI:

When the PCI bridge is unused, configure the PCI controller to park on the bus by pulling the PCIReq0[Gnt] signal low. Parking forces the PLB3 to PCI bridge to actively drive PCIAD31:0 and PCIC3:0[BE3:0]. The remaining PCI control signals must be terminated as follows:

- Disable the internal PCI arbiter and enable PCI sychronous mode (See IIC Boot Strap Chapter in the User’s Manual).

  Note: Synchronous mode is not supported when operating the PCI bus. This mode should only be used for terminating an unused PCI interface).
- Individually connect PCISErr, PCIPErr, PCITRDY, and PCISTOP through 3kΩ resistors to +3.3V.
- Individually connect PCIReq1:5 through 3kΩ resistors to +3.3V.
- Connect PCIReq0[Gnt] through 1kΩ resistor to GND.

DDR:

- In 32 bit mode, termination is not needed on the upper data, strobe and mask signals when the DDR I/O and DDR controller are configured for 32 bit mode, SDR0_DDRCFG[64B32B]=0 and DDR0_14[REDUC=1.
- Termination of unused ECC signals (ECC0:7, DM8, DQS8) is not needed.

Table 9. Signal Functional Description (Sheet 1 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI Interface				
PCIAD00:31	Address/Data bus (bidirectional).	I/O	3.3V PCI	
PCIC0:3/$\overline{\text{BE0:3}}$	PCI Command/Byte Enables.	I/O	3.3V PCI	
PCIClk	Provides timing to the PCI interface for PCI transactions.	I	3.3V PCI	1, 5
$\overline{\text{PCIDevSel}}$	Indicates the driving device has decoded its address as the target of the current access. (PCI 2.2 specification requires 8.2kΩ pull up on host system).	I/O	3.3V PCI	
$\overline{\text{PCIFrame}}$	Driven by the current master to indicate beginning and duration of an access. (PCI 2.2 specification requires 8.2kΩ pull up on host system).	I/O	3.3V PCI	
$\overline{\text{PCIGnt0}}$/$\overline{\text{Req}}$	Indicates that the specified agent is granted access to the bus. When the internal arbiter is enabled, output is $\overline{\text{PCIGnt0}}$. When the internal arbiter is disabled, output is $\overline{\text{Req}}$.	O	3.3V PCI	
$\overline{\text{PCIGnt1:5}}$	Indicates that the specified agent is granted access to the bus. Used only when internal PCI arbiter enabled.	O	3.3V PCI	
PCIIDSel	Used as a chip select during configuration read and write transactions.	I	3.3V PCI	
$\overline{\text{PCIINT}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
$\overline{\text{PCIIRDY}}$	Indicates initiating agent's ability to complete the current data phase of the transaction. (PCI 2.2 specification requires 8.2kΩ pull up on host system).	I/O	3.3V PCI	
PCIPar	Even parity.	I/O	3.3V PCI	
$\overline{\text{PCIPErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle. (PCI 2.2 specification requires 8.2kΩ pull up on host system).	I/O	3.3V PCI	
$\overline{\text{PCIReq0}}$/$\overline{\text{Gnt}}$	Indicates to the PCI arbiter that the specified agent wishes to use the bus. When the internal arbiter is enabled, input is $\overline{\text{PCIReq0}}$. When internal arbiter is disabled, input is $\overline{\text{Gnt}}$.	I	3.3V PCI	1, 4
$\overline{\text{PCIReq1:5}}$	An indication to the PCI arbiter that the specified agent wishes to use the bus. Used only when internal PCI arbiter enabled.	I	3.3V PCI	1, 4
$\overline{\text{PCIReset}}$	Brings PCI device registers and logic to a consistent state.	O	3.3V PCI	
$\overline{\text{PCISErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors. (PCI 2.2 specification requires 8.2kΩ pull up on host system).	I/O	3.3V PCI	
$\overline{\text{PCIStop}}$	Indicates the current target is requesting the master to stop the current transaction. (PCI 2.2 specification requires 8.2kΩ pull up on host system).	I/O	3.3V PCI	
$\overline{\text{PCITRDY}}$	Indicates the target agent's ability to complete the current data phase of the transaction. (PCI 2.2 specification requires 8.2kΩ pull up on host system).	I/O	3.3V PCI	

Table 9. Signal Functional Description (Sheet 2 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
DDR2/1 SDRAM Interface				
BA0:2	Bank Address supporting up to eight internal banks.	O	2.5V (1.8V) SDRAM-DDR	
$\overline{\text{BankSel0:1}}$	Selects up to two external DDR SDRAM banks.	O	2.5V (1.8V) SDRAM-DDR	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5V (1.8V) SDRAM-DDR	
ClkEn	Clock Enable.	O	2.5V (1.8V) SDRAM-DDR	
DM0:7 DM8	Memory write data byte lane masks. DM8 is the byte lane mask for the ECC byte lane.	O	2.5V (1.8V) SDRAM-DDR	
DQS0:7 DQS8	Byte lane data strobe. Byte lane data strobe for ECC.	I/O	2.5V (1.8V) SDRAM-DDR	
ECC0:7	ECC check bits 0:7.	I/O	2.5V (1.8V) SDRAM-DDR	
MemAddr00:13	Memory address bus.	O	2.5V (1.8V) SDRAM-DDR	
MemData00:63	Memory data bus (MemData32:63 available for DDR2 only).	I/O	2.5V (1.8V) SDRAM-DDR	
MemClkOut $\overline{\text{MemClkOut}}$	Subsystem clock.	O	2.5V (1.8V) SDRAM-DDR Diff driver	
MemODT0:1	DDR2 On-die termination enable (not used with DDR1).	O	2.5V (1.8V) SDRAM-DDR	
$\overline{\text{RAS}}$	Row Address Strobe.	O	2.5V (1.8V) SDRAM-DDR	
$\overline{\text{WE}}$	Write Enable.	O	2.5V (1.8V) SDRAM-DDR	
$S_{VREF1A:B}$	DDR SDRAM reference voltage 1 input.	I	Volt ref receiver (1.25V or 0.9V)	
$S_{VREF2A:B}$	DDR SDRAM reference voltage 2 input.	I	Volt ref driver (1.25V or 0.9V)	

Table 9. Signal Functional Description (Sheet 3 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Ethernet Interface				
GMCRxD0:1, GMC0RxD0:1, SMII0:1RxD	GMII/MII: Receive data. RGMII 0: Receive data. SMII 0:1: Receive data.	I	3.3V tolerant 2.5V CMOS	1
GMCRxD2:3, GMC0RxD2:3	GMII/MII: Receive data. RGMII 0: Receive data.	I	3.3V tolerant 2.5V CMOS	1
GMCRxD4:7, GMC1RxD0:3	GMII/MII: Receive data. RGMII 1: Receive data	I	3.3V tolerant 2.5V CMOS	1
GMCTxD0:1, GMC0TxD0:1, SMII0:1TxD	GMII/MII: Transmit data. RGMII 0: Transmit data. SMII 0:1: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMCTxD2:3, GMC0TxD2:3	GMII/MII: Transmit data. RGMII 0: Transmit data.	O	3.3V tolerant 2.5V CMOS	1
GMCTxD4:7, GMC1TxD0:3	GMII/MII: Transmit data. RGMII 1: Transmit data.	O	3.3V tolerant 2.5V CMOS	1
GMCRxEr, GMC1RxCtl	GMII/MII: Receive error. RGMII 1: Receive control.	I	3.3V tolerant 2.5V CMOS	1
GMCRxClk, GMC0RxClk, SMIISync	GMII/MII: Receive clock. RGMII 0: Receive clock. SMII: Synchronizing signal.	I	3.3V tolerant 2.5V CMOS	1, 5
GMCRxDV, GMC0RxCtl	GMII/MII: Receive data valid. RGMII 0: Receive control.	I	3.3V tolerant 2.5V CMOS	1
GMCCrs, GMC1TxClk	GMII/MII: Carrier sense. RGMII 0: Transmit clock.	I/O	3.3V tolerant 2.5V CMOS	1
GMCTxEr, GMC1TxCtl	GMII/MII: Transmit error. RGMII 1: Transmit control.	O	3.3V tolerant 2.5V CMOS	
GMCTxEn, GMC0TxCtl	GMII/MII: Transmit enable. RGMII 0: Transmit control.	O	3.3V tolerant 2.5V CMOS	
GMCTxClk	MII: Transmit clock for MII.	O	3.3V tolerant 2.5V CMOS	1, 5
GMCCD, GMC1RxClk	GMII/MII: Collision detect.	I	3.3V tolerant 2.5V CMOS	1, 5
GMCMDClk	Management data clock	O	3.3V tolerant 2.5V CMOS	
GMCMDIO	Management data I/O	I/O	3.3V tolerant 2.5V CMOS	
GMCGTxClk, GMC0TxClk	GMII: Transmit clock for GMII. RGMII 0: Transmit clock.	O	3.3V tolerant 2.5V CMOS	
GMCRefClk, SMIIRefClk	GMII, RGMII: Reference clock. SMII: Reference clock.	I	3.3V tolerant 2.5V CMOS Rcvr	1, 5
RejectPkt0:1	External request to reject a packet.	I	3.3V tolerant 2.5V CMOS	1, 5

Table 9. Signal Functional Description (Sheet 4 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External Slave Peripheral Interface				
DMAAck0:3	Used by the PPC440GRx to indicate that data transfers have occurred.	O	3.3V LVTTL	1
DMAReq0	Used by slave peripherals to indicate they are prepared to transfer data.	I	3.3V LVTTL	1
DMAReq1	Used by slave peripherals to indicate they are prepared to transfer data.	I	3.3VLVTTL	1, 5
DMAReq2:3	Used by slave peripherals to indicate they are prepared to transfer data.	I	3.3VLVTTL	1
EOT0:3/TC0:3	End Of Transfer/Terminal Count.	I/O	3.3V LVTTL	1
PerAddr02:07	Peripheral address bus used by the PPC440GRx when not in external master mode; otherwise, used by external master.	I/O	3.3V LVTTL	1, 2
PerAddr08:31	Peripheral address bus used by the PPC440GRx when not in external master mode; otherwise, used by external master.	I/O	3.3V LVTTL	
PerData00:31	Peripheral data bus used by the PPC440GRx when not in external master mode; otherwise, used by external master. **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	3.3V LVTTL	
PerDataPar0:3	Peripheral data bus parity used by the PPC440GRx when not in external master mode; otherwise, used by external master.	I/O	3.3V LVTTL	
$\overline{\text{PerBLast}}$	Used by either the peripheral controller, DMA controller, or external master to indicates the last transfer of a memory access.	I/O	3.3V LVTTL	1, 4
$\overline{\text{PerCS0}}$	External peripheral device select.	O	3.3V LVTTL	2
$\overline{\text{PerCS1:5}}$	External peripheral device select.	I/O	3.3V LVTTL	1, 2
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC440GRx is the bus master, it enables the selected device to drive the bus.	O	3.3V LVTTL	1, 2
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	3.3V LVTTL	1
PerR/$\overline{\text{W}}$	Used by the PPC440GRx when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise, it is used by the external master as an input to indicate the direction of transfer.	I/O	3.3V LVTTL	1, 2
$\overline{\text{PerWBE0:3}}$	External peripheral data bus byte enables.	I/O	3.3V LVTTL	1, 2
PerErr	External Error. Used as an input to record external slave peripheral errors.	I	3.3V LVTTL	1

Table 9. Signal Functional Description (Sheet 5 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External Master Peripheral Interface				
BusReq	Bus Request. Used when the PPC440GRx needs to regain control of peripheral interface from an external master.	O	3.3V LVTTL	
$\overline{\text{ExtAck}}$	External Acknowledgement. Used by the PPC440GRx to indicate that a data transfer occurred.	O	3.3V LVTTL	
$\overline{\text{ExtReq}}$	External Request. Used by an external master to indicate it is prepared to transfer data.	I	3.3V LVTTL	1
$\overline{\text{ExtReset}}$	Peripheral Reset. Used by an external master and by synchronous peripheral slaves. **Note:** The state of signals or clocks cannot be guaranteed until the ExtReset signal has been de-asserted.	O	3.3V LVTTL	
HoldAck	Hold Acknowledge. Used by the PPC440GRx to transfer ownership of peripheral bus to an external master.	O	3.3V LVTTL	
HoldReq	Hold Request. Used by an external master to request ownership of the peripheral bus.	I	3.3V LVTTL	
HoldPri	Hold Primary. Used by an external master to indicate the priority of a given external master tenure.	I	3.3V LVTTL w/pull-up	
PerClk	Peripheral Clock. Used by an external master and by synchronous peripheral slaves.	O	3.3V LVTTL	1
UART Peripheral Interface The UART interface can be configured as follows: 1. One 8-pin, where n = 0 2. Two 4-pin, where n = 0 & 1 3. One 4-pin, where n = 0 and two 2-pin, where n = 1 & 2 4. Four 2-pin, where n = 0 & 1 & 2 & 3				
UARTSerClk	The SerClk input provides an alternative to the internally generated serial clock. It is used in cases where the allowable internally generated clock rates are not satisfactory.	I	3.3V LVTTL	1, 4
UARTn_Rx	Receive data.	I	3.3V LVTTL Rcvr	1, 4
UARTn_Tx	Transmit data.	O	3.3V LVTTL	
$\overline{\text{UARTn_DCD}}$	Data Carrier Detect.	I	3.3V LVTTL	1, 6
$\overline{\text{UARTn_DSR}}$	Data Set Ready.	I	3.3V LVTTL	1, 6
$\overline{\text{UARTn_CTS}}$	Clear To Send.	I	3.3V LVTTL	1, 6
$\overline{\text{UARTn_DTR}}$	Data Terminal Ready.	O	3.3V LVTTL	1
$\overline{\text{UARTn_RTS}}$	Request To Send.	O	3.3V LVTTL	1
$\overline{\text{UARTn_RI}}$	Ring Indicator.	I	3.3V LVTTL	1
IIC Peripheral Interface				
IIC0SClk	IIC0 Serial Clock.	I/O	3.3V LVTTL	1, 2
IIC0SData	IIC0 Serial Data.	I/O	3.3V LVTTL	1, 2
IIC1SClk	IIC1 Serial Clock.	I/O	3.3V LVTTL	1
IIC1SData	IIC1 Serial Data.	I/O	3.3V LVTTL	

Table 9. Signal Functional Description (Sheet 6 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
NAND Flash Interface				
NFALE	Address Latch Enable.	O	3.3V LVTTL	1
$\overline{\text{NFCE0:3}}$	Chip Enable (multiplexed with the $\overline{\text{PerCS0:3}}$ signals).	O	3.3V LVTTL	1
NFCLE	Command Latch Enable. Latches operational commands into the NAND Flash.	O	3.3V LVTTL	1
NFRdy$\overline{\text{Busy}}$	Ready/$\overline{\text{Busy}}$. Indicates status of device during program erase or page read. This signal is wire-OR connected from all NAND Flash devices.	I	3.3V LVTTL	1
$\overline{\text{NFREn}}$	Read Enable. Data is latched on the rising edge.	O	3.3V LVTTL	1
$\overline{\text{NFWEn}}$	Write Enable. Data is latched on the rising edge.	O	3.3V LVTTL	1
Serial Peripheral Interface				
SCPClkOut	Clock output.	I/O	3.3V LVTTL	
SCPDI	Data input.	I/O	3.3V LVTTL	
SCPDO	Data output.	O	3.3V LVTTL	
Interrupts Interface				
IRQ0:4	External interrupt requests 0 through 4.	I/O	3.3V LVTTL	1
IRQ5	External interrupt request 5.	I	3.3V LVTTL Rcvr	1, 5
IRQ6:9	External interrupt requests 6 through 9.	I/O	3.3V LVTTL	1
JTAG Interface				
TCK	Test Clock.	I	3.3V LVTTL w/pull-up	1
TDI	Test Data In.	I	3.3V LVTTL w/pull-up	1, 4
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V LVTTL w/pull-up	1
$\overline{\text{TRST}}$	Test Reset.	I	3.3V LVTTL w/pull-up	1, 5

Table 9. Signal Functional Description (Sheet 7 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main system clock input.	I	3.3V tolerant 2.5V CMOS	1
SysErr	Set to 1 when a machine check is generated.	O	3.3V tolerant 2.5V CMOS	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software. Implemented as an open-drain output (two states; 0 or open circuit).	I/O	3.3V tolerant 2.5V CMOS	1, 2
$\overline{\text{Halt}}$	Halt from external debugger.	I	3.3V LVTTL Rcvr w/pull-up	
TmrClk	Processor timer external input clock.	I	3.3V LVTTL	
GPIO00:15 GPIO22:23 GPIO26:48	General purpose I/O. To access these functions, software must set DCR register bits.	I/O	3.3V LVTTL	1
GPIO16:21 GPIO24:25	General purpose I/O. To access these functions, software must set DCR register bits.	I/O	3.3V tolerant 2.5V CMOS	1
GPIO49:63	General purpose I/O. To access these functions, software must set DCR register bits.	I/O	3.3V tolerant 2.5V CMOS	
TestEn	Test Enable. **Note:** Do not connect for normal operation.	I	3.3V LVTTL Rcvr w/pull-down	
RcvrInh	Receiver Inhibit. Active only when TestEn is active. Used for manufacturing test only.	I	3.3V LVTTL	1
ModeCtrl	Mode Control. Active only when TestEn is active. Used for manufacturing test only.	I	3.3V tolerant 2.5V CMOS Rcvr	1
LeakTest LeakTest2	Leakage Test. Active only when TestEn is active. Used for manufacturing test only.	I	3.3V LVTTL w/pull-up	1
RefEn	Reference Enable. Active only when TestEn is active. Used for manufacturing test only.	I	3.3V LVTTL	1
DrvrInh1:2	Driver Inhibit. Active only when TestEn is active. Used for manufacturing test only. Tie up as specified in Note 2 for normal operation.	I	3.3V LVTTL w/pull-up	1
TherMonA:B	On-chip PNP thermal monitor transistor. A is the emitter and B is the base. The collector is grounded.	I	Thermal monitor	5
PSROOut	Module characterization and screening. Use for test purposes only. Tie down as specified in Note 3 for normal operation.	O	Perf screen ring osc	1, 3

Table 9. Signal Functional Description (Sheet 8 of 8)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to OV_{DD} (EOV_{DD} for Ethernet)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Trace Interface				
TrcBS0:2	Trace branch execution status.	I/O	3.3V tolerant 2.5V CMOS	
TrcClk	Trace data capture clock, runs at 1/4 the frequency of the processor.	O	3.3V tolerant 2.5V CMOS	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	I/O	3.3V tolerant 2.5V CMOS	
TrcTS0:6	Additional information on trace execution and branch status.	I/O	3.3V tolerant 2.5V CMOS	
Power				
V_{DD}	+1.5V—Logic voltage.	n/a	n/a	
OV_{DD}	+3.3V—I/O (except DDR2 SDRAM and Ethernet).	n/a	n/a	
EOV_{DD}	+2.5V—I/O Ethernet.	n/a	n/a	
SOV_{DD}	+1.8V (DDR2) or +2.5V (DDR1)—I/O DDR SDRAM.	n/a	n/a	
GND	Ground for logic and I/O voltage.	n/a	n/a	
AV_{DD}	+1.5V—Filtered voltage for system PLLs (analog).	n/a	n/a	
AGND	Ground for system PLL voltage (analog).	n/a	n/a	
EAV_{DD}	+1.5V—Filtered voltage for Ethernet PLLs (analog).	n/a	n/a	
EAGND	Ground for Ethernet PLL voltage (analog).	n/a	n/a	
Reserved				
Reserved	To avoid noise pickup, the balls on this chip classified as Reserved must be connected as shown in *Table 8* on page 55.	na/	n/a	

Device Characteristics

Table 10. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Internal logic supply voltage	V_{DD}	0 to +1.65	V	1
I/O supply voltage	OV_{DD}	0 to +3.6	V	1
Ethernet I/O supply voltage	EOV_{DD}	0 to +2.7	V	1
DDR2 (DDR1) SDRAM I/O supply voltage	SOV_{DD}	0 to +1.94 (+2.7V)	V	1
System analog supply voltage	AV_{DD}	0 to +1.65	V	
Ethernet analog supply voltage	EAV_{DD}	0 to +1.65	V	
Storage Temperature Range	T_{STG}	–55 to +150	°C	
Case temperature under bias	T_C	–40 to +120	°C	2

Notes:

1. If $OV_{DD} \leq 0.4$V, it is required that $V_{DD} \leq 0.4$V. Supply excursions not meeting this criteria must be limited to less than 25ms duration during each power up or power down event.
2. This value is not a specification of the operational temperature range, it is a stress rating only.

Table 11. Recommended DC Operating Conditions (Sheet 1 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+1.425	+1.5	+1.6	V	4
I/O Supply Voltage	OV_{DD}	+3.15	+3.3	+3.45	V	4
Ethernet I/O Supply Voltage	EOV_{DD}	+2.4	+2.5	+2.6	V	4
DDR2 (DDR1) SDRAM I/O Supply Voltage	SOV_{DD}	+1.7 (+2.4)	+1.8 (+2.5)	+1.9 (+2.6)	V	4
System Analog Supply Voltages	AV_{DD}	+1.425	+1.5	+1.6	V	3, 4
Ethernet Analog Voltage	EAV_{DD}	+1.425	+1.5	+1.6	V	3, 4
DDR2 (DDR1) SDRAM Reference Voltage	SV_{REF}	+0.85 (+1.19)	+0.9 (+1.25)	+0.95 (+1.31)	V	2
Input Logic High 3.3V PCI	V_{IH}	$0.5OV_{DD}$		OV_{DD}+0.5	V	1
Input Logic High 3.3V LVTTL		+2.0		+3.6	V	
Input Logic High 2.5V CMOS, 3.3V tolerant		+1.7		+3.6	V	
Input Logic High 1.8V DDR2 (2.5V DDR1)		SV_{REF} + 0.125 (0.15)		2.2 (3.0)	V	

Table 11. Recommended DC Operating Conditions (Sheet 2 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Input Logic Low 3.3V PCI	V_{IL}	–0.5		$0.35OV_{DD}$	V	1
Input Logic Low 3.3V LVTTL		0		+0.8	V	
Input Logic Low 2.5V CMOS		0		+0.7	V	
Input Logic Low 1.8V DDR2 (2.5V DDR1)		–0.3 (–0.3)		SV_{REF} – 0.125 (0.15)	V	
Output Logic High 3.3V PCI	V_{OH}	$0.9OV_{DD}$		-	V	1
Output Logic High 3.3V LVTTL		+2.4		+3.6	V	
Output Logic High 2.5V CMOS		+2.0		+2.7	V	
Output Logic High 1.8V DDR2 (2.5V DDR1)		+0.95 (+1.7)		+1.95 (+2.7)	V	5
Output Logic Low 3.3V PCI	V_{OL}	-		$0.1OV_{DD}$	V	1
Output Logic Low 3.3V LVTTL		0		+0.4	V	
Output Logic Low 2.5V CMOS		0		+0.4	V	
Output Logic Low 1.8V DDR2 (2.5V DDR1)		0		+0.43 (+0.54)	V	5
Input Leakage Current (no pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for pull-down	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	
Input Leakage Current for pull-up	I_{IL3}	–150 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot 3.3V LVTTL	V_{IMAO}			+3.9	V	
Input Max Allowable Undershoot 3.3V LVTTL	V_{IMAU}	–0.6			V	
Output Max Allowable Overshoot 3.3V LVTTL	V_{OMAO}			+3.9	V	
Output Max Allowable Undershoot 3.3V LVTTL	V_{OMAU3}	–0.6			V	
Case Temperature	T_C	–40		+100	°C	6

Notes:

1. PCI drivers meet PCI specifications.
2. $SV_{REF} = SOV_{DD}/2$. SOV_{DD} = +1.8V for DDR2 memory or +2.5V for DDR1 memory.
3. The analog voltages used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GRx. See “Absolute Maximum Ratings” on page 64.
4. Startup sequencing of the power supply voltages is not required. A power-down cycle must complete (OV_{DD} and V_{DD} are below +0.4V) before a new power-up cycle is started
5. At $I_{OH} = I_{OL}$ = 10ma.
6. Case temperature, T_C, is measured at top center of case surface with device soldered to a circuit board.

Table 12. Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
2.5V/1.8V DDR	C_{IN1}	2.9	pF	
3.3V LVTTL	C_{IN2}	2.1	pF	
PCI	C_{IN3}	2.5	pF	
3.3V tolerant CMOS	C_{IN5}	2.4	pF	

Figure 4. Overshoot Waveform

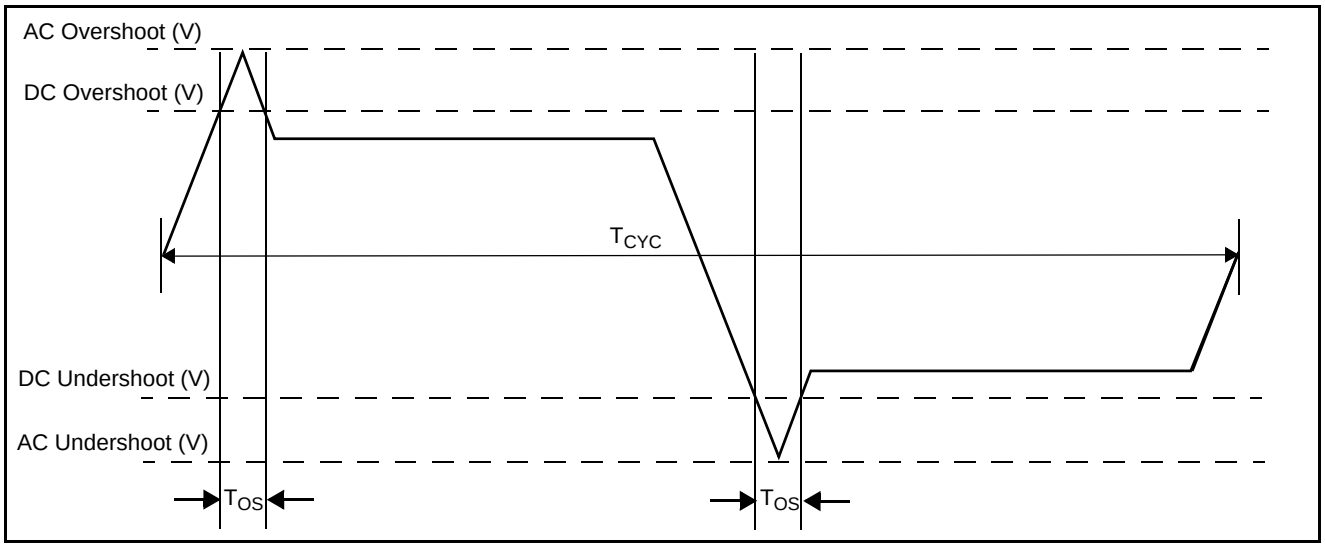


Table 13. Overshoot and Undershoot

Receiver	AC Overshoot (V)	DC Overshoot (V)	DC Undershoot (V)	AC Undershoot (V)	T_{OS}
3.3V LVTTL	3.9	3.6	-0.16	-0.6	$0.1*T_{CYC}$[1]
2.5V (3.3V tolerant)	3.9	3.6	-0.16	-0.6	$0.1*T_{CYC}$[1]
DDR	$1.2*SOV_{DD}$	SOV_{DD} + 0.3	-0.3	-0.6	0.1/MemClkOut
PCI	$1.2*OV_{DD}$	OV_{DD} + 0.5	-0.5	$-0.2*OV_{DD}$	0.1/PCIClk

Notes:

1. T_{CYC} is the period of the bus clock.
   1/PerClk - EBC and NAND flash interfaces.
   1/GMCRXClk - GMII and MII modes
   1/SMIIRefClk - SMII mode
   1/GMCGRXClk - RGMII mode
   1/TrcClk - instruction trace interface
   1/IIC0Clk and 1/IIC1Clk - IIC interfaces
   1/SPIClkOut - SPI

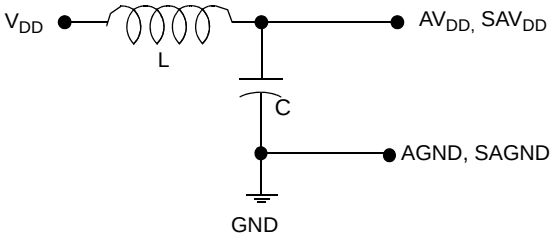
Power Sequencing

Startup sequencing of the power supply voltages is not required. However, a power-down cycle must complete (OV_{DD} and V_{DD} are below +0.4V) before a new power-up cycle is started.

Analog Voltage Filter

The analog voltages (AVdd and EAVdd) used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GRx. A Separate filter, as shown below, is recommended for each voltage.

- The filter should keep the analog voltage to analog ground compression/expansion due to noise less than +/- 50 mV.
- Keep all wire lengths as short as possible.
- Analog grounds must be brought out and connected to the digital ground plane at the filter capacitor.
- The impedance of the ferrite bead should be much greater than that of the capacitor at frequencies where noise is expected.



L – SMT ferrite bead chip, Murata BLM21PG600SN1

C – 0.1µF ceramic

Table 14. Typical DC Power Supply Requirements Using DDR2 Memory

Frequency (MHz)	+1.5V Supply (V_{DD}+AV_{DD}+EAV_{DD})	+1.8V Supply (SOV_{DD})	+2.5V Supply (EOV_{DD})	+3.3V Supply (OV_{DD}+UAV_{DD})	Total	Unit	Notes
400	1.35	0.9	0.2	0.7	3.15	W	1
533	1.45	0.9	0.2	0.7	3.25	W	1
667	1.9	0.9	0.2	0.7	3.7	W	1

Notes:

1. Typical power is estimated and is based on a nominal voltage of V_{DD} = +1.5V, T_C = 85°C, while running Linux and a test application that exercises each functiion with representative traffic.

Table 15. Typical DC Power Supply Requirements Using DDR1 Memory

Frequency (MHz)	+1.5V Supply (V_{DD}+AV_{DD}+EAV_{DD})	+1.8V Supply (SOV_{DD})	+2.5V Supply (SOV_{DD} + EOV_{DD})	+3.3V Supply (OV_{DD}+UAV_{DD})	Total	Unit	Notes
400	1.35	na	1.3	0.7	3.35	W	1
533	1.45	na	1.3	0.7	3.45	W	1
667	1.9	na	1.3	0.7	3.9	W	1

Notes:

1. Typical power is estimated and is based on a nominal voltage of V_{DD} = +1.5V, T_C = 85°C, while running Linux and a test application that exercises each functiion with representative traffic.

Table 16. V_{DD} Supply Power Dissipation

Frequency (MHz)	+1.425V	+1.5V	+1.6V	Unit	Notes
400	1.2	1.35	1.55	W	1
533	1.25	1.45	1.7	W	1
667	1.7	1.9	2.4	W	1

Notes:

1. Power is estimated and is based on V_{DD} specified in the table and T_C = 85°C, while running Linux and a test application that exercises each function with representative traffic.

Table 17. DC Power Supply Loads

Parameter	Symbol	Typical	Maximum	Unit	Notes
V_{DD} (+1.5V) active operating current	I_{DD}	1600	2900	mA	
OV_{DD} (+3.3V) active operating current	I_{ODD}	160	260	mA	
EOV_{DD} (+2.5V) active operating current	I_{EODD}	80	100	mA	
SOV_{DD} (+1.8V) DDR2 active operating current [2]	I_{SODD2}	500	600	mA	
SOV_{DD} (+2.5V) DDR1 active operating current [2]	I_{SODD1}	400	500	mA	
AV_{DD} (+1.5V) input current	I_{ADD}	20	30	mA	1
EAV_{DD} (+1.5V) active operating current	I_{EADD}	20	30	mA	1

Notes:

1. 1. See “Absolute Maximum Ratings” on page 64 for filter recommendations.
2. 2. SOV_{DD} will be either +2.5V or +1.8V, but not both.
3. The maximum current values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results. V_{DD} (logic) current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, PCI, Ethernet, and so on). OV_{DD} (I/O) current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.
4. Typical current is estimated at 667MHz with V_{DD} = +1.5V, OV_{DD} = +3.3V, EOV_{DD} = +2.5V, SOV_{DD} = +2.5V (DDR1) or +1.8V (DDR2), and T_C = +85°C.
5. Maximum current is estimated at 667MHz with V_{DD} = +1.6V, OV_{DD} = +3.45V, EOV_{DD} = +2.6V, SOV_{DD} = +2.6V (DDR1) or +1.9V (DDR2), and TC = +100°C, and best-case process (which drives worst-case power).

Table 18. Package Thermal Specifications

Thermal resistance values for the TE-PBGA package in a convection environment at 6.3W are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)						Unit	Notes
		0 (0)	100 (0.51)	200 (1.02)	300 (1.53	400 (2.04)	500 (2.55)		
Junction-to-ambient thermal resistance without heat sink	θ_{JA}	13.1	11.7	10.9	10.5	10.3	10	°C/W	5
Junction-to-ambient thermal resistance with heat sink	θ_{JA}	11.1	8.2	7.2	6.8	6.6	6.3	°C/W	5, 6
		Resistance Value							
Junction-to-case thermal resistance	θ_{JC}	3.5						°C/W	5
Junction-to-board thermal resistance	θ_{JB}	7.3						°C/W	5

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
2. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
3. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature (+125°C) and P is power consumption.
4. The preceding equations assume that the chip is mounted on a board with at least one signal and two power planes.
5. Values in the table were achieved using a JEDEC standard board with the following characteristics: 114.5mm x 101.6mm x 1.6mm, 4 layers. The board has 100 thermal vias (same as the number of thermal balls on the TE-PBGA package).
6. Values for an attached heat sink were achieved with a 35mm x 35mm x 15mm unit (see Thermal Management below), attached with a 0.1mm thickness of adhesive having a thermal conductivity of 1.3W/mK.

Thermal Management

The following heat sink was used in the above thermal analysis:
ALPHA LPD35-15B (35mm x 35mm x15mm)

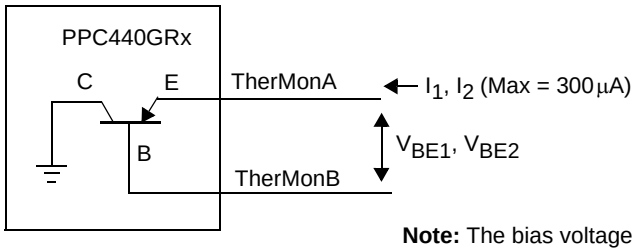
The heat sink is manufactured by:
Alpha Novatech, Inc. (www.alphanovatech.com)
473 Sapena Court, #12
Santa Clara, CA 95054
Phone: 408-567-8082

Thermal Monitor

Thermal monitoring of the chip is accomplished using the PNP transistor ($\beta \approx 2$) provided on the chip. The collector of the transistor is connected to ground (GND). The emitter (TherMonA) and base (TherMonB) are connected to chip pins. A voltage measurement (V_{BE1} and V_{BE2}) across the TherMonA and TherMonB pins at the two current values I_1 and I_2 provides the chip temperature in °K according to the equation:

$$T = (q/nk)(V_{BE2}-V_{BE1})/\ln(I_2/I_1)\ °K \quad \text{where } q = 1.602\ 176\ 53\times10^{-19},\ n = 1.0 \pm 0.015, \text{ and } k = 1.380\ 6505\times10^{-23}.$$

Note: V_{BE2} and V_{BE1} should be specified in Volts. I_1 and I_2 can be any units of measure provided they are the same. The small values require precision measurement and current sources.



Note: The bias voltage V_{EB} should be between +0.5V and +0.7V.

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table *Table 11* on page 64. AC specifications are characterized with V_{DD} = +1.5V, T_C = +85 °C and a 50pF test load as shown in the figure to the right.

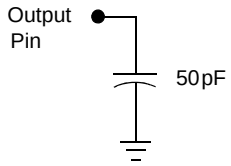


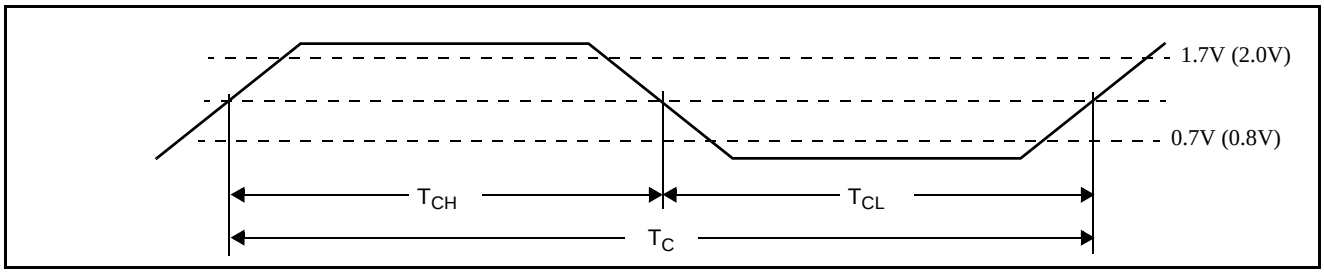
Table 19. Clocking Specifications

Symbol	Parameter	Min	Max	Units	Notes
SysClk Input					
F_C	Frequency	33.33	66.66	MHz	
T_C	Period	15	30	ns	
T_{CS}	Edge stability (cycle-to-cycle jitter)	–	±0.15	ns	
T_{CH}	High time	40% of nominal period	60% of nominal period	ns	
T_{CL}	Low time	40% of nominal period	60% of nominal period	ns	
Note: Input slew rate ≥ 1V/ns					
PLL VCO					
F_C	Frequency	600	1333.33	MHz	
T_C	Period	0.750	1.66	ns	
Processor (CPU) Clock					
F_C	Frequency	333.33	666.66	MHz	1
T_C	Period	1.5	3	ns	
MemClkOut and PLB Clock					
F_C	Frequency	133.33	166.66	MHz	
T_C	Period	6	7.5	ns	
T_{CH}	High time	45% of nominal period	55% of nominal period	ns	
MAL Clock					
F_C	Frequency	45	83.33	MHz	
T_C	Period	12	22.2	ns	

Notes:

1. The maximum supported processor clock frequency for any part is specified in the part number (see “Ordering and PVR Information” on page 5).

Figure 5. Timing Waveform



Note: SysClk and GMCRefClk are 2.5V (3.3V tolerant). Slew rate should be measured between 0.7V and 1.7V.

Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC440GRx. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC440GRx the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC440GRx with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC440GRx peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Important: It is up to the system designer to ensure that any SSCG used with the PPC440GRx meets the above requirements and does not adversely affect other aspects of the system.

I/O Specifications

Table 20. Peripheral Interface Clock Timings

Parameter	Min	Max	Units	Notes
PCIClk frequency (asynchronous mode)	–	66.66	MHz	
PCIClk period (asynchronous mode)	15	–	ns	
PCIClk high time	40% of nominal period	60% of nominal period	ns	
PCIClk low time	40% of nominal period	60% of nominal period	ns	
GMCMDClk frequency	–	2.5	MHz	
GMCMDClk period	400	–	ns	
GMCMDClk high time	160	–	ns	
GMCMDClk low time	160	–	ns	
GMCTxClk frequency MII	2.5	25	MHz	
GMCTxClk period MII	40	400	ns	
GMCTxClk high time	35% of nominal period	–	ns	
GMCTxClk low time	35% of nominal period	–	ns	
GMCRxClk frequency MII	2.5	25	MHz	
GMCRxClk period MII	40	400	ns	
GMCRxClk high time	35% of nominal period	–	ns	
GMCRxClk low time	35% of nominal period	–	ns	
GMCRefClk frequency	–	125	MHz	
GMCRefClk period	8	–	MHz	
GMCRefClk high time	40% of nominal period	60% of nominal period	ns	2
GMCRefClk low time	40% of nominal period	60% of nominal period	ns	2
PerClk (and OPB Clock) frequency (for ext. master or sync. slaves)	33.33MHz	83.33	MHz	
GMCRefClk Edge stability (cycle-to-cycle jitter)	–	$\pm$0.15	ns	
GMCRefClk Slew Rate	2	–	V/ns	
PerClk period	12	30	ns	
PerClk high time	50% of nominal period	66% of nominal period	ns	
PerClk low time	33% of nominal period	50% of nominal period	ns	
UARTSerClk frequency	–	1000 / ($2T_{OPB}$[1]+2ns)	MHz	1
UARTSerClk period	$2T_{OPB}$[1]+2	–	ns	1
UARTSerClk high time	T_{OPB}[1]+1	–	ns	1
UARTSerClk low time	T_{OPB}[1]+1	–	ns	1

Table 20. Peripheral Interface Clock Timings (continued)

Parameter	Min	Max	Units	Notes
TmrClk frequency	–	100	MHz	
TmrClk period	10	–	ns	
TmrClk high time	40% of nominal period	60% of nominal period	ns	
TmrClk low time	40% of nominal period	60% of nominal period	ns	

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 83 MHz.
2. An internal PLL improves this duty cycle to a worst case of 48% minimum, 52% maximum.

Figure 6. Input Setup and Hold Waveform

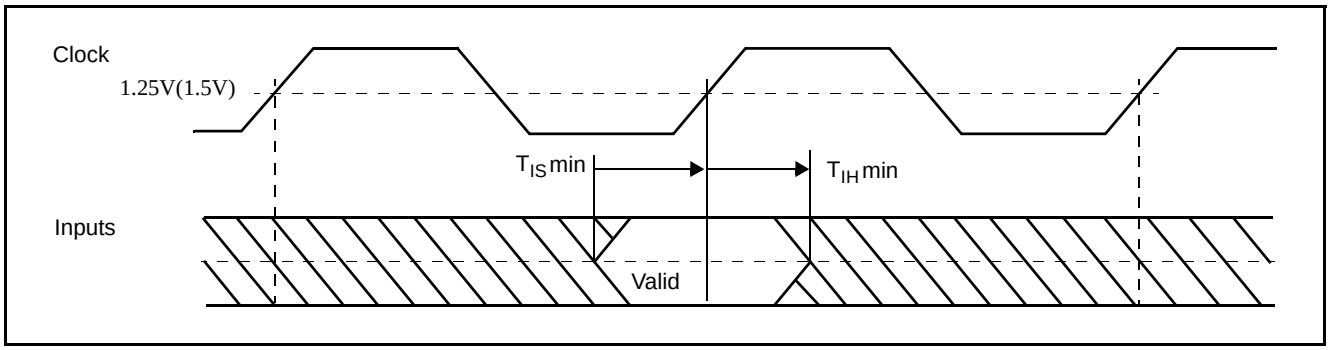


Figure 7. Output Delay and Float Timing Waveform

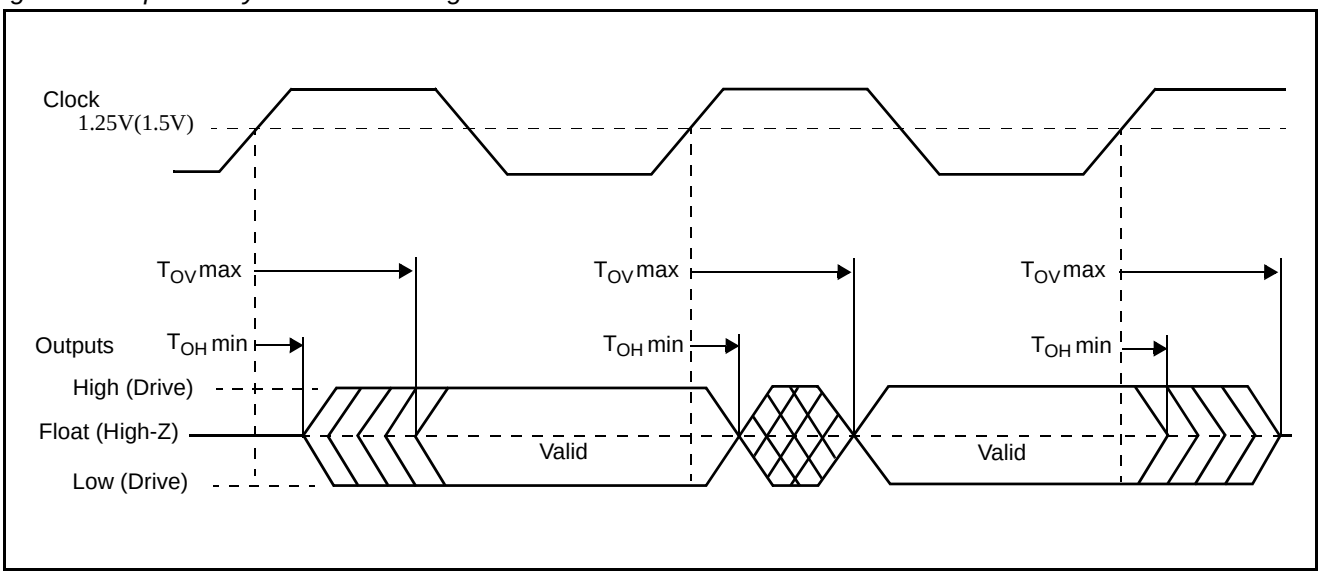
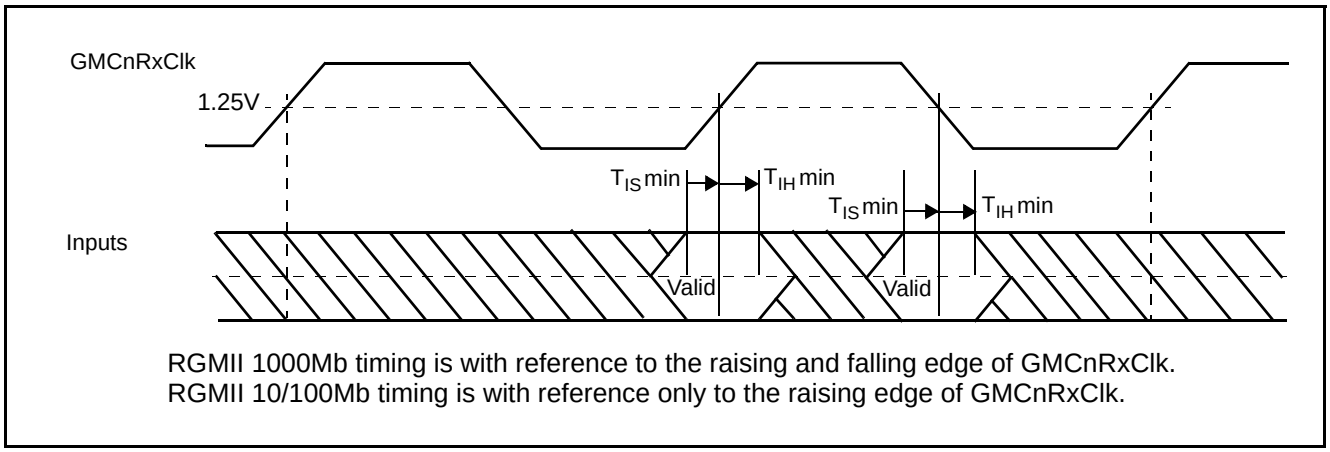
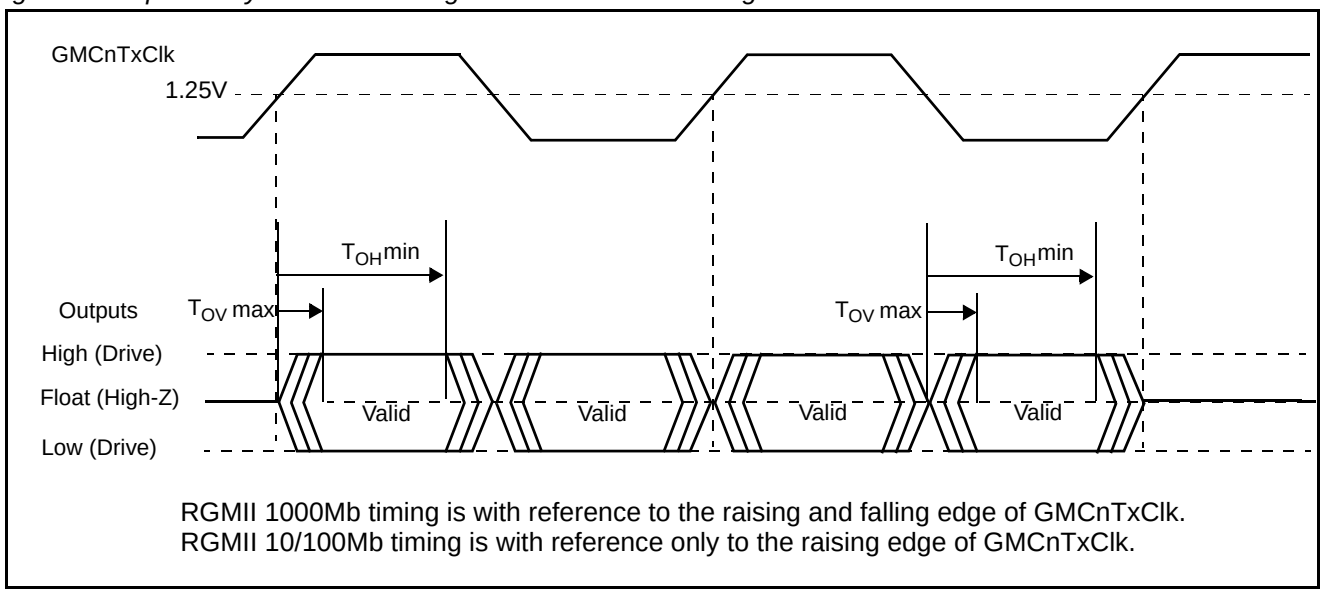


Figure 8. Input Setup and Hold Waveform for RGMII Signals



RGMII 1000Mb timing is with reference to the raising and falling edge of GMCnRxClk.
RGMII 10/100Mb timing is with reference only to the raising edge of GMCnRxClk.

Figure 9. Output Delay and Hold Timing Waveform for RGMII Signals



RGMII 1000Mb timing is with reference to the raising and falling edge of GMCnTxClk.
RGMII 10/100Mb timing is with reference only to the raising edge of GMCnTxClk.

Table 21. I/O Specifications—All Speeds (Sheet 1 of 3)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI Interface								
PCIAD31:00	3	0	6	2	0.5	1.5	PCIClk	
PCIC3:0/BE3:0	3	0	6	2	0.5	1.5	PCIClk	
PCIClk					n/a	n/a		async
PCIDevSel	5	0	6	2	0.5	1.5	PCIClk	
PCIFrame	5	0	6	2	0.5	1.5	PCIClk	
PCIGnt0:5	n/a	n/a	6	2	0.5	1.5	PCIClk	
PCIIDSel	5	0	n/a	n/a	n/a	n/a	PCIClk	
PCIINT	n/a	n/a	n/a	n/a	0.5	1.5		async
PCIIRDY	5	0	6	2	0.5	1.5	PCIClk	
PCIPar	5	0	6	2	0.5	1.5	PCIClk	
PCIPErr	5	0	6	2	0.5	1.5	PCIClk	
PCIReq0:5	5	0	n/a	n/a	n/a	n/a	PCIClk	
PCIReset	n/a	n/a	n/a	n/a	n/a	n/a		async
PCISErr	5	0	6	2	0.5	1.5	PCIClk	
PCIStop	5	0	6	2	0.5	1.5	PCIClk	
PCITRDY	5	0	6	2	0.5	1.5	PCIClk	
Ethernet MII Interface								
GMCCD	n/a	n/a	n/a	n/a	5.1	6.8		async
GMCCrs	n/a	n/a	n/a	n/a	5.1	6.8		async
GMCMDClk					5.1	6.8		
GMCMDIO	10	10	10	1.5	5.1	6.8	GMCMDClk	
GMCRxClk					n/a	n/a		
GMCRxD0:3	10	10	n/a	n/a	5.1	6.8	GMCRxClk	
GMCTxD0:3	n/a	n/a	10	1	5.1	6.8	GMCTxClk	
GMCRxDV	10	10	n/a	n/a	5.1	6.8	GMCRxClk	
GMCRxEr	10	10	n/a	n/a	5.1	6.8	GMCRxClk	
GMCTxClk					n/a	n/a		
GMCTxEr	n/a	n/a	10	1	5.1	6.8	GMCTxClk	
GMCTxEn	n/a	n/a	10	1	5.1	6.8	GMCTxClk	
Ethernet GMII Interface								
GMCCD	n/a	n/a	n/a	n/a	5.1	6.8		async
GMCCrs	n/a	n/a	n/a	n/a	5.1	6.8		async
GMCGTxClk					5.1	6.8		
GMCMDClk					5.1	6.8		
GMCMDIO	10	10	10	1.5	5.1	6.8	GMCMDClk	
GMCRefClk					n/a	n/a		
GMCRxClk					5.1	6.8		
GMCRxD0:7	2	0	n/a	n/a	5.1	6.8	GMCRxClk	
GMCTxD0:7	n/a	n/a	2.5	1	5.1	6.8	GMCGTxClk	
GMCRxDV	2	0	n/a	n/a	5.1	6.8	GMCRxClk	
GMCRXEr	2	0	n/a	n/a	5.1	6.8	GMCRxClk	
GMCTxEr	n/a	n/a	2.5	1	5.1	6.8	GMCGTxClk	
GMCTxEn	n/a	n/a	2.5	1	5.1	6.8	GMCGTxClk	

Table 21. I/O Specifications—All Speeds (Sheet 2 of 3)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
Ethernet RGMII Interface								
GMC0RxClk					n/a	n/a		
GMC0TxClk					5.1	6.8		
GMC0RxD0:3	1	1	n/a	n/a	5.1	6.8	GMC0RxClk	
GMC0RxCtl	1	1	n/a	n/a	5.1	6.8	GMC0RxClk	
GMC0TxD0:3	n/a	n/a	0.5	3.5	5.1	6.8	GMC0TxClk	
GMC0TxCtl	n/a	n/a	0.5	3.5	5.1	6.8	GMC0TxClk	
GMC1RxClk					n/a	n/a		
GMC1TxClk					5.1	6.8		
GMC1RxD0:3	1	1	n/a	n/a	5.1	6.8	GMC1RxClk	
GMC1RxCtl	1	1	n/a	n/a	5.1	6.8	GMC1RxClk	
GMC1TxD0:3	n/a	n/a	0.5	3.5	5.1	6.8	GMC1TxClk	
GMC1TxCtl	n/a	n/a	0.5	3.5	5.1	6.8	GMC1TxClk	
GMCRefClk					n/a	n/a		
Ethernet SMII Interface								
SMIIRefClk					n/a	n/a		
SMIISync	na	na	3	1	5.1	6.8	SMIIRefClk	
SMII0RxD	1.5	1	n/a	n/a	5.1	6.8	SMIIRefClk	
SMII1RxD	1.5	1	n/a	n/a	5.1	6.8	SMIIRefClk	
SMII0TxD	n/a	n/a	3	1	5.1	6.8	SMIIRefClk	
SMII1TxD	n/a	n/a	3	1	5.1	6.8	SMIIRefClk	
Internal Peripheral Interface								
IIC0SClk					27.7	12.8		
IIC0SData	n/a	n/a	5	0	27.7	12.8		
IIC1SClk					27.7	12.8		
IIC1SData	n/a	n/a	5	0	27.7	12.8		
SCPClkOut					27.7	12.8		
SCPDI	5	1.5	n/a	n/a	27.7	12.8		
SCPDO	n/a	n/a	6	0	15.3	10.2		
UARTSerClk					n/a	n/a		
UARTn_Rx	n/a	n/a	n/a	n/a	n/a	n/a		
UARTn_Tx	n/a	n/a	n/a	n/a	19.1	8.7		
$\overline{\text{UARTn_DCD}}$	n/a	n/a	n/a	n/a	n/a	n/a		
$\overline{\text{UARTn_DSR}}$	n/a	n/a	n/a	n/a	n/a	n/a		
$\overline{\text{UARTn_CTS}}$	n/a	n/a	n/a	n/a	n/a	n/a		
$\overline{\text{UARTn_DTR}}$	n/a	n/a	n/a	n/a	19.1	8.7		
$\overline{\text{UARTn_RI}}$	n/a	n/a	n/a	n/a	n/a	n/a		
$\overline{\text{UARTn_RTS}}$	n/a	n/a	n/a	n/a	19.1	8.7		
Interrupts Interface								
IRQ0:9	n/a	n/a	n/a	n/a	n/a	n/a		
JTAG Interface								
TCK	n/a	n/a	n/a	n/a	n/a	n/a		async
TDI	n/a	n/a	n/a	n/a	n/a	n/a		async
TDO	n/a	n/a	n/a	n/a	19.1	8.7		async
TMS	n/a	n/a	n/a	n/a	n/a	n/a		async
$\overline{\text{TRST}}$	n/a	n/a	n/a	n/a	n/a	n/a		async

Table 21. I/O Specifications—All Speeds (Sheet 3 of 3)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
System Interface								
SysClk					n/a	n/a		
TmrClk					n/a	n/a		async
SysReset	n/a	n/a	n/a	n/a	n/a	n/a		async
Halt	n/a	n/a	n/a	n/a	n/a	n/a		async
SysErr	n/a	n/a	n/a	n/a	5.1	6.8		async
TestEn	n/a	n/a	n/a	n/a	n/a	n/a		async
DrvrInh1:2	n/a	n/a	n/a	n/a	n/a	n/a		
RcvrInh	n/a	n/a	n/a	n/a	n/a	n/a		
GPIO00:11	n/a	n/a	n/a	n/a	19.1	8.7		
GPIO12:25	n/a	n/a	n/a	n/a	5.1	6.8		
GPIO26:48	n/a	n/a	n/a	n/a	14.6	6.6		
GPIO49:63	n/a	n/a	n/a	n/a	5.1	6.8		
Trace Interface								
TrcClk				n/a	5.1	6.8		
TrcBS0:2	n/a	n/a	n/a	n/a	5.1	6.8		
TrcES0:4	n/a	n/a	n/a	n/a	5.1	6.8		
TrcTS0:6	n/a	n/a	n/a	n/a	5.1	6.8		

Table 22. I/O Specifications—400MHz to 667MHz

Notes:
1. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
External Slave Peripheral Interface								
DMAAck0:3	n/a	n/a	6	1	19.1	8.7	PerClk	
DMAReq0:3	4	1	n/a	n/a	n/a	n/a	PerClk	
EOT0:3/TC0:3	4	1	6	1	19.1	8.7	PerClk	
PerAddr02:31	4	1	6	1	19.1	8.7	PerClk	
PerBLast	4	1	6	1	19.1	8.7	PerClk	
PerCS0:5	n/a	n/a	6	1	19.1	8.7	PerClk	
PerData00:15	4	1	6	1	19.1	8.7	PerClk	
PerData16:31	4	1	6	1	14.6	6.6	PerClk	
PerOE	n/a	n/a	6	1	19.1	8.7	PerClk	
PerReady	4	1	n/a	n/a	19.1	8.7	PerClk	
PerR/W	4	1	6	1	19.1	8.7	PerClk	
PerWBE0:1	4	1	6	1	19.1	8.7	PerClk	
External Master Peripheral Interface								
BusReq	n/a	n/a	6	1	19.1	8.7	PerClk	
ExtAck	n/a	n/a	6	1	19.1	8.7	PerClk	
ExtReq	4	1	n/a	n/a	19.1	8.7	PerClk	
ExtReset	n/a	n/a	6	1	19.1	8.7	PerClk	
HoldAck	n/a	n/a	6	1	19.1	8.7	PerClk	
HoldReq	4	1	n/a	n/a	n/a	n/a	PerClk	
HoldPri	4	1	n/a	n/a	n/a	n/a		
PerClk					19.1	8.7	PLB Clk	1
PerErr	4	1	n/a	n/a	n/a	n/a	PerClk	
NAND Flash Interface								
NFALE	n/a	n/a	6	1	19.1	8.7	PerClk	
NFCE0:3	n/a	n/a	6	1	19.1	8.7	PerClk	
NFCLE	n/a	n/a	6	1	19.1	8.7	PerClk	
NFRdyBusy	4	1	n/a	n/a	n/a	n/a	PerClk	
NFREn	n/a	n/a	6	1	19.1	8.7	PerClk	
NFWEn	n/a	n/a	6	1	19.1	8.7	PerClk	

DDR2/1 SDRAM I/O Specifications

The DDR2/1 SDRAM controller times its operation with the internal PLB clock signal and generates MemClkOut from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Read capture logic in the DDR controller captures read data using a delayed version of DQS and internally re-synchronizes the data to the PLB clock.The PPC440GRx contains three independently programmable digital delay lines (DLLs) that control the timing of the indicated signals in read and write operations:

1. DQS (with respect to MemClkOut) for write operations.

2. MemData, ECC, and DM (with respect to MemClkOut) for write operations.

3. DQS (with respect to inbound MemData) for read operations.

There is also a master delay line for calibration. Programming details can be found in the *PPC440GRx Embedded Processor Users Manual*.

The signals are terminated as indicated in *Figure 10* for the DDR timing data in the following sections.

The PPC440GRx uses a clock forwarding scheme in which it drives the clock to the memory devices.

Data signals are divided into eight subgroups—one for each byte lane (see *Table 27* on page 85)— plus a ninth subgroup for the ECC byte lane. These signals include MemData00:63, DQS0:8, DM0:8, and ECC0:7 signals. Signals within a data subgroup (byte lane) should be routed together.

Command Bus Operation

The command bus (MemAddr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA, ClkEn, BankSel, MemODT) is driven 180° out-of-phase with MemClkOut, and has no corresponding delay line. Therefore, board designers must consider two different types of systems: 1) registered DIMMs and 2) unbuffered DIMMs. The system clocking design must also be considered. To avoid crosstalk, the command bus signals and the data signals should not be routed together.

Board Layout Restrictions

The paths (traces) for the data and the associated data strobe signal should be routed with the same length between the PPC440GRx and the SDRAM devices, allowing the rising and falling edges of the strobe to arrive at the capture logic at the same time the data is in transition. All of the following timing assumes a trace velocity of 167ps/in.

Board designs must meet the following criteria:

- Skew on the signals in any byte lane should not exceed 50ps (0.3 in).
- Data subgroup trace lengths must be no more than 5in. (800ps) and have a difference of no more than 2.5in. (400ps).
- Byte lane subgroup trace length must be no less than 1.25in. (209ps).

For example, traces that average 3.00in. in length and 167ps/in., and meet the maximum 50ps skew requirement, would have a maximum length difference of 0.3in. So, they would be between 2.85in. and 3.15in. in length.

If the above timing recommendations are followed, the package wire bond lengths can be ignored.

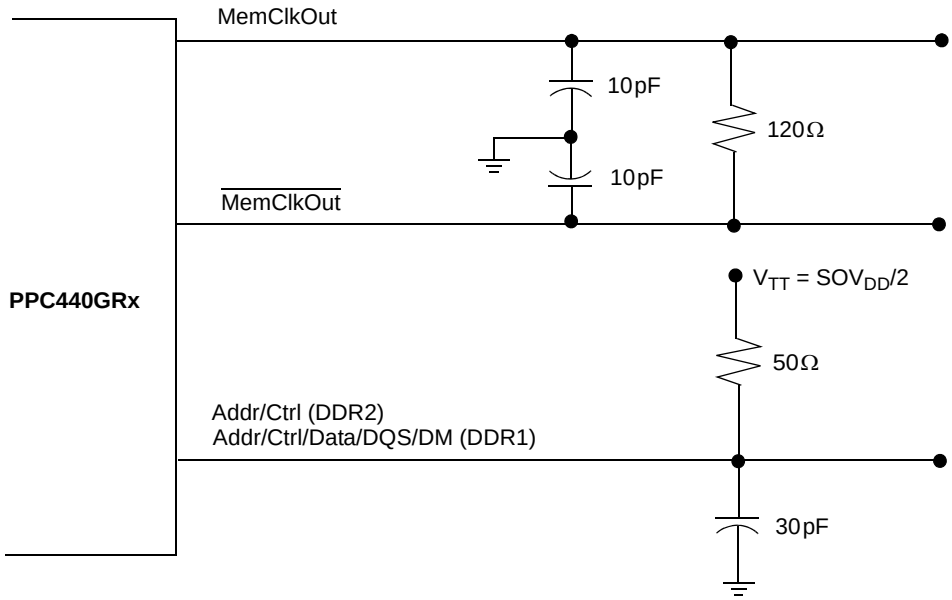
Clocking

Clocking skew to all DRAMs must be minimized. The maximum allowed is considered to be 10ps. Because of the stringent requirements on DDR device clock inputs, it is expected that board designers will use some type of external PLL suitable to redrive the clock to the DDR SDRAMs. In such a system, the PLL acts like a zero-delay insertion buffer.

When using unbufferred DIMMS, the loading on the address bus will be considerably greater than the clock (up to 18 loads for double-sided DIMMs). In this case, it is strongly suggested that a delay of 500ps in the clock path so that the Address/Command setup time at the DIMMs can be met. This delay is sufficient to meet the setup time, without having to change the programmable delay (internal to the PPC440GRx) between the DQS/DQ/DM and the clock (assuming nominal settings as specified in the PPC440GRx Users Manual). While the clock is now 500ps later than the nominal DQS arrival time, this still falls well within the window allowed by the JEDEC spec for T_{DQSS} (± 0.25 cycle, or 1.5ns at 166MHz). In the case where it is not possible to anticipate which kind of DIMMs may be employed in a system, it is always safe to use this 500ps clock delay, since registered DIMMs (the least heavily loaded) will have more than enough margin (almost 1/2 cycle) to accommodate the slight decrease in address hold time.

Termination Model

Figure 10. DDR SDRAM Simulation Signal Termination Model



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design will depend on many factors, including the type of memory used and the board layout.

DDR2 SDRAM On-Die Termination Impedance Setting

For all DDR2 applications, the On-Die Termination (ODT) impedance value *must* be set to 75 ohms in the DIMM Extended Mode Register (EMR) in order to optimize the data transmission during memory write operations.

Table 23. DDR SDRAM Output Driver Specifications (Sheet 1 of 2)

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (maximum)
Write Data		
MemData00:63	10	10
ECC0:7	10	10
DM0:8	10	10
MemClkOut	10	10
MemAddr00:13	10	10
BA0:2	10	10

Table 23. DDR SDRAM Output Driver Specifications (Sheet 2 of 2)

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (maximum)
RAS	10	10
CAS	10	10
WE	10	10
BankSel0:1	10	10
ClkEn	10	10
DQS0:8	10	10
MemODT0:1	10	10

DDR SDRAM Write Operation

The rising edge of MemClkOut aligns with the first rising edge of the DQS signal on writes. The following data is generated by means of simulation and includes logic, driver, package RLC, and lengths. Values are calculated over best case and worst case processes with speed, junction temperature, and voltage as follows:

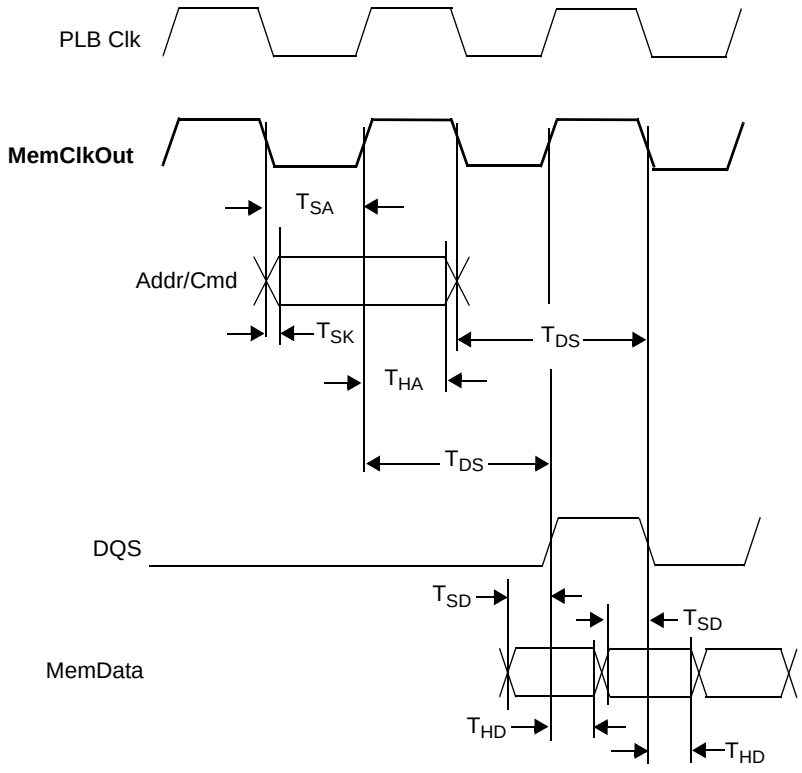
Table 24. DDR SDRAM Write Operation Conditions

Case	Process Speed	Junction Temperature (°C)	Voltage (V)
Best	Fast	–40	+1.6
Worst	Slow	+125	+1.425

Note: In the following tables and timing diagrams, minimum values are measured under best case conditions and maximum values are measured under worst case conditions. The timing numbers in the following sections are obtained using a simulation that assumes a model as shown in *Figure 10, DDR SDRAM Simulation Signal Termination Model*.

The following diagram illustrates the relationship among the signals involved with a DDR write operation.

Figure 11. DDR SDRAM Write Cycle Timing



T_{SK} = Delay from falling edge of MemClkOut to rising/falling edge of signal (skew)
T_{SA} = Setup time for address and command signals to MemClkOut
T_{HA} = Hold time for address and command signals from MemClkOut
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

Note: The timing data in the following tables is based on simulation runs using Einstimer.

Table 25. I/O Timing—DDR SDRAM T_{DS}

Notes:
1. All of the DQS signals are referenced to MemClkOut with the DQS delay line programmed to 1 cycle.
2. Clock speed is 166MHz.

Signal Name	T_{DS} (ns)	
	Minimum	Maximum
DQS0	–0.030	+0.650
DQS1	–0.030	+0.620
DQS2	–0.050	+0.580
DQS3	–0.110	+0.480
DQS4	–0.140	+0.410
DQS5	–0.120	+0.480
DQS6	–0.060	+0.580
DQS7	–0.010	+0.690
DQS8	–0.140	+0.420

Table 26. I/O Timing—DDR SDRAM T_{SK}, T_{SA}, and T_{HA}

Notes:
1. Clock speed is 166MHz. T_{SK} is referenced to MemClkOut falling edge. T_{SA} and T_{HA} are referenced to MemClkOut rising edge.
2. The timing in this table assumes a single registered DIMM load on the outputs. To adjust the timing for unbuffered DIMMs, use the following values by subtracting them from T_{SA} and adding them to T_{SK} and T_{HA}:
   5 loads adjust by 0.41ns
   9 loads adjust by 1.12ns
   18 loads adjust by 2.12ns
3. To obtain adjusted T_{SA} values for lower clock frequencies, use 1/2 of the cycle time for the lower clock frequency and subtract T_{SK} maximum ($0.5T_{CYC} - T_{SK}max$).
4. To obtain adjusted T_{HA} values for lower clock frequencies, use 1/2 of the cycle time for the lower clock frequency and add T_{SK} minimum ($0.5T_{CYC} + T_{SK}min$).

Signal Name	T_{SK} (ns)		T_{SA} (ns)	T_{HA} (ns)
	Minimum	Maximum	Minimum	Minimum
MemAddr00:13	–0.960	–0.270	3.27	2.04
BA0:2				
BankSel0:1				
ClkEn				
$\overline{CAS}$				
$\overline{RAS}$				
$\overline{WE}$				

Table 27. I/O Timing—DDR SDRAM T_{SD} and T_{HD}

Notes:
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 166 MHz.
3. The time values in the table include 1/4 of a cycle at 166 MHz (6 ns x 0.25 = 1.5 ns).
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 1.5 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (for example, $T_{SD} - 1.5 + 0.25T_{CYC}$).

Signal Names	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
MemData00:07, DM0	DQS0	1.37	1.23
MemData08:15, DM1	DQS1	1.41	1.18
MemData16:23, DM2	DQS2	1.40	1.17
MemData24:31, DM3	DQS3	1.41	1.20
MemData32:39, DM4	DQS4	1.45	1.18
MemData40:47, DM5	DQS5	1.40	1.18
MemData48:55, DM6	DQS6	1.46	1.17
MemData56:63, DM7	DQS7	1.45	1.10
ECC0:7, DM8	DQS8	1.46	1.18

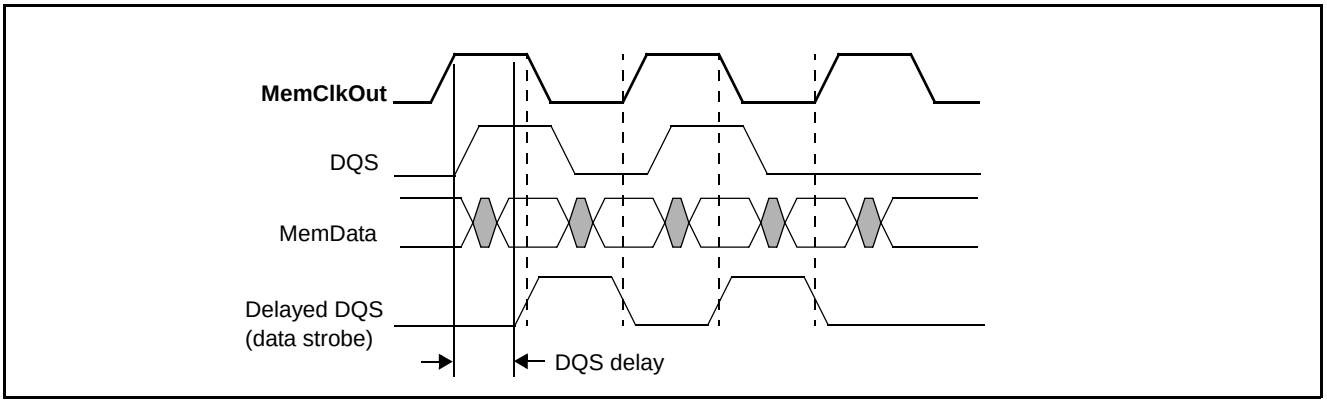
DDR SDRAM Read Operation

The read data capture logic is responsible for capturing the data outputs from the SDRAM devices and passing the data back to the system clock domain. The data strobe signal (DQS) signals used to capture data are delayed to ensure that the rising and falling edges of these strobes are in the middle of the valid window of data.

DDR devices send a DQS coincident with the read data so that the data can be reliably captured by the PPC440GRx. The edges of these strobe signals are aligned with the data output by the SDRAM devices.

In order to reliably latch the data into a synchronizing FIFO, the PPC440GRx produces an internal, delayed version of DQS. The amount of delay is user programmable. In the example shown in *Figure 12, DDR SDRAM DQS Read Timing*, the delay is set to approximately 25% of the system clock. A delay compensation circuit in the PPC440GRx keeps this delay constant.

Figure 12. DDR SDRAM DQS Read Timing



Initialization

The PPC440GRx provides the option for setting initial parameters based on default values or by reading them from a slave PROM attached to the IIC0 bus (see “Serial EEPROM” below). Some of the default values can be altered by strapping on external pins (see “Strapping” below).

Strapping

While the $\overline{\text{SysReset}}$ input pin is low (system reset), the state of certain I/O pins is read to enable certain default initial conditions prior to PPC440GRx start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are used for strap functions only during reset. Following reset they are used for normal functions. The signal names assigned to the pins for normal operation are shown in parentheses following the pin number.

Note: When $\overline{\text{UART0_DCD}}$, $\overline{\text{UART0_DSR}}$ and $\overline{\text{UART0_CTS}}$ are used functionally, the pin straps should be isolated from the UART transceiver during reset as the transceiver may overdrive the pin straps and cause the PPC440GRx to read incorrect straps.

The following table lists the strapping pins along with their functions and strapping options:

Table 28. Strapping Pin Assignments

Function	Option	Pin Strapping		
		C28 (UART0_DCD)	C29 (UART0_DSR)	A29 (UART0_CTS)
Serial device is disabled. Each of the six options (A–F) is a combination of boot source, boot-source width, and clock frequency specifications. Refer to the IIC Bootstrap Controller chapter in the *PPC440GRx Embedded Processor User’s Manual* for details.	A	0	0	0
	B	0	0	1
	C	0	1	0
	D	0	1	1
	E	1	0	0
	F	1	1	0
Serial device is enabled. The option being selected is the IIC0 slave address that will respond with strapping data.	G (0xA8)	1	0	1
	H (0xA4)	1	1	1

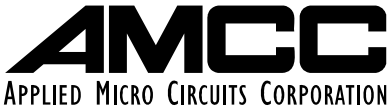
Serial EEPROM

During reset, initial conditions other than those obtained from the strapping pins can be read from a ROM device connected to the IIC0 port. At the de-assertion of reset, if the bootstrap controller is enabled, the PPC440GRx sequentially reads 16B from the ROM device on the IIC0 port and sets the SDR0_SDSTP0, SDR0_SDSTP1, SDR0_SDSTP2 and SDR0_SDSTP3 registers accordingly.

The initialization settings and their default values are covered in detail in the *PowerPC 440GRx User’s Manual*.

Revision Log

Date	Version	Contents of Modification
04/11/2006	1.01	Initial creation of document.
04/24/2006	1.02	Correct security designation. Add new/updated power and current values.
05/30/2006	1.03	Correct list containing balls by ball number. Update power and temperature data. Add clocking information. Update EEPROM.
11/02/2006	1.04	Change and delete incorrect MemClkEn references Correct enable/disable specifications for PCI Gnt/Req signals. Change analog voltage filter circuit inductor Part number. Correct I/O designation for some Ethernet signals. Remove leaded PNs.
12/28/2006	1.05	Correct descriptions of LeakTest, RcvrInh, ModeCtrl, RefEn, and DrvrInh1:2 signals. Add information concerning address bus loading on DDR SDRAMs. Restore leaded PNs.
01/10/2007	1.06	Update DDR2/1 SDRAM timing and board design data.
07/25/2007	1.07	Added more information to the Thermal Monitor section. Changes to Figure 3.
10/15/2007	1.08	Added assembly recommendations, Tables 3 and 4. Added recommendations for Unused I/O. Updated signal description in table 9for signals SPCClkOUT, SCPDI, SCPDO, LeakTest and LeakTest2. Updated Table 21 to include reference clocks. Removed all references to TBI and RTBI as these modes are not supported due to errata: Chip_4 and Chip_5. Added voltage reference to Figures 5, 6 and 7 Corrected I/O comments for UART and Ethernet signals in Table 9. Removed Note 2 from Table 10and added section on Analog Voltage Filter Added Figure 4 and Table 13 for Overshoot and Undershoot. Added section on Power Sequencing. Added slew rate and jitter requirements for GMCRefClk in Table 20. Added note in Strapping section Changed GPIO26[IIC0SData] to [GPIO26]IIC0SData in Table 9. Added figures 8 and 9 showing setup, hold, output valid and output hold timing for RGMII signals. Corrected PVR number Corrected phone numbers on last page Corrected RGMII timing relative to GMCnTXClk in Table 21. Added pull up recommendations to Table 9 for PCI signals.



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