

FEATURES

- CDMA/EVDO and WCDMA/HSPA Compliant
- High Efficiency (R99 waveform):
 - 48% @ $P_{OUT} = +28.5 \text{ dBm}$
- Optimized for SMPS Supply
- Low Leakage Current in Shutdown Mode: $<5 \mu\text{A}$
- Internal Voltage Regulator
- Optimized for a 50Ω System
- Internal DC blocks on IN/OUT RF ports
- 1.8 V Control Logic
- RoHS Compliant Package, $260 \text{ }^\circ\text{C}$ MSL-3

APPLICATIONS

- Wireless Handsets and Data Devices for:
 - WCDMA/HSPA PCS Band 2 & 25
 - CDMA/EVDO Bandclass 1 & 14G

PRODUCT DESCRIPTION

The AWT5002 PA is designed to provide highly linear output for WCDMA and CDMA handsets and data devices with high efficiency at high power mode. This ANADIGICS PA can be used with an external switch mode power supply (SMPS) to improve its efficiency and reduce current consumption further at high, medium and low output powers. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. There are three selectable bias modes that optimize efficiency for different output power levels, and a shutdown mode with low leakage current, which increases handset talk and standby time. The self-contained $3 \text{ mm} \times 3 \text{ mm} \times 0.9 \text{ mm}$ surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50Ω system.

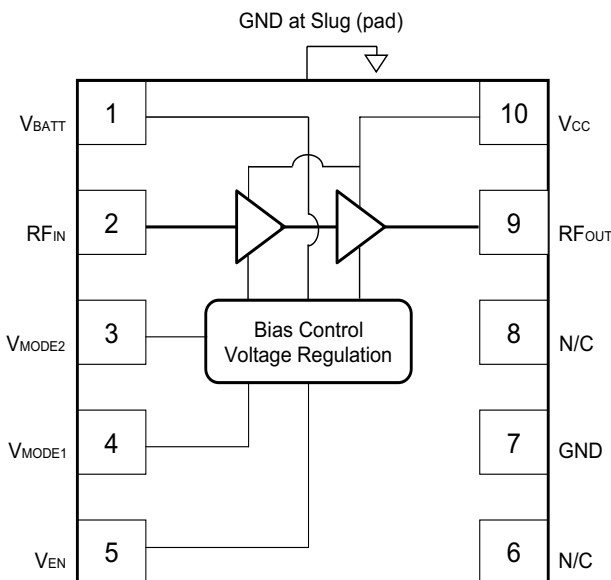
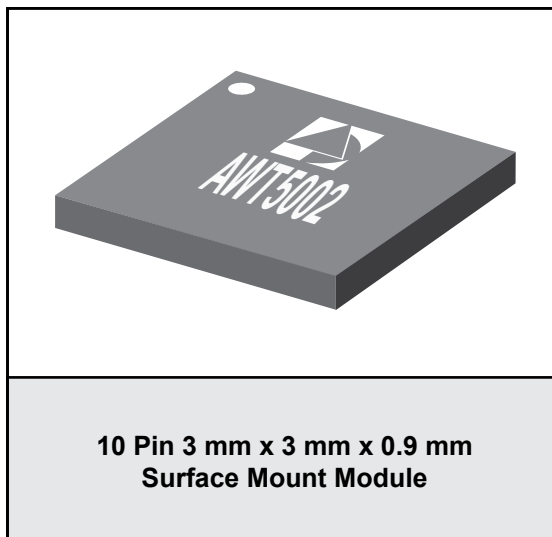


Figure 1: Block Diagram

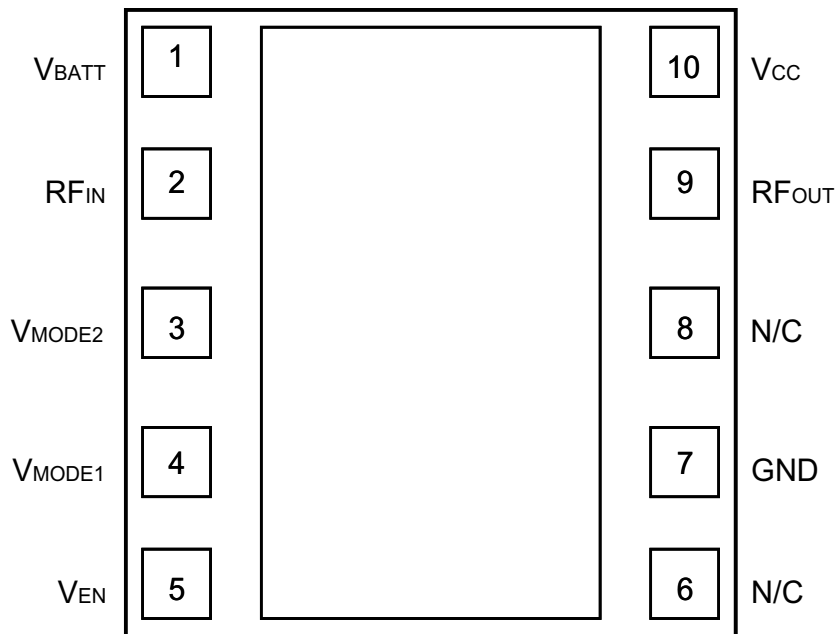


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{BATT}	Battery Voltage
2	RF_{IN}	RF Input
3	V_{MODE2}	Mode Control Voltage 2
4	V_{MODE1}	Mode Control Voltage 1
5	V_{EN}	PA Enable Voltage
6	N/C	No Connection
7	GND	Ground
8	N/C	No Connection
9	RF_{OUT}	RF Output
10	V_{CC}	Supply Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
RF Input (P_{IN})	-	-	10	dBm
V_{CC}	-1.2	3.4	5	V
V_{BATT}	-1.2	3.4	6	V
Control Voltage (V_{ENABLE} , V_{MODE})	0	1.8	3.5	V
Storage Temperature ($T_{STORAGE}$)	-40	25	150	°C

Functional operation to the specified performance is not implied under these conditions. Operation of any single parameter in excess of the absolute ratings may cause permanent damage. No damage occurs if one parameter is set at the limit while all other parameters are set within normal operating ranges.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	1850	-	1915	MHz	
Supply Voltage (V_{CC})	+0.6	+3.4	+4.4	V	$P_{OUT} \leq +28.5$ dBm
Battery Voltage (V_{BATT})	+3.1	+3.4	+4.4	V	$P_{OUT} \leq +28.5$ dBm
Enable Voltage (V_{ENABLE})	+1.35 0	+1.8 0	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE1})	+1.35 0	+1.8 0	+3.1 +0.5	V	Low Bias Mode High Bias Mode
RF Output Power (P_{OUT}) ⁽¹⁾ R99 WCDMA, HPM HSPA (MPR = 0), HPM R99 WCDMA, MPM HSPA (MPR = 0), MPM R99 WCDMA, LPM HSPA (MPR = 0), LPM	27.7 26.7 - - - -	28.5 27.5 18 17 8 7	- - - - - -	dBm	3GPP TS 34.121-1, Rel 8 Table C.11.1.3, Subtest 1
CDMA Output Power ⁽¹⁾ HPM MPM LPM	27.2 - -	28.0 17 7	- - -	dBm	CDMA2000, RC-1
Case Temperature (T_C)	-30	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) For operation at $V_{CC} = +3.1$ V, P_{OUT} is derated by 0.8 dB.

Table 4: Electrical Specifications - WCDMA Operation (R99 waveform)
(T_C = +25 °C, V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system, unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS			
					P _{OUT}	V _{CC}	V _{MODE1}	V _{MODE2}
Gain	25 17 14	28.5 21.5 17	32 24.5 21	dB	+28.5 dBm +18 dBm +8 dBm	3.4 V 1.4 V 0.8 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR1 at 5 MHz offset ⁽¹⁾	- - -	-40 -41 -43	-36 -36 -36	dBc	+28.5 dBm +18 dBm +8 dBm	3.4 V 1.4 V 0.8 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR2 at 10 MHz offset ⁽¹⁾	- - -	-52 -55 -54	-47 -47 -47	dBc	+28.5 dBm +18 dBm +8 dBm	3.4 V 1.4 V 0.8 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Efficiency ⁽¹⁾	- - -	48 30 16	- - -	%	+28.5 dBm +18 dBm +8 dBm	3.4 V 1.4 V 0.8 V	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (I _{cq}) Low Bias Mode	-	25	-	mA	through V _{CC} pin, V _{MODE1,2} = +1.8 V			
Mode Control Current	-	0.05	0.1	mA	through V _{MODE} pin, V _{MODE1,2} = 1.8 V			
Enable Current	-	0.05	0.1	mA	through V _{ENABLE} pin			
BATT Current	-	2.5	4.5	mA	through V _{BATT} pin, V _{MODE1,2} = +1.8 V			
Leakage Current	-	<5	10	μA	V _{BATT} = +4.4 V, V _{CC} = +4.4 V V _{ENABLE} = 0 V, V _{MODE1,2} = 0 V			
Noise in Receive Band ⁽²⁾	-	-134	-	dBm/Hz	P _{OUT} < +28.5 dBm			
Harmonics 2f _o 3f _o , 4f _o	- - -	-45 -50	-30 -35	dBc	P _{OUT} < +28.5 dBm			
Input Impedance	-	-	2:1	VSWR				
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P _{OUT} ≤ +28.5 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions			
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range			

Notes:

(1) ACLR and Efficiency measured at 1880 MHz.

(2) Noise measured at 1930 MHz to 1990 MHz.

Table 5: Electrical Specifications - CDMA Operation (CDMA2000, RC-1)
 (T_C = +25 °C, V_{BATT} = +3.4 V, V_{EN} = +1.8 V, 50 Ω system, unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS			
					P _{OUT}	V _{CC}	V _{MODE1}	V _{MODE2}
Gain	25	28.5	32	dB	+28 dBm	3.4 V	0 V	0 V
	17	21.5	24.5		+17 dBm	1.4 V	1.8 V	0 V
	14	17	21		+7 dBm	0.8 V	1.8 V	1.8 V
Adjacent Channel Power ⁽¹⁾ at +1.25 MHz offset Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	-	-50	-46	dBc	+28 dBm	3.4 V	0 V	0 V
	-	-60	-46		+17 dBm	1.4 V	1.8 V	0 V
	-	<-60	-46		+7 dBm	0.8 V	1.8 V	1.8 V
Adjacent Channel Power ⁽¹⁾ at +1.98 MHz offset Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	-	-56	-53	dBc	+28 dBm	3.4 V	0 V	0 V
	-	<-60	-53		+17 dBm	1.4 V	1.8 V	0 V
	-	<-60	-53		+7 dBm	0.8 V	1.8 V	1.8 V
Efficiency ⁽¹⁾	-	44	-	%	+28 dBm	3.4 V	0 V	0 V
	-	28	-		+17 dBm	1.4 V	1.8 V	0 V
	-	13	-		+7 dBm	0.8 V	1.8 V	1.8 V

Notes:

(1) ACLR and Efficiency measured at 1880 MHz.

Table 6: Bias Control

APPLICATION	P _{OUT} LEVELS	BIAS MODE	V _{ENABLE}	V _{MODE1}	V _{MODE2}	V _{CC}	V _{BATT}
High power (High Bias Mode)	> +16 dBm	High	+1.8 V	0 V	0 V	0.6 - 4.4 V	3.1 - 4.4 V
Med power (Med Bias Mode)	≤ +18 dBm	Medium	+1.8 V	+1.8 V	0 V	0.6 - 4.4 V	3.1 - 4.4 V
Low power (Low Bias Mode)	≤ +8 dBm	Low	+1.8 V	+1.8 V	+1.8 V	0.6 - 4.4 V	3.1 - 4.4 V
Shutdown	-	Shutdown	0 V	0 V	0 V	0.6 - 4.4 V	3.1 - 4.4 V

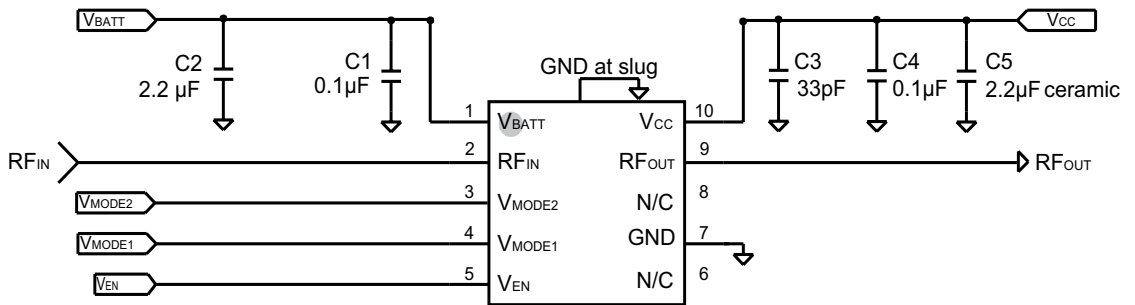
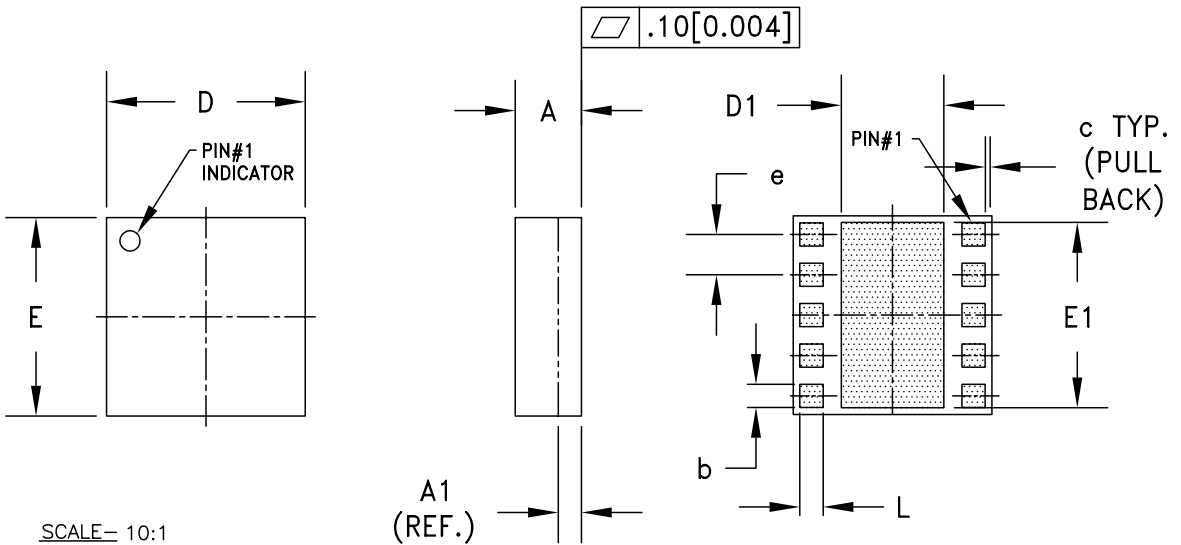


Figure 4: Evaluation Board Schematic

PACKAGE OUTLINE



SCALE= 10:1

SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.88	0.94	1.00	0.035	0.037	0.039	-
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						-
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	-	0.10	-	-	0.004	-	-
D	2.88	3.00	3.12	0.113	0.118	0.123	-
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	-
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e	0.60			0.024			3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS IN MILLIMETERS.
2. UNLESS SPECIFIED, TOLERANCE=±0.076[0.003].
3. SIGNAL PADS SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO THE PRODUCT DESIGN.
4. GROUND PADS SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL SIZE AND LOCATION ARE REFERENCE ONLY.
5. PITCH MEASUREMENTS (e) TAKE CENTERLINE TO CENTERLINE OF SOLDERMASK OPENINGS.
6. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
7. LAMINATE CONTROL DRAWING SPECIFIED BY PRODUCT DESIGN.

Figure 5: Package Outline - 10 Pin 3 mm x 3 mm x 0.9 mm Surface Mount Module

TOP BRAND

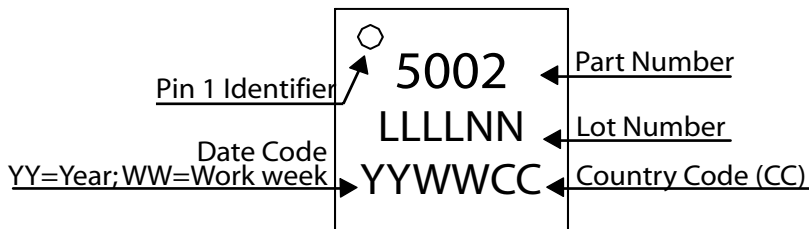
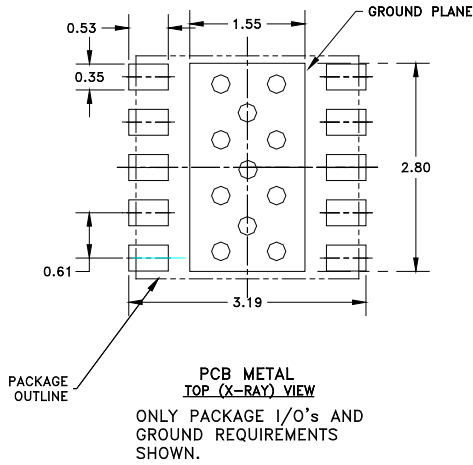


Figure 6: Branding Specification

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

- (1) OUTLINE DRAWING REFERENCE: P8002478_E
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.
- (4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.
- (5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)

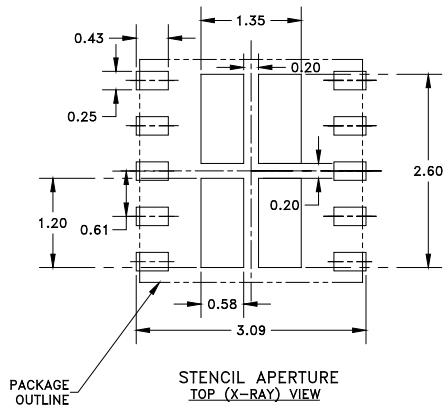
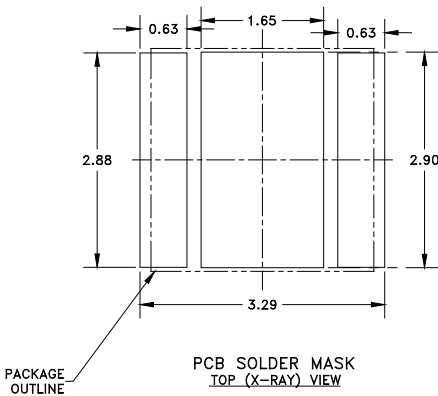
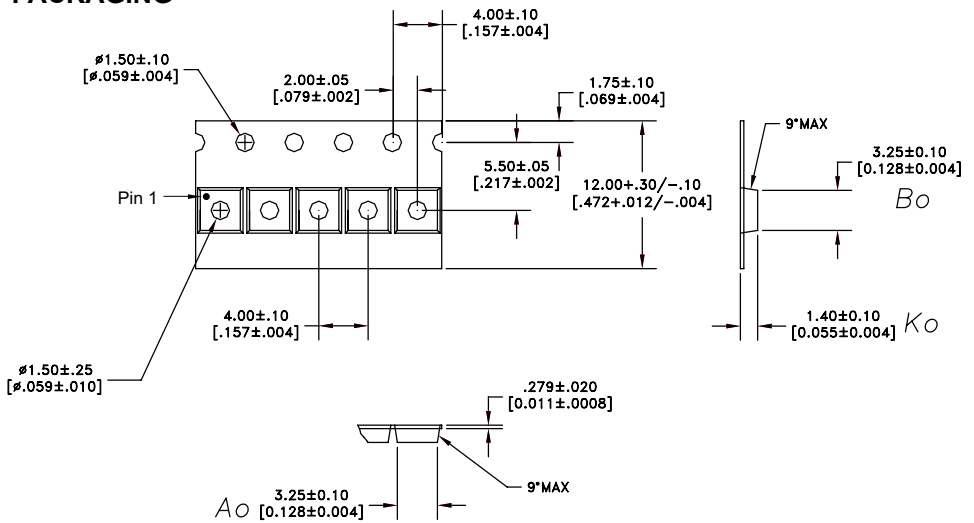


Figure 7: Recommended PCB Layout Information

COMPONENT PACKAGING



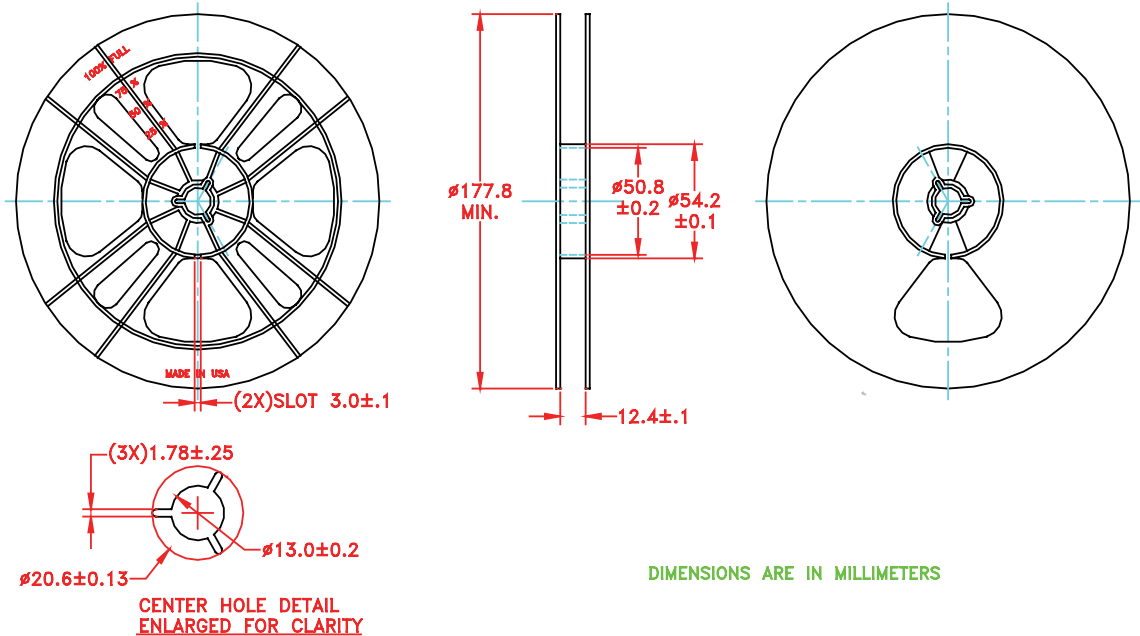
NOTES:

- 1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

Figure 8: Carrier Tape



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- 1. MATERIAL: BLACK CARBON POLYSTYRENE
- SURFACE RESISTIVITY: 1X10⁴TO 1X10⁸ ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

Figure 9: Reel

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT5002Q7	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 0.9 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWT5002P9	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 0.9 mm Surface Mount Module	Partial Tape and Reel



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