Look-Ahead Carry Generators

SN54S182 SN74S182

Features/Benefits

- **Provides lookahead carry scross a group of four 'S381s**
- **Capable of multilevel lookahead carry for high-speed arithmetic operations over long wordlengths**
- **High-speed operation**

Description

The SN54S182 and SN74S182 are high-speed, lookahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full lookahead across n-bit adders. Carry, carry-generate and carry-propagate functions are provided as enumerated in the pin designation table below.

When used in conjunction with 74S381, 74F381, 74S181 or 2901 arithmetic logic units (ALU), these generators provide high-speed carry lookahead capability for any word length. Each 'S182 generates the lookahead (anticipated carry) across a group of four ALUs and, in addition, other carry lookahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to any number of levels.

The carry functions (input, outputs, generate and propagate) of the carry lookahead generators are implemented in the compatible form for directed connection to the ALU. Logic equations for the 'S182 are:

$C_{n+x} = G0 + P0\ Cn$

$C_{n+y} = G1 + P1\ G0 + P1\ P0\ Cn$

$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$

$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$

$\overline{P} = \overline{P3\ P2\ P1\ P0}$

or

$\overline{C}n+x = \overline{Y0\ (X0 + Cn)}$

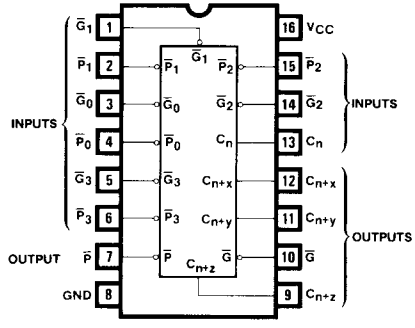
$\overline{C}n+y = \overline{Y1\ [X1 + Y0\ (X0 + Cn)]}$

$\overline{C}n+z = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + Cn)]\}}$

$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$

$X = X3 + X2 + X1 + X0$

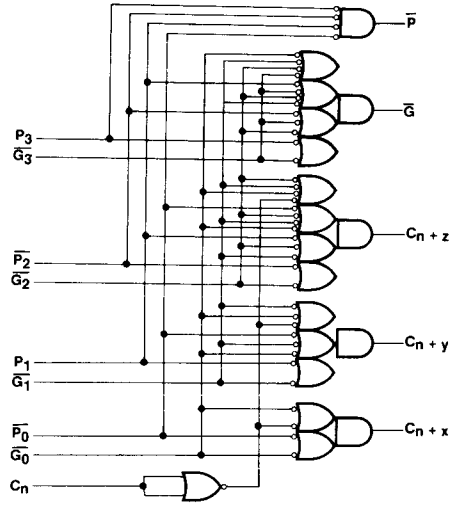
Pin Configuration



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S182	F,J,W,(20L)	Military
SN74S182	N,J	Commercial

Logic Diagram



Summarizing Tables

FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	Cn	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	Cn	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{C}n$	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = High Level, L = Low Level, X = Irrelevant. Any inputs not shown in a given table are irrelevant with respect to that output.

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Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Storage temperature range ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2						V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5 V	Cn input			−2			−2	V
				$\overline{P3}$ input			−4			−4	mA
				$\overline{P2}$ input			−6			−6	
				$\overline{P0}$, $\overline{P1}$, or $\overline{G3}$ input			−8			−8	
				$\overline{G0}$ or $\overline{G2}$			−14			−14	
				$\overline{G1}$ input			−16			−16	
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7 V	Cn input			50			50	μA
				$\overline{P3}$ input			100			100	
				$\overline{P2}$ input			150			150	
				$\overline{P0}$, $\overline{P1}$, or $\overline{G3}$ input			200			200	
				$\overline{G0}$ or $\overline{G2}$			350			350	
				$\overline{G1}$ input			400			400	
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V				1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OL} = 20 mA				0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OH} = −1 mA		2.5	3.4		2.7	3.4		V
I_{OS}	Output short-circuit current*	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX	See Note 1			69	109		69	99	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5 V	See Note 2			35			35		mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

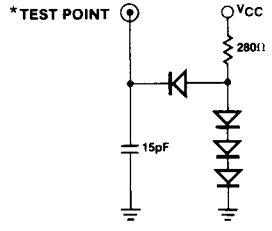
NOTE: 1. I_{CCL} is measured with all outputs open, inputs $\overline{G0}$, $\overline{G1}$ and $\overline{G2}$ at 4.5 V, and all others inputs grounded.

2. I_{CCH} is measured with all outputs open, inputs $\overline{P3}$ and $\overline{G3}$ at 4.5 V, and all others inputs grounded.

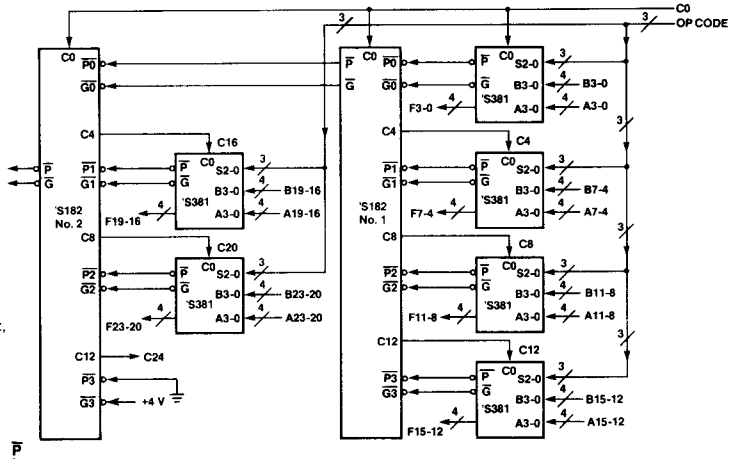
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	FROM (INPUT)	TO (OUTPUT)	5/74S182 TYP	5/74S182 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high	C_L = 15 pF R_L = 280Ω	$\overline{G0},\overline{G1},\overline{G2},\overline{G3}$	Cn + x, Cn + y or Cn + z	4.5	7	ns
t_{PHL}	Propagation delay time, high-to-low		$\overline{P0},\overline{P1},\overline{P2}$ or $\overline{P3}$		4.7	7	ns
t_{PLH}	Propagation delay time, low-to-high		$\overline{G0},\overline{G1},\overline{G2},\overline{G3}$	$\overline{G}$	5	7.5	ns
t_{PHL}	Propagation delay time, high-to-low		$\overline{P1},\overline{P2}$, or $\overline{P3}$		7	10.5	ns
t_{PLH}	Propagation delay, low-to-high		$\overline{P0},\overline{P1},\overline{P2}$ or $\overline{P3}$	$\overline{P}$	4.5	6.5	ns
t_{PHL}	Propagation delay, high-to-low				6.5	10	ns
t_{PLH}	Propagation delay, low-to-high		Cn	Cn + x, Cn + y or Cn + z	6.5	10	ns
t_{PHL}	Propagation delay high-to-low				7	10.5	ns

Standard Test Load

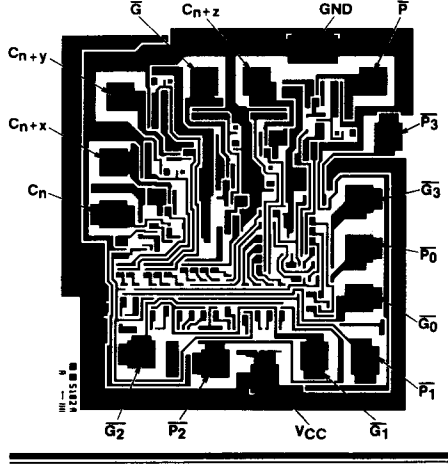


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



A 24-bit ALU made from 'S381s and 'S182s

Die Configuration



Die Size: 53x57 mil^2