

M-986-1R2 & -2R2 MF Transceivers

Teltone M-986-1R2 and -2R2 MFC Transceivers contain all the logic necessary to transmit and receive CCITT R2F (forward) and R2B (backward) multifrequency signals on one integrated circuit (IC). M-986-1R2 is a single-channel version; M-986-2R2 provides two channels. R1 single and dual multifrequency transceivers are also available as M-986-1R1 and -2R1.

Operating with a 20.48 MHz crystal, the M-986 is capable of providing a direct digital interface to an A-law-encoded PCM digital input. Each channel can be connected to an analog source using a coder-decoder (codec) as shown in Figure 1.

The M-986 can be configured by the customer to operate with the transmitter and receiver either coupled together or independent, allowing it to handle a compelled cycle automatically or via command from the host processor. For the R2 versions of the M-986, A-law is used for coding/decoding. The M-986 is configured and controlled through an integral coprocessor port.

Features

- Direct A-Law PCM digital input
- 2.048 Mb/s clocking
- Programmable forward/backward mode
- Programmable compelled/direct control
- Operates with standard codecs for analog interfacing
- Microprocessor read/write interface
- Binary or 2-of-6 data formats
- Single- or dual-channel versions
- 5 volt power

Applications

- Test equipment
- Trunk adapters
- Paging terminals
- Traffic recorders
- PBXs

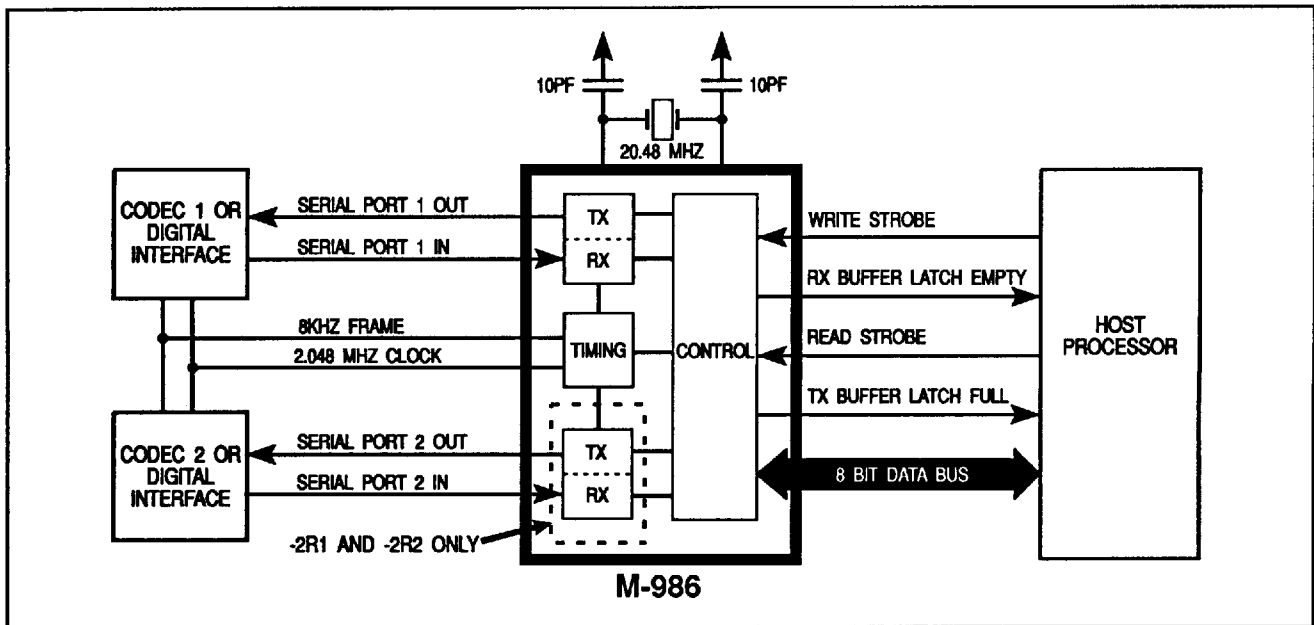


Figure 1 Block Diagram

Functional Description

The M-986 can be set up for various operating modes by writing two configuration bytes to the coprocessor port. The format of the two configuration bytes is shown in Table 1 and the configuration options are described in the following paragraphs.

Configuration Options

External/Internal Codec Clock (ECLK): If external codec clocking is selected, an external clocking source provides an 8kHz transmit framing clock and an 8kHz receive framing clock. It also provides a serial bit clock with a frequency that is a multiple of 8 kHz between 2.496 MHz and 216 kHz for exchange of data via the serial ports. When internal codec clocking is selected, the M-986 provides an 8kHz framing clock and a 2.048 MHz serial bit clock.

Binary/2 of 6 Input/Output (IOM): When the 2-of-6 input/output is selected, the M-986 encodes the received R2 MF tone pair into a 6-bit format, where each bit represents one of the six possible frequencies. A logic high level indicates the presence of a frequency. The digital input to the M-986 that selects the transmitted R2 MF tone pair must also be coded in the 2-of-6 format. See Table 2.

When binary input/output is selected, the M-986 encodes the received R2 MF tone pair into a 4 bit binary format. The

digital input to the M-986 that selects the transmitted R2 MF tone pair must also be coded in a 4 bit binary format. See Table 3.

Enable/Disable Channel (ENC): When a channel is disabled, the receiver does not process its codec input for R2 MF tones, and the transmitter does not respond to transmit commands. If a transmit command is given while the channel is enabled, the "tone off" command must be given before the channel is disabled. Disabling the channel does not automatically shut off the transmitter. When a channel is enabled, the receiver and transmitter for that channel function normally.

End-of-Digit Indication (EOD): The end-of-digit indication option configures the M-986 to inform the host processor when the far end terminates transmission of the R2 MF tone it is sending. If this option is disabled, the host processor will not be notified when tone transmission terminates.

Automatic Compelled/Manual Sequence Signaling (CMP): When manual mode is selected, R2 MF tone transmission is turned on and off only via command from the host processor.

If the automatic mode is selected, the transmitter and receiver perform the compelled signaling handshake automatically. The specifics of operation are different for the forward and backward configurations.

Table 1 Configuration Bytes

CONFIGURATION BYTE 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	ECLK	IOM	ENC1	EOD1	CMP1	FB1
ECLK	Channels 1 & 2	1 = External codec clock; 0 = Internal codec clock					
IOM	Channels 1 & 2	1 = Binary input/output; 0 = 2-of-6 input/output					
ENC1	Channel 1	1 = Enable channel; 0 = Disable channel					
EOD1	Channel 1	1 = Indicate end of digit; 0 = No end of digit indication					
CMP1	Channel 1	1 = Automatic compelled mode; 0 = Manual mode					
FB1	Channel 1	1 = Forward mode (Tx forward frequencies and Rx backward frequencies) 0 = Backward mode (Tx backward frequencies and Rx forward frequencies)					
CONFIGURATION BYTE 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	ENC2	EOD2	CMP2	FB2
ENC2	Channel 2	1 = Enable channel; 0 = Disable channel					
EOD2	Channel 2	1 = Indicate end of digit; 0 = No end of digit indication					
CMP2	Channel 2	1 = Automatic compelled mode; 0 = Manual mode					
FB2	Channel 2	1 = Forward mode (Tx forward frequencies and Rx backward frequencies) 0 = Backward mode (Tx backward frequencies and Rx forward frequencies)					

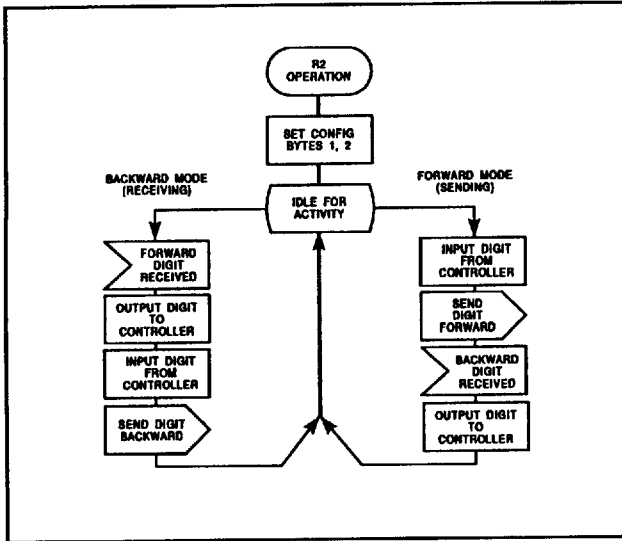


Figure 2 Automatic Compelled Mode Operation

In forward mode, the transceiver can exist in two states, STATE 1 and STATE 2:

- . STATE 1: No backward signal detected.
Transmitter under control of the host.
- . STATE 2: Backward signal detected.
Transmitter off unconditionally.

A Transmit Tone Command written while the transceiver is in STATE 1 will be acted upon immediately. The transmitter is unconditionally disabled upon entry into STATE 2. If a transmit command is written to the transceiver while in STATE 2, that command will become pending. Upon entry into STATE 1, a pending transmit command is acted upon.

In backward mode, the transceiver can exist in two states, STATE 1 and STATE 2:

- . STATE 1: No forward signal detected.
Transmitter off unconditionally.
- . STATE 2: Forward signal detected.
Transmitter transmits backward signal.

Table 2 2 of 6 Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	F6	F5	F4	F3	F2	F1
Receive tone return	0	CHN	F6	F5	F4	F3	F2	F1

CHN: 1 = channel 2; 0 = channel 1
R2 MF Frequencies:

Bit name	Forward (Hz)	Backward (Hz)	Bit name	Forward (Hz)	Backward (Hz)
F6	1980	540	F3	1620	900
F5	1860	660	F2	1500	1020
F4	1740	780	F1	1380	1140

Table 3 Binary Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	0	0	A	B	C	D
Receive tone return	0	CHN	0	0	A	B	C	D

CHN: 1 = channel 2; 0 = channel 1
R2 MF Frequencies:

ABCD	Forward (Hz)	Backward (Hz)	ABCD	Forward (Hz)	Backward (Hz)
0000	Tone off	Tone off	1000	1500 & 1860	1020 & 660
0001	1380 & 1500	1140 & 1020	1001	1620 & 1860	900 & 660
0010	1380 & 1620	1140 & 900	1010	1740 & 1860	780 & 660
0011	1500 & 1620	1020 & 900	1011	1380 & 1980	1140 & 540
0100	1380 & 1740	1140 & 780	1100	1500 & 1980	1020 & 540
0101	1500 & 1740	1020 & 780	1101	1620 & 1980	900 & 540
0110	1620 & 1740	900 & 780	1110	1740 & 1980	780 & 540
0111	1380 & 1860	1140 & 660	1111	1860 & 1980	660 & 540

A transmit tone command written while the transceiver is in STATE 2 will be acted upon immediately. The transmitter is unconditionally disabled upon entry into STATE 1. If a transmit command is written to the transceiver while in STATE 1, that command will become pending. Upon entry into STATE 2, a pending transmit command is acted upon.

EXAMPLE: Assume that the transceivers at both ends of a link are configured in automatic compelled mode. Both transceivers are in STATE 1. A compelled signaling sequence begins with the R2F host writing a transmit command byte to its transceiver via the coprocessor bus. The transceiver immediately begins transmitting the signal.

The R2B transceiver detects the signal, enters STATE 2, and outputs the received tone code to its host via the coprocessor port. If the R2B host had determined the next tone to transmit and written a transmit command to the transceiver prior to entry into STATE 2, the state transition will cause this tone to be transmitted. Otherwise, the R2B transmitter waits for a transmit tone command from the host, and starts transmitting a tone once the transmit tone command is received.

The R2F transceiver detects the backward signal, enters STATE 2, and outputs the received tone code to its host. Entry into STATE 2 unconditionally disables the transmitter.

The R2B transceiver detects the absence of signal, enters STATE 1, and informs the host with the end-of-tone code if configured to do so. Entry into STATE 1 unconditionally disables the transmitter.

The R2F transceiver detects the absence of signal, enters STATE 1, and informs the host with the end-of-tone code if configured to do so. If the R2F host had determined the next signal to transmit and written a transmit command to the transceiver prior to entry into STATE 1, the state transition will cause this signal to be transmitted. Otherwise, the transmitter remains silent until the next transmit command by its host.

Forward/Backward Frequencies (FB): When forward mode is selected, the R2F (forward) frequencies are transmitted and R2B (backward) frequencies are received. When backward mode is selected, R2B frequencies are transmitted and R2F frequencies are received. The R2F frequencies are 1380, 1500, 1620, 1740, 1860, and 1980 Hertz. The R2B frequencies are 540, 660, 780, 900, 1020, and 1140 Hz.

Initial Configuration: The configuration of the M-986 immediately after a reset will be as follows:

- End-of-digit indication ON
- Forward mode ON
- Channel disabled
- 2-of-6 input/output
- External serial and serial frame clocks.

Also, the M-986 will place 00 hex on the coprocessor port to indicate to the host processor that it is working.

Transmit Tone Command

The transmit tone command allows the host processor to transmit any two of the 6 possible frequencies in the transmission mode the channel has been configured for (forward or backward). The format of the command depends on whether the M-986 is configured for binary format or 2-of-6 format. See Tables 2 and 3.

Received Tone Detection

When a tone is detected by the M-986, the $\overline{\text{TBLF}}$ output goes low, indicating reception of the tone to the host processor. The host processor can determine which tone was detected and which channel the tone was detected on by reading data from the M-986 coprocessor port. The M-986 will return a single byte indicating the tone received and the channel that the tone was received on. The format of the returned byte depends on whether the M-986 is configured for binary or 2-of-6 coding. See Tables 2 and 3.

Coprocessor Port

Commands are written to the M-986 via the coprocessor port, and data indicating the received R2 MF tone is read from the coprocessor port.

Writing to the Coprocessor Port: The following sequence describes writing a command to the M-986.

- (1) The $\overline{\text{WR}}$ signal is driven low by the host processor.
- (2) The $\overline{\text{RBLE}}$ (receive buffer latch empty) signal transitions to a logic high level.
- (3) Data is written from LD7-LD0 to the receive buffer latch (D7-D0) when the $\overline{\text{WR}}$ signal goes high.
- (4) The $\overline{\text{RBLE}}$ signal transitions to a logic low level after the M-986 reads the data. This signals the host processor that the receive buffer is empty.

Note: The $\overline{\text{RBLE}}$ should be low before writing to the coprocessor.

Reading the Coprocessor Port: The following sequence describes reading received tone information from the coprocessor port.

- (1) The $\overline{\text{TBLF}}$ (transmit buffer latch full) port pin on the M-986 goes low indicating the reception of a tone.
- (2) The host processor detects the low logic level on the $\overline{\text{TBLF}}$ pin either by polling a connected port pin or by an interrupt.
- (3) The host processor drives the $\overline{\text{RD}}$ signal low.
- (4) The $\overline{\text{TBLF}}$ (transmit buffer latch full) signal transitions to a logic high level.
- (5) Data is driven onto LD7-LD0 by the M-986 until the $\overline{\text{RD}}$ signal is driven high by the host processor.

Clock Characteristics and Timing

Internal Clock Option: The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The crystal must be 20.48 MHz, fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pf.

External Clock Option: An external frequency source can be used by injecting the frequency directly in X2/CLKIN, with X1 left unconnected. The external frequency injected must conform to the specifications listed in Table 8.

Flammability/Reliability Specifications

Reliability: 185 FITS failures/billion hours
 Flammability: Passes UL 94 V-0 tests

Ordering Information

M-986-1 R 2 C L

1 or 2 channels ———
 CCITT SYSTEM R1 or R2 ———
 P = plastic; C = ceramic ———
 L = leaded chip carrier (optional marking)

MF Signaling References

1. CCITT Blue Book, Fascicle VI.4 Q.310 - Q490. Contains specifications of signaling systems R1 and R2. If not available at your local university library, contact:

OMNICOM
 115 Park Street S.E.
 Vienna, VA 22180
 1-703 -281-1135

2. Bellcore Technical Publications. 1-800-521-2673
 TR-NPL-000275—Notes on the Network (primarily deals with MF R1 because it pertains to the U.S. domestic Telco market.

3. Reference Manual for Telecommunications by Roger L. Freeman, ISBN-0-471-86753-5

A-law/ μ -law version available.
 Call for information.

See Section 9 for PLCC package information.

Table 4 Signal Descriptions

SIGNAL	PIN	I/O/Z	DESCRIPTION
D15-D8	18-11	I/O/Z	Unused. Leave open.
D7-D0	19-26	I/O/Z	8-bit coprocessor latch.
TBLF	40	O	Transmit buffer latch full flag.
RBLE	1	O	Receive buffer latch empty flag
HI/LO	2	I	Latch byte select pin. Tie low.
BIO	9	I	Unused. Leave open.
RD	32	I/O	Used by the external processor to read from the coprocessor latch by driving the RD line active (low), thus enabling the output latch to drive the latched data. When the data has been read, the external device must bring the RD line high.
EXINT	5	I	Unused. Leave open.
MC	3	I	Microcomputer mode select pin. Tie low.
MC/PM	27	I	Coprocessor mode select pin. Tie low.
RS	4	I	Reset input for initializing the device. When an active low is placed on RS pin for a minimum of five clock cycles, RD and WR are forced high, and the data bus (LD7 through LD0) goes to a high impedance state. The serial port clock and transmit outputs also go to the high impedance state.
WR	31	I/O	Used by the external processor to write data to the coprocessor port. To write data the external processor drives the WR line low, places data on the data bus, and then drives the WR line high to clock the data into the on-chip latch.
XF	28	O	Watchdog signal. Toggles at least once every 15 milliseconds when the processor is functioning properly. If the pin is not toggled at least once every 10 ms, the processor is lost and should be reset.
CLKOUT	6	O	System clock output (one-fourth crystal/CLKIN frequency, nominally 5.12 MHz).

Table 4 Signal Descriptions (continued)

SIGNAL	PIN	I/O/Z	DESCRIPTION
CLKOUT	6	O	System clock output (one-fourth crystal/CLKIN frequency, nominally 5.12 MHz)
V _{CC}	30	I	5V supply pin
V _{SS}	10	I	Ground pin
X1	7	O	Crystal output for internal oscillator. If an internal oscillator is not used, this pin should be left unconnected.
X2/CLKIN	8	I	Input to internal oscillator (X2) from crystal, or input for external oscillator (CLKIN).
DR1 & DR0	33 & 29	I	Serial-port receive-channel inputs. 2.048 MHz serial data is received in the receive registers via these pins.
DX1 & DX0	36 & 35	O	Serial-port transmit-channel outputs. 2.048 MHz serial data is transmitted from the transmit registers on these pins. These outputs are in the high-impedance state when not transmitting. DX0 = channel 1; DX1 = channel 2
FR	37	O	8 kHz internal serial-port framing output. If internal clocking is selected, serial-port transmit and receive operations occur simultaneously on an active (high) FR framing pulse.
$\overline{\text{FSR}}$	39	I	8 kHz external serial-port receive-framing input. If external clocking is selected, data is received via the receive pins (DR1 and DR0) on the active (low) FSR input. The falling edge of FSR initiates the receive process, and the rising edge causes the M-986 to process the data.
$\overline{\text{FSX}}$	38	I	8 kHz external serial-port transmit-framing input. If external clocking is enabled, data is transmitted on the transmit pins (DX1, DX0) on the active (low) input. The falling edge of FSX initiates the transmit process, and the rising edge causes the M-986 to internally load data for the next cycle.
SCLK	34	I/O/Z	2.048 MHz serial-port clock. Master clock for transmitting and receiving serial-port data. Configured as an input in external clocking mode or output in internal clocking mode. Reset ($\overline{\text{RS}}$) forces SCLK to the high-impedance state.

Table 5 Absolute Maximum Ratings Over Specified Temperature Range

Supply voltage range, V _{CC}	-0.3 V to 7 V
Input voltage range	-0.3 V to 15 V
Output voltage range	-0.3 V to 15 V
Ambient air temperature range	0 °C to 70 °C
Storage temperature range	-45 °C to 150 °C

Table 6 Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{SS}	Supply voltage		0		V
V _{IH}	High-level input voltage	All inputs except CLKIN	2		V
		CLKIN	3		V
		MC/PM	2.2		V
V _{IL}	Low-level input voltage	All inputs except MC/MP		0.8	V
		MC/MP		0.6	V
I _{OH}	High-level output current (all outputs)			-300	μA
I _{OL}	Low-level output current (all outputs)			2	mA

Table 7 Electrical Characteristics Over Specified Temperature Range

Parameter		Test Conditions	Min	Typ	Max	Unit
ICC	Supply current	f = 20.5 MHz, V _{CC} = 5.5V, T _A = 0 ° to 70 ° C		50	75	mA
VOH	High-level output voltage	I _{OH} = MAX	2.4	3		V
		I _{OH} = 20 μA	V _{CC} - 0.4			V
VOL	Low-level output voltage	I _{OL} = MAX		0.3	0.6	V
IOZ	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		20	μA
			V _O = 0.4 V		-20	μA
II	Input current	V _I = V _{SS} to V _{CC}	Except CLKIN		±20	μA
			CLKIN		±50	μA
CI	Input capacitance	Data bus		25		pF
		All others		15		pF
CO	Output capacitance	Data bus		25		pF
		All others		10		pF

Table 8 External Frequency Specifications

Parameter	Min	Nom	Max	Unit
t _{Q(MC)} Master clock cycle time	48.818	48.828	48.838	ns
t _{r(MC)} Rise time master clock input		5	10	ns
t _{f(MC)} Pulse duration master clock	20			ns

Table 9 Serial Port Timing

Parameter	Min	Nom	Max	Unit
t _d (CH-FR)			70	ns
t _d (DX1-CL)	20			ns
t _d (DX2-CL)	20			ns
t _h (DX)	244			ns
t _{su} (DR)	20			ns
t _h (DR)	20			ns
t _c (SCLK)	399	488.28	4770	ns
t _f (SCLK)			30	ns
t _r (SCLK)			30	ns
t _w (SCLKL)	220	244.14	2500	ns
t _w (SCLKH)	220	244.14	2500	ns
t _{su} (FS)	100			ns

* The duty cycle of the serial port clock must be within 45% to 55%.

Table 10 Coprocessor Interface Timing

Parameter		Min	Nom	Max	Unit
t _d (R-A)	RD low to TBLF high			75	ns
t _d (W-A)	WR low to RBLE high			75	ns
t _a (RD)	RD low to data valid			80	ns
t _h (RD)	Data hold time after RD high	25			ns
t _{su} (WR)	Data setup time prior to WR high	30			ns
t _h (WR)	Data hold time after WR high	25			ns
t _w (RDL)	RD low-pulse duration	80			ns
t _w (WRL)	WR low-pulse duration	60			ns
t _{wr} (RBLE)	RBLE↑ to RBLE↓			1	ms

Table 11 Reset (RS) Timing

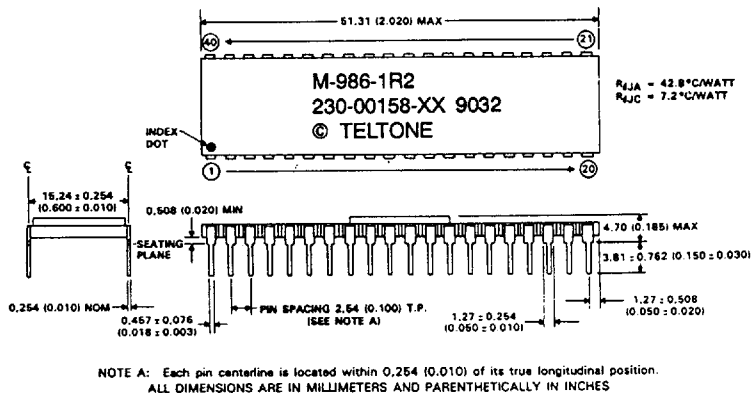
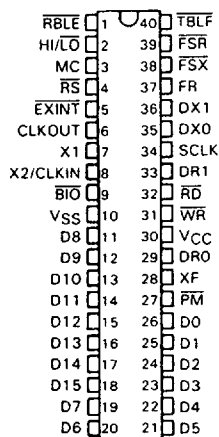
Parameter		Test Conditions	Min	Max	Unit
t _{dis} (R)	Data bus disable time after RS	R _L = 825 Ω C _L = 100 pF		75	ns
t _{d12}	Delay time from RS↓ to high-impedance SCLK			200	ns
t _{d13}	Delay time from RS↓ to high-impedance DX1, DX0			200	ns
t _{su} (R)	Reset (RS) setup time prior to CLKOUT		50		ns
t _w (R)	RS pulse duration		977		ns

Table 12 CLKOUT Timing Parameters

Parameter		Test Conditions	Min	Nom	Max	Unit
t _c (C)	CLKOUT cycle time	R _L = 825 Ω C _L = 100 pF	195.27	195.31	195.35	ns
t _r (C)	CLKOUT rise time			10		ns
t _f (C)	CLKOUT fall time			8		ns
t _d (MCC)	Delay time CLKIN↑ to CLKOUT↓		25		60	ns

Table 13 Transmitter Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
FOS	Frequency offset	From nominal			±1	Hz
TW	Twist	High/low			±0.5	dB
AS	Signal amplitude	Per component	-9.26	-8.86	-8.46	dBm0
TS	Time skew	Between components			0	ms
Phi	Power due to harmonic distortion and intermodulation	300 to 3400 Hz			-46.5	dBm0



PLCC, CLCC 44-PIN PACKAGES AVAILABLE.
CALL TELTONE FOR PIN CONFIGURATION DETAILS.

Figure 3 Pin Assignments

Figure 4 Package Dimensions

See Section 9 for PLCC package information.

Table 14 Receiver Characteristics

Parameter		Test Conditions	Min	Max	Unit
A _d	Detect amplitude	Per frequency	-35	-5	dBm0
A _{nd}	No-detect amplitude	Per frequency	-42	-35	dBm0
F _d	Detect with frequency offset	From nominal	±10		Hz
TW _d	Detect with twist	Adjacent frequencies	±5		dB
		Nonadjacent frequencies	±7		dB
TW _{nd}	No detect with twist		±20		dB
T _{3r}	Third R2F tone reject	Relative to highest level frequency	-20		dB
FF _d	Detect R2B with R2F disturbing	Above lowest level R2B tone (-12.5 dBm0 max.)	13.5		dB
FT _{nd}	No detect R2F with 2 out-of-band sine waves	Any frequencies from 330 - 1150 Hz and 2130 - 3400 Hz	-5		dBm0
RT _{nd}	No detect R2B with 2 out-of-band sine waves	Any frequencies from 1300-3400 Hz	-5		dBm0
T _{on}	Tone time	Reject	7		ms
T _{int}	Interrupted tone time	Reject	7		ms
T _{or}	Operate and release time			80	ms

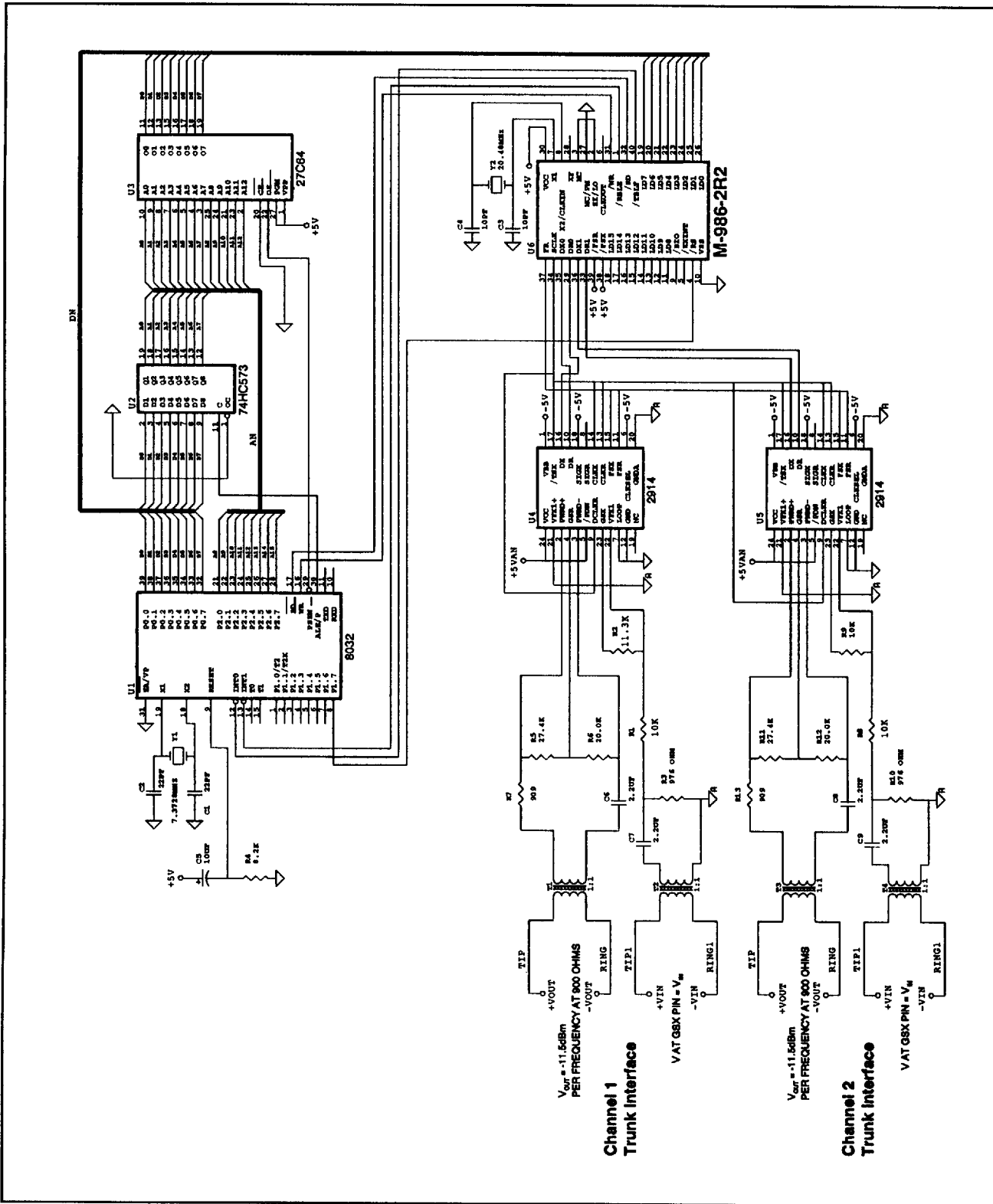
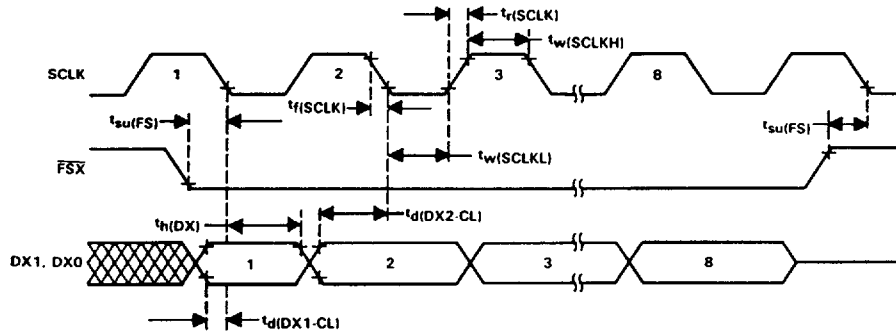


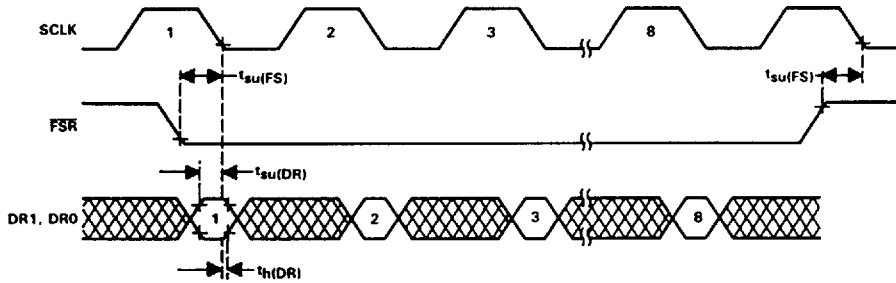
Figure 5 M-986 Dual Channel 4-wire Interface Application Circuit

External Framing: Transmit Timing



NOTES: Data valid on transmit outputs until SCLK rises.
The most significant bit is shifted first.

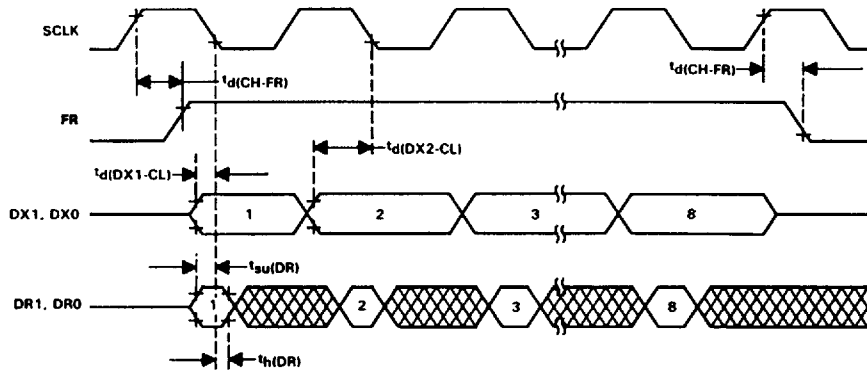
External Framing: Receive Timing



NOTE: The most significant bit is shifted first.

Figure 6 External Framing Timing Diagrams

Internal Framing



NOTE: The most significant bit is shifted first.

Figure 7 Internal Framing Timing

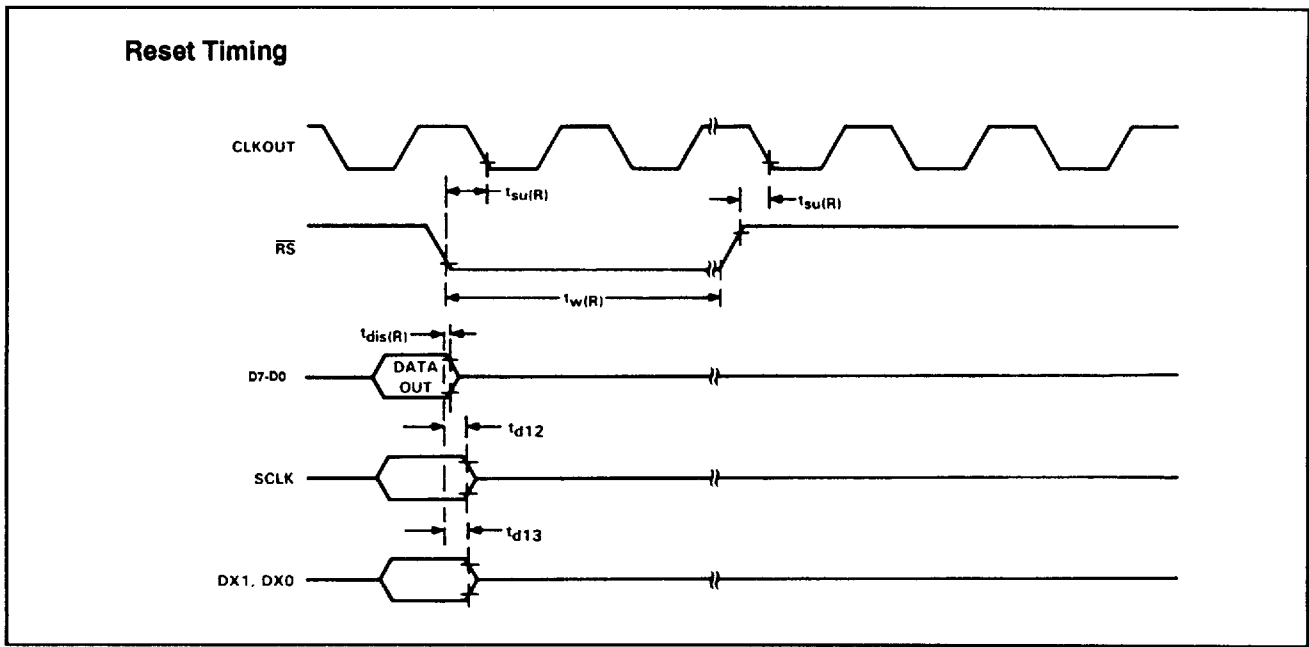


Figure 8 Reset Timing

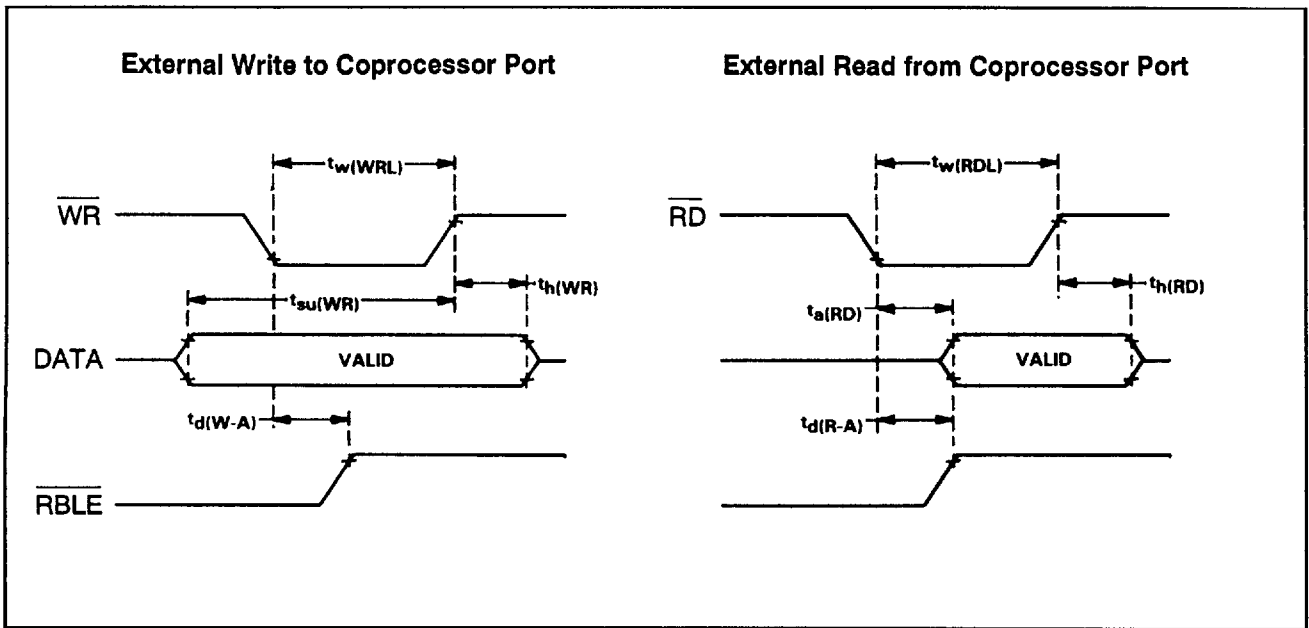


Figure 9 Coprocessor Timing