

## PRELIMINARY



**LG Semicon Co., Ltd.**

**GM76FV16256/ GM76FU16256/ GM76FS16256**  
**GM76FR16256**      262,144WORDS x 16 BIT  
**CMOS STATIC RAM**

### Description

The GM76FV16256/ GM76FU16256/ GM76FS16256/ GM76FR16256 is a 4,194,304 bits static random access memory organized as 262,144 words by 16 bits. It uses an advanced Full CMOS process technology and high speed and low power circuit technology. Thus it is suitable for high speed and low power applications, especially where battery back-up is required.

### Features

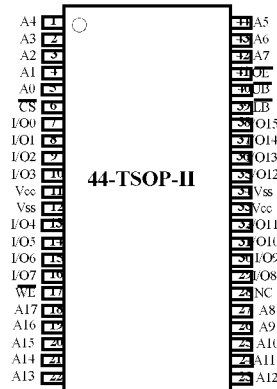
- Power Supply Voltage
  - GM76FV16256 Family : 3.0 ~ 3.6V
  - GM76FU16256 Family : 2.7 ~ 3.3V
  - GM76FS16256 Family : 2.2 ~ 2.7V
  - GM76FR16256 Family : 1.8 ~ 2.2V
- Completely Static RAM : No Clock or Timing Strobe Required
- TTL compatible inputs and outputs
- Capability of Battery Back-up Operation
- Package : 44-TSOP II

### Product Family

Product Family	Operating Temp. Range	Voltage Range	Speed	Standby Current Iccs2(LL/SL)	Operating Current(Icc1)
GM76FV16256LL/SL GM76FU16256LL/SL GM76FS16256LL/SL GM76FR16256LL/SL	Commercial ( 0 ~ 70 °C )	3.0 ~ 3.6V 2.7 ~ 3.3V 2.2 ~ 2.7V 1.8 ~ 2.2V	*55/70/85ns *55/70/85ns *85/100ns *100/120ns	20/5 uA	90mA 80mA 55mA 45mA
GM76FV16256LLI/SLI GM76FU16256LLI/SLI GM76FS16256LLI/SLI GM76FR16256LLI/SLI	Industrial (-40 ~ 85 °C )	3.0 ~ 3.6V 2.7 ~ 3.3V 2.2 ~ 2.7V 1.8 ~ 2.2V	*55/70/85ns *55/70/85ns *85/100ns *100/120ns	20/5 uA	90mA 80mA 55mA 45mA

\* The parameter is measured with 30pF test load.

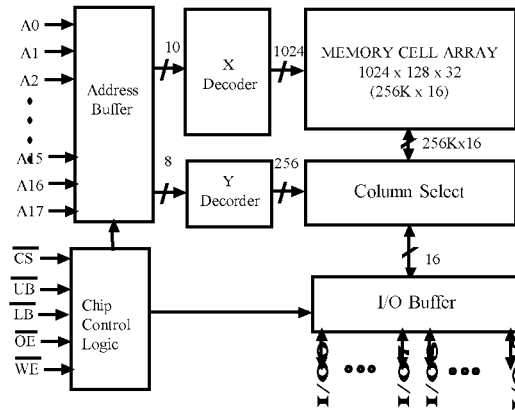
### Pin Configuration



### Pin Description

Pin	Function	Pin	Function
A0-A17	Address Inputs	$\overline{\text{LB}}$	Lower Byte(I/O0~I/O7)
$\overline{\text{WE}}$	Write Enable Input	$\overline{\text{UB}}$	Upper Byte(I/O8~I/O15)
$\overline{\text{CS}}$	Chip Select Input	Vcc	Power Supply
$\overline{\text{OE}}$	Output Enable Input	Vss	Ground
I/O0-I/O15	Data Inputs/Outputs	N.C	No Connection

### Block Diagram



**PRELIMINARY GM76FV16256,GM76FU16256,GM76FS16256,GM76FR16256**

**Absolute Maximum Ratings\***

Symbol	Parameter	Rating	Unit	
T <sub>A</sub>	Ambient Temperature under Bias	GM76FV16256 GM76FU16256 GM76FS16256 GM76FR16256	0 ~ 70	°C
		GM76FV16256-I GM76FU16256-I GM76FS16256-I GM76FR16256-I	-40 ~ 85	
T <sub>STG</sub>	Storage Temperature	-55 ~ 150	°C	
T <sub>SOL</sub>	Soldering Temperature and Time	260, 10 (at lead)	°C, S	
V <sub>CC</sub>	Supply Voltage	-0.2 ~ 4.0**	V	
V <sub>IN</sub>	Input Voltage	-0.2 ~ V <sub>CC</sub> + 0.5	V	
V <sub>IO</sub>	Input and Output Voltage	-0.2 ~ V <sub>CC</sub> + 0.5	V	
P <sub>D</sub>	Power Dissipation	1	W	

\*: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\* : Maximum V<sub>CC</sub> = -0.2 to 4.6V for GM76FV16256Family and GM76FU16256 Family

**Recommended DC Operating Conditions\***

Symbol	Parameter	Product	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	GM76FV16256 Family	3.0	3.3	3.6	V
		GM76FU16256 Family	2.7	3.0	3.3	
		GM76FS16256 Family	2.2	2.5	2.7	
		GM76FR16256 Family	1.8	2.0	2.2	
V <sub>HI</sub>	Input High Voltage	GM76FV16256 Family	2.2	-	V <sub>CC</sub> + 0.2	V
		GM76FU16256 Family	2.2			
		GM76FS16256 Family	2.0			
		GM76FR16256 Family	1.6			
V <sub>IL</sub>	Input Low Voltage	All Product	-0.2**	-	0.4	V

\* 1) Commercial Product : T<sub>a</sub> = 0 ~ 70 °C, unless otherwise specified

2) Industrial Product : T<sub>a</sub> = -40 ~ 85 °C, unless otherwise specified

\*\* V<sub>IL</sub>(min) = -1.5V for ≤ 30ns pulse

***PRELIMINARY***    **GM76FV16256,GM76FU16256,GM76FS16256,GM76FR16256**

**Truth Table**

<b>/CS</b>	<b>/OE</b>	<b>/WE</b>	<b>/LB</b>	<b>/UB</b>	<b>I/O0 ~ I/O7</b>	<b>I/O8 ~ I/O15</b>	<b>Vcc Current</b>
H	X	X	X	X	Not Selected	Not Selected	Iccs1, Iccs2
L	L	H	L	L	Read	Read	Icc, Icc1, Icc2
			L	H	Read	High - Z	Icc, Icc1, Icc2
			H	L	High - Z	Read	Icc, Icc1, Icc2
L	X	L	L	L	Write	Write	Icc, Icc1, Icc2
			L	H	Write	Not Write/High - Z	Icc, Icc1, Icc2
			H	L	Not Write/High - Z	Write	Icc, Icc1, Icc2
L	H	H	X	X	High - Z	High - Z	Icc, Icc1, Icc2
L	X	X	H	H	High - Z	High - Z	Icc, Icc1, Icc2

\*Note: X means don't care

**Capacitance** (f = 1MHz, T<sub>A</sub> = 25°C)

<b>Symbol</b>	<b>Parameter</b>	<b>Test Conditions</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V	-	8	pF
C <sub>IO</sub>	Output Capacitance	V <sub>O</sub> = 0V	-	10	pF

\*Note: This parameter is sampled and not 100% tested.

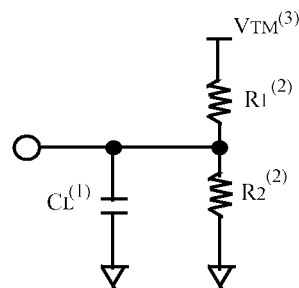
**DC Operating Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$I_{I(L)}$	Input Leakage Current	$V_{IN} = 0$ to $V_{CC}$	-1	-	1	$\mu A$	
$I_{O(L)}$	Output Leakage Current	$\overline{CS} = V_{IH}$ $OE = V_{IH}, V_{SS} \leq V_{OUT} \leq V_{CC}$	-1	-	1	$\mu A$	
$V_{OH}$	High Level Output Voltage	$I_{OH} = -1.0mA$ at $V_{CC}=3.0/3.3V$ $I_{OH} = -0.5mA$ at $V_{CC}=2.5V$ $I_{OH} = -0.44mA$ at $V_{CC}=2.0V$	2.4 2.0 1.6	-	-	V	
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 2.1mA$ at $V_{CC}=3.0/3.3V$ $I_{OL} = 0.5mA$ at $V_{CC}=2.5V$ $I_{OL} = 0.33mA$ at $V_{CC}=2.0V$	-	-	0.4	V	
$I_{CC}$	Operating Supply Current	$\overline{CS} = V_{IL}$ , $V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0mA$	-	-	20	mA	
$I_{CC1}$	Average Operating Current	$\overline{CS} = V_{IL}$ $V_{IN} = V_{IH}/V_{IL}$ , $I_{OUT} = 0mA$ tcycle = Min, cycle	$V_{CC}=3.3V@55ns$	-	-	90	mA
			$V_{CC}=3.0V@55ns$	-	-	80	
			$V_{CC}=2.5V@85ns$	-	-	55	
			$V_{CC}=2.0V@100ns$	-	-	45	
$I_{CC2}$		$\overline{CS} = 0.2V$ , $V_{IN} = V_{CC} - 0.2V/0.2V$ $I_{OUT} = 0mA, t_{cycle} = 1\mu s$	-	-	20	mA	
$I_{CCS1}$	Standby Current(TTL)	$\overline{CS} = V_{IH}$	-	-	0.5	mA	
$I_{CCS2}$	Standby Current(CMOS)	$\overline{CS} = V_{CC}-0.2V$	SL	-	-	5	$\mu A$
			LL	-	-	20	

**AC Operating Characteristics**

**Test Conditions**

Parameter	Value			
	$V_{CC}$	3.0,3.3V	2.5V	2.0V
Input Pulse Level		0.4 to 2.2V		0.4 to 1.8V
Input Rise and Fall Time		5ns		
Input and Output Timing Reference Levels		1.5V	1.1V	0.9V
Output Load		$C_L = 30pF(100 pF)$ + 1TTL Load		



- (1) Including Scope and Jig Capacitance
- (2)  $R_1 = 3070\Omega$ ,  $R_2 = 3150\Omega$
- (3)  $V_{TM} = 2.8V$  for  $V_{CC} = 3.0/3.3V$   
 $= 2.3V$  for  $V_{CC} = 2.5V$   
 $= 1.8V$  for  $V_{CC} = 2.0V$

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**AC Operating Characteristics**

**Read Cycle**

(Commercial Product : Ta = 0 ~ 70°C, Industrial Product : Ta = -40 ~ 85°C )

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>RC</sub>	Read cycle time	55	-	70	-	85	-	ns
t <sub>AA</sub>	Address access time	-	55	-	70	-	85	ns
t <sub>CO</sub>	Chip select access time ( $\overline{CS}$ )	-	55	-	70	-	85	ns
t <sub>BA</sub>	Byte enable access time ( $\overline{UB}$ , $\overline{LB}$ )	-	30	-	35	-	45	ns
t <sub>OE</sub>	Output enable access time ( $\overline{OE}$ )	-	30	-	35	-	45	ns
t <sub>CLZ</sub>	Chip select to low - Z output ( $\overline{CS}$ )	5	-	5	-	10	-	ns
t <sub>OLZ</sub>	Output enable to low - Z output ( $\overline{OE}$ )	5	-	5	-	5	-	ns
t <sub>BLZ</sub>	Byte enable to low - Z output ( $\overline{UB}$ , $\overline{LB}$ )	5	-	5	-	5	-	ns
t <sub>CHIZ</sub>	Chip select to high - Z output ( $\overline{CS}$ )	0	20	0	25	0	30	ns
t <sub>OHI</sub>	Output enable to high -Z output ( $\overline{OE}$ )	0	20	0	25	0	30	ns
t <sub>BHIZ</sub>	Byte enable to high - Z output ( $\overline{UB}$ , $\overline{LB}$ )	0	20	0	25	0	30	ns
t <sub>OH</sub>	Output hold time	5	-	10	-	10	-	ns

**Write Cycle**

Symbol	Parameter	55ns		70ns		85ns		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	55	-	70	-	85	-	ns
t <sub>CW</sub>	Chip select to end of write	50	-	65	-	75	-	ns
t <sub>BW</sub>	Byte enable to end of write	50	-	60	-	70	-	ns
t <sub>AW</sub>	Address valid to end of write	50	-	60	-	70	-	ns
t <sub>AS</sub>	Address setup time	0	-	0	-	0	-	ns
t <sub>WP</sub>	Write pulse width	45	-	50	-	60	-	ns
t <sub>WR</sub>	Write recovery time	0	-	0	-	0	-	ns
t <sub>DW</sub>	Data to write time overlap	25	-	30	-	35	-	ns
t <sub>DH</sub>	Data hold from write time	0	-	0	-	0	-	ns
t <sub>WIIZ</sub>	Write to output in high - Z	0	20	0	25	0	30	ns
t <sub>OW</sub>	Output active from end of write	5	-	5	-	5	-	ns

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**AC Operating Characteristics**

**Read Cycle**

(Commercial Product :Ta = 0 ~ 70°C, Industrial Product : Ta = -40 ~ 85°C )

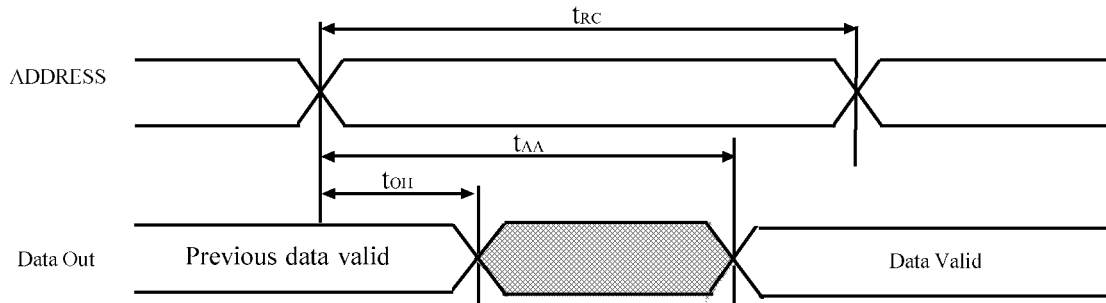
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t <sub>RC</sub>	Read cycle time	100	-	120	-	ns
t <sub>AA</sub>	Address access time	-	100	-	120	ns
t <sub>CO</sub>	Chip select access time ( $\overline{CS}$ )	-	100	-	120	ns
t <sub>BA</sub>	Byte enable access time ( $\overline{UB}$ , $\overline{LB}$ )	-	50	-	60	ns
t <sub>OE</sub>	Output enable access time ( $\overline{OE}$ )	-	50	-	60	ns
t <sub>CLZ</sub>	Chip select to low - Z output ( $\overline{CS}$ )	10	-	20	-	ns
t <sub>OLZ</sub>	Output enable to low - Z output ( $\overline{OE}$ )	5	-	5	-	ns
t <sub>BLZ</sub>	Byte enable to low - Z output ( $\overline{UB}$ , $\overline{LB}$ )	5	-	5	-	ns
t <sub>CHIZ</sub>	Chip select to high - Z output ( $\overline{CS}$ )	0	35	0	35	ns
t <sub>OIZ</sub>	Output enable to high -Z output ( $\overline{OE}$ )	0	35	0	35	ns
t <sub>BIZ</sub>	Byte enable to high - Z output ( $\overline{UB}$ , $\overline{LB}$ )	0	35	0	35	ns
t <sub>OH</sub>	Output hold time	10	-	15	-	ns

**Write Cycle**

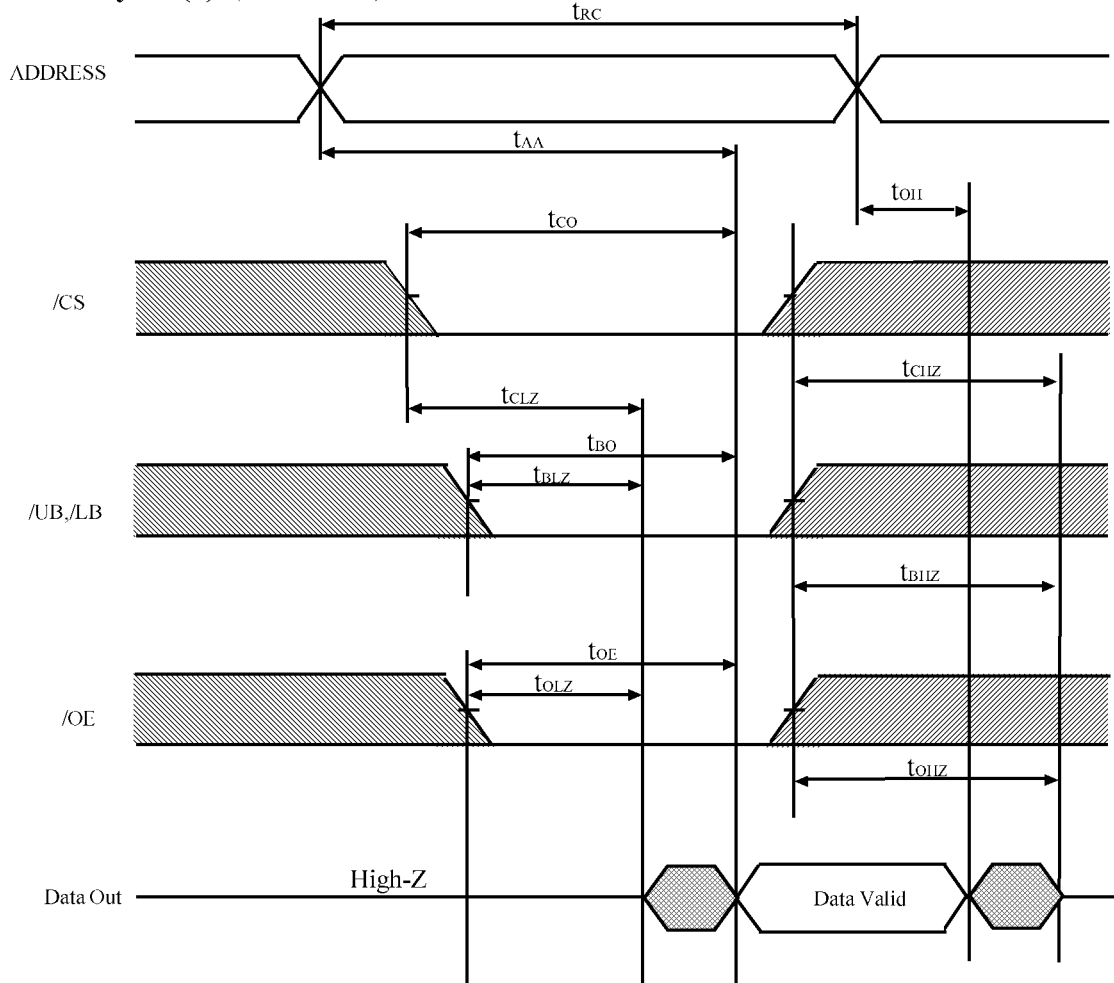
Symbol	Parameter	100ns		120ns		Unit
		Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	100	-	120	-	ns
t <sub>CW</sub>	Chip select to end of write	85	-	100	-	ns
t <sub>BW</sub>	Byte enable to end of write	80	-	90	-	ns
t <sub>AW</sub>	Address valid to end of write	80	-	90	-	ns
t <sub>AS</sub>	Address setup time	0	-	0	-	ns
t <sub>WP</sub>	Write pulse width	70	-	80	-	ns
t <sub>WR</sub>	Write recovery time	0	-	0	-	ns
t <sub>DW</sub>	Data to write time overlap	40	-	50	-	ns
t <sub>DH</sub>	Data hold from write time	0	-	0	-	ns
t <sub>WIZ</sub>	Write to output in high - Z	0	40	0	40	ns
t <sub>OW</sub>	Output active from end of write	10	-	10	-	ns

**Timing Waveforms**

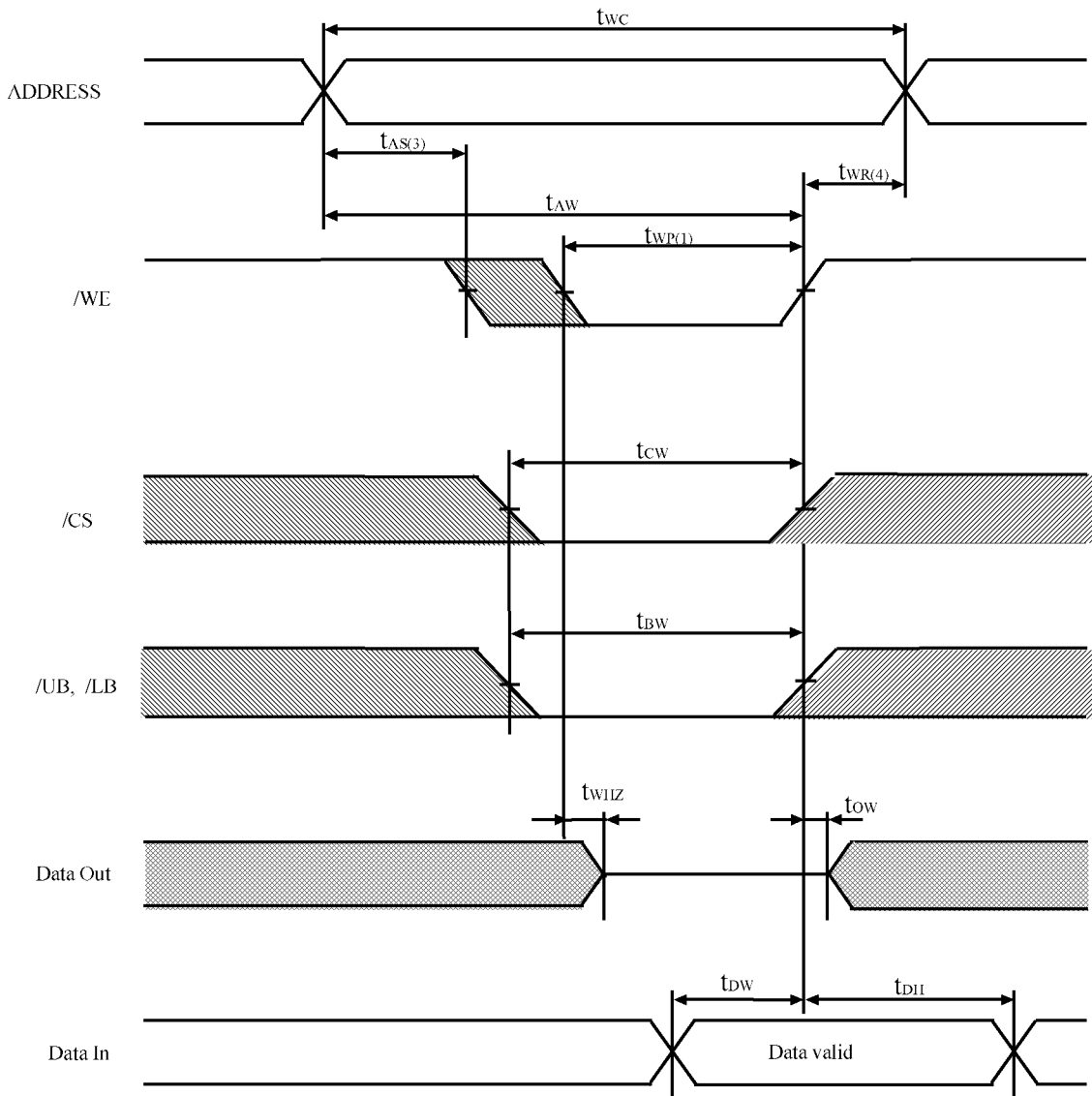
**Read Cycle (1)** ( $/CS = /OE = V_{IL}$ ,  $/WE = V_{IH}$ ,  $/UB$  and, or  $/LB = V_{IL}$ )



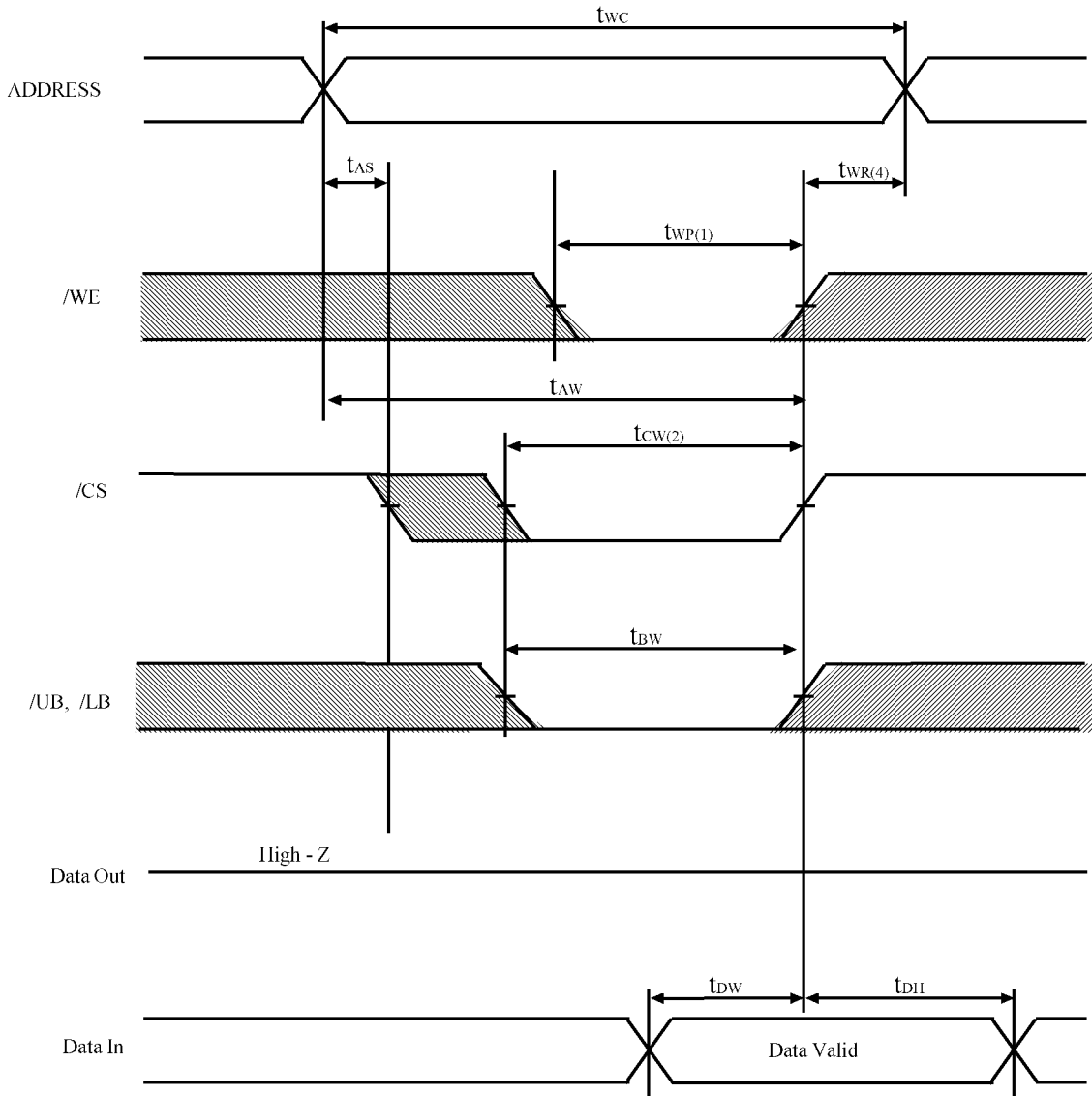
**Read Cycle (2)** ( $/WE = V_{IH}$ )



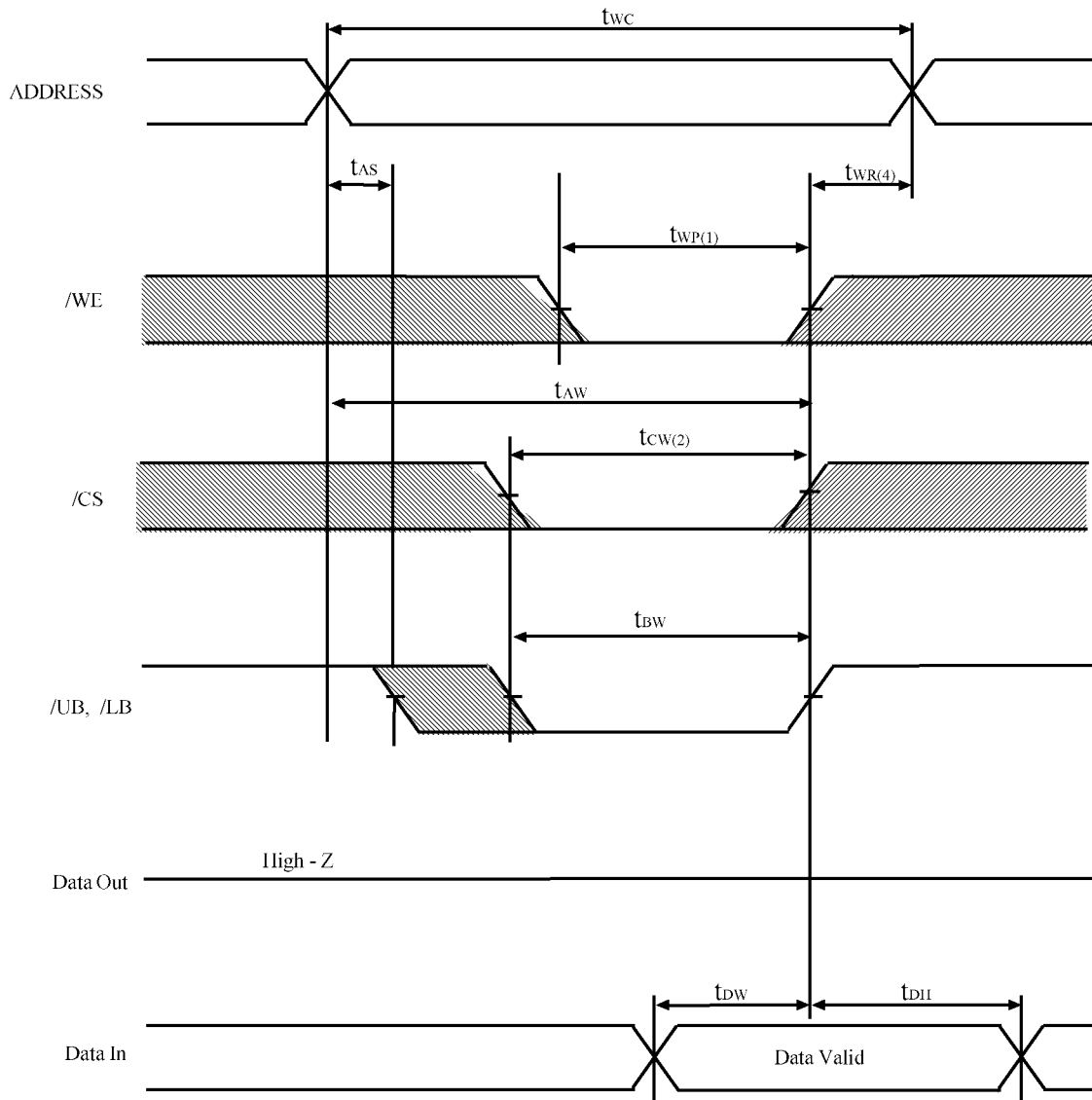
**Write Cycle (1) (/WE Controlled)**



**Write Cycle (2) (/CS Controlled)**



**Write Cycle (3) (/UB, /LB Controlled)**



**Notes(Write Cycle):**

1. A write occurs during the overlap( $t_{WP}$ ) of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low : A write end at the earliest transition among /CS going high and /WE going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of /CS going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as /CS, or /WE, or /UB, or /LB going high.

**Data Retention Characteristics**

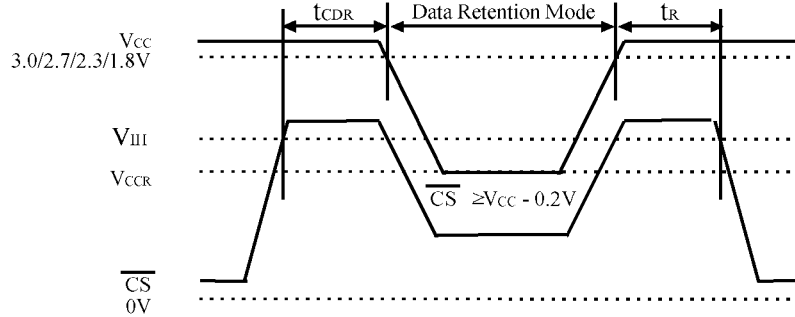
Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CCR</sub>	Data Retention Supply Voltage		1.5	-	3.6	V
I <sub>CCR</sub>	Data Retention Current	V <sub>CC</sub> =3.0V	-	1	5	μA
			-	1	20	
t <sub>CDR</sub>	Chip Select to Data Retention Time		0			ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC(2)</sub>			ns

(1) Test Condition

- Commercial Product : Ta = 0 ~ 70 °C
- Industrial Product : Ta = -40 ~ 85 °C

(2) t<sub>RC</sub> = Read cycle time

**• Data Retention Timing Diagram**



**Package Dimensions**

**44 TSOP-II**

