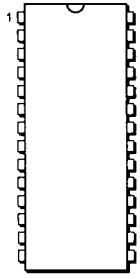
FEATURES

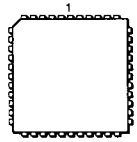
- ☐ Supports 32,768 colors (HiCOLOR-15™)
- ☐ Supports Pseudo Color format (256 colors)
- ☐ Anti-aliasing capability
- ☐ Maintains color integrity when multiple windows are displayed
- ☐ Up to 110 MHz Pipelined Operation
- ☐ Triple 6-bit or 8-bit D/A Converters
- ☐ Analog Output Comparators
- ☐ On-chip Reference
- ☐ Anti-Sparkle Circuitry
- ☐ Standard Microprocessor Interface
- ☐ 256 x 24 Color Lookup Table
- ☐ 15 Overlay Registers (SC11482/SC11484/SC12482/SC12484)
- ☐ RS-343A/RS-170 Compatible Outputs
- ☐ Sync on all Three Channels (SC11482/SC11484/SC12482/SC12484)
- ☐ Programmable Pedestal (SC11482/SC11484/SC12482/SC12484)
- ☐ +5V CMOS Monolithic (EPI) Construction
- ☐ Available Clock Rates for Pseudo Color
  - 110 MHz • 66 MHz
  - 80 MHz
- ☐ Power-on-reset for the command register.

28-PIN DIP PACKAGE



SC11483CN

44-PIN PLCC PACKAGE



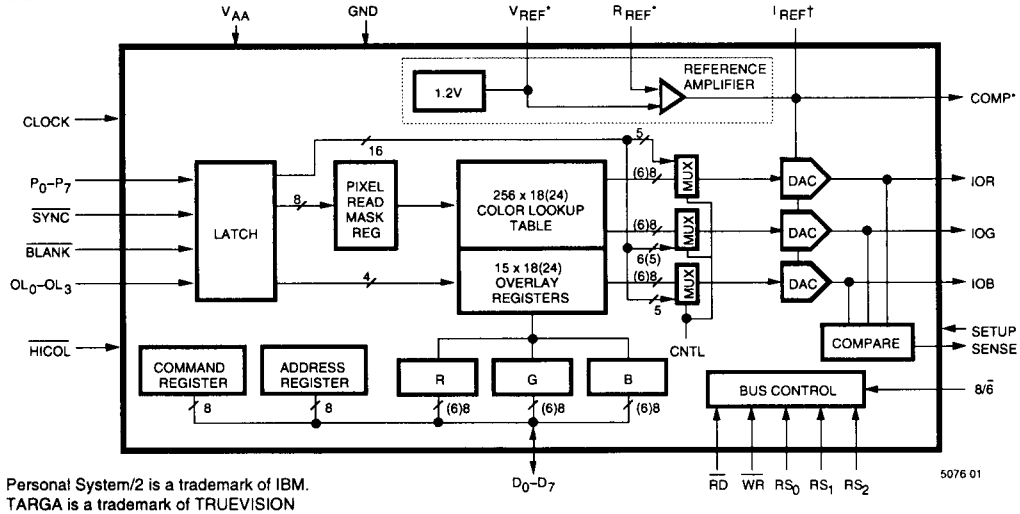
SC11482CV SC12482CV
SC11483CV SC12483CV
SC11484CV SC12484CV

GENERAL DESCRIPTION

The SC11482/SC11483/SC11484/SC12482/SC12483/SC12484 is a family of 15-bit HiCOLOR palettes that supports the popular HiCOLOR™ format which uses 5 bits of data per primary color (32,768 colors). The SC11482/SC11483/SC11484/SC12482/SC12483/SC12484 palette offers the capability of the expensive TARGA board and provides access to the wide variety of software packages (once dedicated to TARGA boards only) to the low cost VGA market. The SC11482/SC11483/SC11484/SC12482/SC12483/SC12484 also support 8 bit pseudo color (256 colors) mode.

The HiCOLOR-15 palette also provides the ability to maintain color integrity in PC-windowing applications, when more than one application window is displayed with different images simultaneously.

BLOCK DIAGRAM



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TARGA is a trademark of TRUEVISION

*Voltage reference circuitry and associated pins are available only on the SC11482/SC11483/SC11484.
†Current reference circuitry and associated pins are available only on the SC12482/SC12483/SC12484.

Also supported is anti-aliasing capability—a technique which can significantly improve the graphics quality by smoothing jagged edges. This technique requires a large number of different colors and can be easily implemented with the large number of colors offered by HiCOLOR-15 palettes.

The top-of-the-line product in this family is the SC11484/SC12484 which offers three 8-bit D/A converters, 256 x 24 color lookup table, and 15 overlay registers. It may be configured for either 6 bits or 8 bits per color operation in the 256 color mode. The SC11482/SC12482 is the same as the SC11484/SC12484 except that it offers three 6-bit D/A converters instead of 8-bit, and a 256 x 18 lookup table.

In Pseudo Color mode the SC11484/SC12484 and SC11482/SC12482 include 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Sync generation on all three channels, a programmable pedestal (0 or 7.5 IRE), and use of either an external voltage or current reference is also supported.

The SC11483/SC12483 is similar to the SC11482/SC12482, but has no overlays or sync information on the analog outputs.

On-chip analog comparators are included to simplify diagnostics and debugging, with the resulting output onto the SENSE pin. Also included is an on-chip voltage or current reference to simplify using the device.

The palettes operate in a Pseudo Color mode when HiCOLOR mode is not activated.

The HiCOLOR-15 palette generates RS-343A compatible red, green, and blue video signals, are capable of driving doubly-terminated 75Ω coax directly, and generate RS-170 compatible video signals into a singly-terminated 75Ω load, without requiring external buffering.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER			DESCRIPTION
	SC11482 SC11484 SC12482 SC12484	SC11483	SC11483 SC12483	
	PLCC	DIP	PLCC	
8/$\overline{6}$	2*			8-bit/$\overline{6}$-bit select input (TTL compatible). This bit specifies whether the microprocessor is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D_7 is the most significant data bit during color read/write cycles. For 6-bit operation, D_5 is the most significant bit during color read/write cycles (D_6 and D_7 are ignored during color write cycles and logical zero during color read cycles). This bit is implemented only on the SC11484/SC12484.
$\overline{\text{BLANK}}$	7	16	7	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 5 and 6. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored.
CLOCK	40	13	40	Clock input (TTL compatible). The rising edge of CLOCK latches the P_0–P_7, OL_0–OL_3, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
COMP	29		29	Compensation pin. A 0.1 µF ceramic capacitor must always be used to bypass this pin to V_{AA}. The COMP capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum. (Not connected for SC12482/SC12483/SC12484.)
D_0–D_7	8–15	17–24	8–15	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D_0 is the least significant bit.
GND	3, 24	14	3, 24	Ground. All GND pins must be connected.
$\overline{\text{HICOL}}$	20		20	HiCOLOR Mode select input (TTL compatible). This signal is inverted and logical ORed with D_7 of the command register. A logic zero will enable the HiCOLOR mode (either the HiCOLOR mode 1 or the HiCOLOR mode 2) selected by the D_5 bit of the command register. See Table 2 for details. The $\overline{\text{HICOL}}$ pin should be tied to V_{AA} to disable hardware selection of the HiCOLOR mode.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER SC11482 SC11484 SC12482 SC12484 PLCC	PIN NUMBER SC11483 DIP	PIN NUMBER SC11483 SC12483 PLCC	DESCRIPTION
IOR, IOG, IOB	25–27	1–3	25–27	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75 Ω coaxial cable.
R_{REF}	28			Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current. When using an external voltage reference (Figures 3 and 4), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is: RSET (Ω) = K • 1000 • V_{REF} (V)/I_{OUT} (mA) K is defined in the table below for doubly-terminated 75 Ω loads.
I_{REF}	—	4	28	When using an external current reference (Figures 5 and 6) the relationship between I_{REF} and the full scale output current on each output is: I_{REF} (mA) = I_{OUT} (mA)/K (SC12482/SC12483/SC12484 only) Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current. K is defined in the table below for doubly-terminated 75 Ω loads.
N/C	30		2, 5,19, 23, 30, 41-44	Not Connected. Pins 2, 5, 19, 23, 30, 41–44 are recommended to be tied to ground.
OL_0–OL_3	41–44			Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 4. When accessing the overlay register, the P_0–P_7 inputs are ignored. They are latched on the rising edge of CLOCK. OL_0 is the LSB.
P_0–P_7	32–39	5–12	32–39	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color lookup table is to be used to provide color information. They are latched on the rising edge of CLOCK in Pseudo-color mode and HiCOLOR mode 2. They will be latched on both the rising and falling edges of CLOCK in the HiCOLOR mode 1. P_0 is the LSB. Unused inputs should be connected to GND.
$\overline{RD}$	6	15	6	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS_0–RS_2 are latched on the falling edge of $\overline{RD}$ during microprocessor read operations.
RS_0–RS_2	17–19	26, 27†	17, 18†	Register select inputs (TTL compatible). RS_0–RS_2 specify the type of read or write operation being performed, as illustrated in Tables 2 and 3.

Part Number	Mode	Pedestal	K
SC11484/SC12484	6-bit	7.5 IRE	3.170
	8-bit	7.5 IRE	3.195
	6-bit	0.0 IRE	3.000
	8-bit	0.0 IRE	3.025
SC11482/SC12482	6-bit	7.5 IRE	3.170
		0.0 IRE	3.000
SC11483/SC12483	6-bit	0.0 IRE	2.100

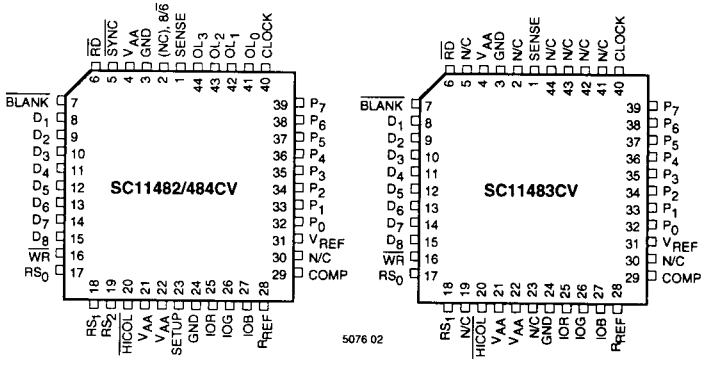
3

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER			DESCRIPTION
	SC11482 SC11484 SC12482 SC12484	SC11483	SC11483 SC12483	
	PLCC	DIP	PLCC	
SENSE	1		1	Sense output (TTL compatible). SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that SENSE may not be stable while SYNC is toggling.
SETUP	23			Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{SYNC}$	5			Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1 and 2). $\overline{SYNC}$ does not override any other control or data input, as shown in Tables 5 and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
V_{AA}	4,21,22	28	4, 21, 22	Analog power. All V_{AA} pins must be connected.
V_{REF}	31		31	Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. If an internal voltage reference is used (Figure 4), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must be used to decouple this input to V_{AA}, as shown in Figures 3 and 4. The decoupling capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum. When using internal reference this pin should not drive any external circuitry except for the decoupling capacitor.
$\overline{WR}$	16	25	16	Write control input (TTL compatible). D_0–D_7 data is latched on the rising edge of $\overline{WR}$, and RS_0–RS_2 are latched on the falling edge of $\overline{WR}$ during microprocessor write operations.

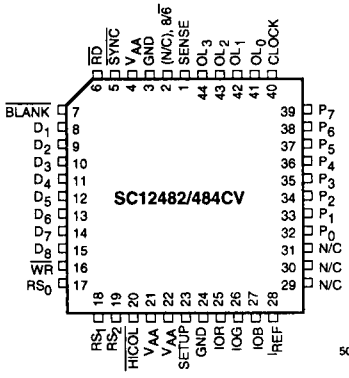
NOTE: †RS_2 is not available on the SC11483/SC12483. *$8/\overline{6}$ is only available on the SC11484/SC12484.

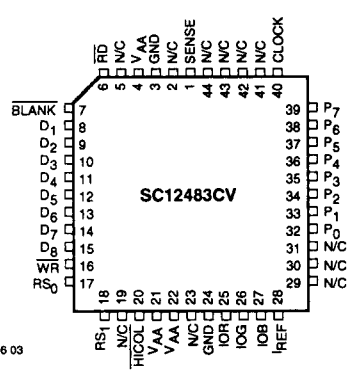
CONNECTION DIAGRAMS



NOTE: N/C pins may be left unconnected without affecting the performance of the SC11482/SC11483/SC11484/SC12482/SC12483/SC12484. N/C pins are recommended to be tied to ground. Names in parentheses are pin names for SC11482/SC12482.

CONNECTION DIAGRAMS (continued)





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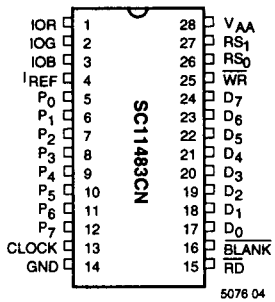

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MICROPROCESSOR INTERFACE

The HiCOLOR-15 palette family supports a standard microprocessor bus interface allowing direct access to the address register, command register, color look up table, overlay registers and pixel read mask register.

The RS_0-RS_2 register select inputs in conjunction with the state of the internal programming flag (IPF) specify the microprocessor access mode as described in Table 1. The 8-bit address register is used to access both the color look-up table and the overlay registers. Note that the IPF flag is not directly accessible by the microprocessor. The IPF flag can only by set by a special sequence described in the Command Register section.

Reading and Writing Color Lookup Table and Overlay Color Data

In order to read color data the RS_0-RS_2 inputs must be set to RAM read mode or overlay read mode. The microprocessor reads color data by loading the address of the color look up table or the overlay location being read into the address register. The color information is then copied from the location specified by the address register to the RGB register and the address register is incremented to the next location. After the microprocessor completes three successive reads (of 6 or 8 bits of each red, green and blue), the contents of the lookup table or overlay location specified by the address register is copied into the RGB register and the address register is incremented again. This feature allows a block of color data to be read by writing to the starting address and performing continuous read cycles until the entire block has been read.

In order to write color data the RS_0-RS_2 inputs must be set to RAM write mode or overlay write mode. The microprocessor writes color data the by writing the address of the color look up table or the overlay location being modified into the address register. After the microprocessor completes three successive writes (of 6 or 8 bits of each red, green and blue), the three bytes of color information are concatenated and written to the location specified by the address register. Once the location has been written, the address register is incremented to the next location to prepare for another write sequence. This feature allows a block of color data to be written by writing to the starting address and performing continuous write cycles until the entire block has been written.

The address register resets to $FF following a blue write cycle and resets to $00 following a blue read cycle when the color lookup table is accessed. When accessing the overlay registers, the address register increments after each blue read/write cycle and the four most significant bits of the address register (ADDR4-7).

The microprocessor interface access is asynchronous to the pixel clock. Data transfers between the color lookup table/overlay registers and the RGB registers occur in the period between microprocessor ac-

IPF	RS_2	RS_1	RS_0	ADDRESSED BY MICROPROCESSOR
X	0	0	0	Palette RAM write address register
X	0	1	1	Palette RAM read address register
X	0	0	1	Palette RAM
0	0	1	0	Pixel mask register
1	0	1	0	Command register
X	1	0	0	Overlay RAM write address register
X	1	1	1	Overlay RAM read address register
X	1	0	1	Overlay RAM
X	1	1	0	Command Register

Table 1. Control Input Truth Table

cesses and are synchronized by internal logic.

The address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 3, to keep track of the red, green and blue read/write cycles. During microprocessor writes these bits are reset to zero and are not reset when the microprocessor reads the address register. The microprocessor only has access to the first eight bits (ADDR0-7) of the address register which are used to address the color lookup table locations and overlay registers as shown in Table 3. ADDR0 is the least significant bit when the microprocessor is accessing the color lookup table or overlay registers. The microprocessor can read the address register at any time without altering its contents or changing the current read/write mode.

SC11482/SC11483/SC12482/ SC12483 Data Bus Interface

The lower six bits of the data bus are used to transfer color data. D_0 is the LSB and D_5 is the MSB. When reading color data D_6 and D_7 will be logic zero. D_6 and D_7 are ignored during write cycles.

SC11484/SC12484 Data Bus Interface

The 8/$\overline{6}$ input controls whether the microprocessor is reading and writing 8-bits (logic one) or 6-bits (logic zero) of color data each cycle.

During 8 bit operation D_0 is the LSB and D_7 is the MSB. During 6-bit operation the SC11484/SC12484 data bus behaves as a SC11482/SC11483/SC12482/SC12483. The full scale current output is about 1.5% lower in 6 bit mode than in 8 bit.

Color Pixel and Overlay Data Interface

The P_0-P_7 and OL_0-OL_3 inputs are used to address the color lookup table and overlay registers, as shown in Table 4. The pixel read mask register is bit-wise logically ANDed with the P_0-P_7 inputs with bit D_0 of the pixel read mask register corresponding to pixel input P_0. The addressed location provides 24-bits (18-bits for the SC11482/SC11483/SC12482/SC12483) of color information to the D/A converters. Note that the pixel read mask register is not initialized at power-on reset.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs are latched on the rising edge of CLOCK maintaining synchronization with the color data. These inputs also add weighted currents to the analog outputs to produce appropriate output levels for video applications as shown in Figures 1 and 2. Tables 4 and 5 show how $\overline{SYNC}$ and $\overline{BLANK}$ inputs affect the output levels.

The SETUP input specifies whether a 0 IRE (SETUP = GND) or a 7.5 IRE (SETUP = V_{AA}) blanking pedestal is used. The SC11483/SC12483 only generates a 0 IRE blanking pedestal as shown in Figure 2.

The analog outputs of the palette are capable of directly driving a 37.5 ohm load such as a doubly-terminated 75 ohm coaxial cable.

HiCOLOR Modes

When a HiCOLOR mode is activated, the input stage accepts 16 bits of pixel information from the 8 bit pixel select lines, P_0-P_7. The two bytes form a 16 bit pixel word (B_{15}-B_0) to directly drive the triple video DACs. The color lookup table and pixel read mask register are bypassed. The 16 bit pixel word (B_{15}-B_0) is assigned to the DACs using the following format:

HiCOLOR-15 Format	Comments
B15	Ignored
B14 - B10	Red DAC
B9 - B5	Green DAC
B4 - B0	Blue DAC

* Internally the unused LSBs of all DACs are forced to zero in HiCOLOR mode.

HiCOLOR Mode 1

In HiCOLOR mode 1 the least significant byte is latched on the rising edge of the pixel clock and the most significant byte is latched on the falling edge of the pixel clock. Therefore only one pixel clock period is needed to load a 16 bit word. See Figure 11.

HiCOLOR Mode 2

When HiCOLOR mode 2 is activated the input stage accepts 16 bits of information by using two pixel clock cycles. The least significant byte is latched on the first rising edge of the pixel clock and the most significant byte is latched on the second rising edge of the pixel clock. They are synchronized with the $\overline{BLANK}$ signal. The first byte latched when $\overline{BLANK}$ goes high is the least significant byte. Since a pixel word is latched in two pixel clock cycles the input clock must be twice as fast as the DACs data conversion clock. See Figure 8. The HiCOLOR palette has an internal divider to generate the data conversion clock from the pixel clock. See Figure 9.

SENSE Output

SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ±10% tolerance. Note that $\overline{SYNC}$ should be logical zero for SENSE to be stable.

Command Register

This register is active in all modes. It is used to set the operating mode of the device as shown in Table 2. It may be written to or read by the microprocessor at any time and is initialized to a logical zero after the power on reset.

In the SC11483/SC12483, where the RS_2 pin is not available, the command register is accessed by using the following special sequence of events:

A flag will be set when the pixel read mask register (RS_1 = 1 & RS_0 = 0) is read four times consecutively. The next write to the pixel mask register will be directed to the command register and can be used to set the command register. A write to any address or a read from any address other than the pixel read mask register will reset the flag. This flag will also get reset after the power on reset.

D_7	D_6*	D_5	D_4*	D_3*	D_2*	D_1*	D_0*	Mode
0	0	0	0	0	0	0	0	Pseudo Color (256 colors)
1	0	0	0	0	0	0	0	HiCOLOR Mode 1
1	0	1	0	0	0	0	0	HiCOLOR Mode 2

*Reserved by Sierra Semiconductor.

D_7 HiCOLOR Mode Enable. A logic zero enables the Pseudo-color mode. A logic one enables the HiCOLOR modes. (Used with D_5.)

D_6 Reserved. This pin must be set to logic zero.

D_5 HiCOLOR Mode Select. When HiCOLOR mode is enabled (D_7 = 1) a logic zero selects the HiCOLOR Mode 1. A logic one selects HiCOLOR mode 2. When HiCOLOR mode is disabled (D_7 = 0) this bit must be set to logic zero.

D_4–D_0 Reserved. These inputs must be set to logic zero.

Table 2. Command Register Modes

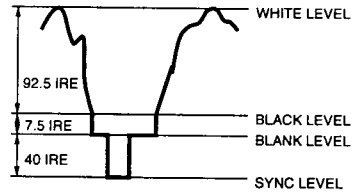
	Value	RS_2	RS_1	RS_0	Addressed by MPU
ADDRa, b (counts modulo 3)	00				Red value
	01				Green value
	10				Blue value
ADDR0–7 (counts binary)	$00-$FF	0	0	1	Color Lookup Table
	xxxx 0000	1	0	1	Reserved
	xxxx 0001	1	0	1	Overlay Color 1
	:	:	:	:	:
	xxxx 1111	1	0	1	Overlay Color 15

Table 3. Address Register (ADDR) Operation

OL_0–OL_3	P_0–P_7	Addressed by Frame Buffer
$0	$00	Color lookup table Location $00
$0	$01	Color lookup table Location $01
:	:	:
$0	$FF	Color lookup table Location $FF
$1	$xx	Overlay Color 1
:	$xx	:
$F	$xx	Overlay Color 15

Table 4. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF)

SC11482/SC11484 SC12482/SC12484 w/o SYNC		SC11482/SC12484 SC12482/SC12484 with SYNC	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

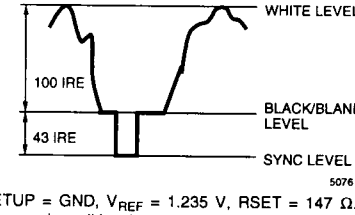
Figure 1. Composite Video Output Waveforms (SETUP = V_{AA})

Description	SC11482/SC11484 SC12482/SC12484 I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	Data + 9.05	1	1	Data
DATA–SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	$00
BLACK–SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω.

Table 5. Video Output Truth Table (SETUP = V_{AA})

SC11483/SC12483 or SC11482/SC11484/ SC12482/SC12484 w/o Sync		SC11482/SC11484 SC12482/SC12484 with Sync	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.256
0.00	0.000	0.00	0.000



NOTE: 75 Ω doubly-terminated load, SETUP = GND, V_{REF} = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms (SETUP = GND)

Description	SC11483 SC12483 I_{OUT} (mA)	SC11482/SC11484 SC12482/SC12484 I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	17.62	26.67	1	1	$FF
DATA	Data	Data + 8.05	1	1	Data
DATA–SYNC	Data	Data	0	1	Data
BLACK	0	8.05	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	0	8.05	1	0	$xx
SYNC	0	0	0	0	$xx

NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω.

Table 6. Video Output Truth Table (SETUP = GND)

PC BOARD LAYOUT CONSIDERATIONS

The layout should minimize the noise on the power and ground lines by providing good decoupling and shielding all digital inputs. In order to minimize inductive ringing the lead lengths between groups of V_{AA} and GND pins should be minimized.

Separate power and ground planes are recommended to minimize power supply noise. The ground plane should encompass all ground pins, analog output traces, power supply bypass circuitry, and all digital signal traces leading up to the HiCOLOR-15 palette.

The HiCOLOR-15 palette and any associated analog circuitry should have its own analog power plane. The analog power plane should be isolated from the PCBs digital power plane by a ferrite bead connected at a single point as shown in Figures 3, 4, and 5. The bead should be located within three inches of the HiCOLOR-15 palette.

The PCBs digital power plane should provide power to all digital logic on the board.

Ensuring that the PCB digital power and ground planes do not overlay portions of the analog power plane can reduce plane to plane noise coupling.

Supply Decoupling

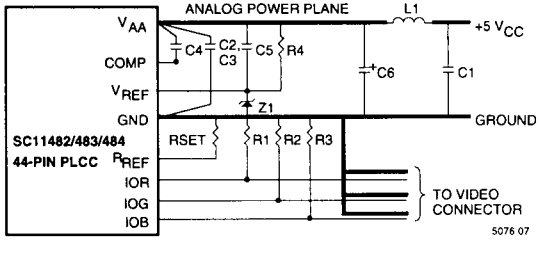
All CMOS and TTL devices on the PCB should be capacitively bypassed. Bypass capacitors should be installed with the shortest possible lead lengths to reduce lead inductance. Each of the two groups of V_{AA} pins should be decoupled to GND using a 0.1 uF ceramic capacitor placed as close as possible to the device. If a high frequency switching power supply is used a three terminal voltage regulator should be used to supply power to the analog power plane.

Digital Signal Interconnect

The digital inputs should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog power plane. Due to the high clock rates the clock lines should be minimized to reduce noise pickup. Active digital input termination resistors should be connected to the regular PCB power plane, not the analog power plane.

Analog Signal Interconnect

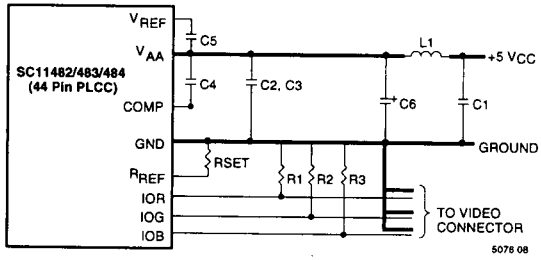
The HiCOLOR-15 palette should be located as close as possible to the output connector to minimize noise pickup. The video output signals should overlay the ground plane to maximize the power supply rejection. The analog outputs should each have a 75 ohm load resistor connected to ground as close as possible to the HiCOLOR-15 palette to minimize reflections.



LOCATION	DESCRIPTION
C1–C5	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C6	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)
Z1	1.2 V Voltage Reference (National Semiconductor LM385BZ-1.2)
R4	1K Ω 5% Resistor

NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11482/SC11483/SC11484.

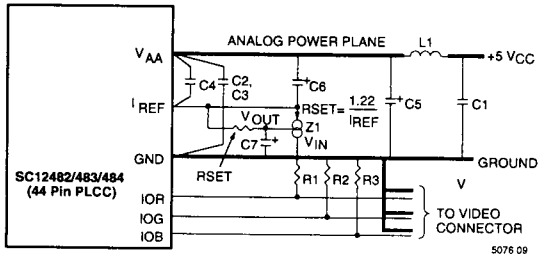
Figure 3. Typical Connection Diagram and Parts List (External Voltage Reference)



NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11482/SC11483/SC11484.

LOCATION	DESCRIPTION
C1–C5	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C6	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)

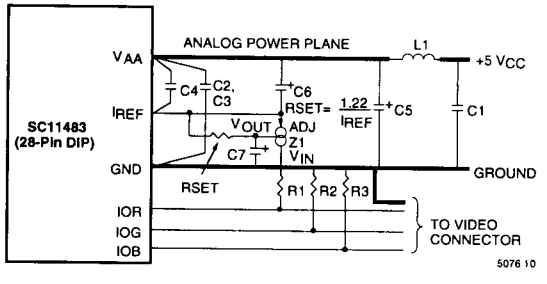
Figure 4. Typical Connection Diagram and Parts List (Internal Voltage Reference)



NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC12482/SC12483/SC12484.

LOCATION	DESCRIPTION
C1–C4	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C5	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
C6	47 µF Tantalum Capacitor (Mallory CSR13F476KM)
C7	1 µF Capacitor (Mallory CSR13G105KM)
RSET	1% Metal Film Resistor (Dale CMF-55C)
L1	Ferrite Bead (Fair-Rite 2743001111)
Z1	Adjustable Regulator (National Semiconductor LM337LZ)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)

Figure 5. Typical Connection Diagram and Parts List (External Current Reference)



NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11483.

LOCATION	DESCRIPTION
C1–C4	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C5	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
C6	47 µF Tantalum Capacitor (Mallory CSR13F476KM)
C7	1 µF Capacitor (Mallory CSR13G105KM)
L1	Ferrite Bead (Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
Z1	Adjustable Regulator (National Semiconductor LM337LZ)
RSET	1% Metal Film Resistor (Dale CMF-55C)

Figure 6. Typical Connection Diagram and Parts List (External Current Reference)

ABSOLUTE MAXIMUM RATINGS

V_{AA} (measured to GND)	+7.0 V
Voltage on Any Digital Pin	– 0.5 V to V_{AA} + 0.5 V
Analog Output Short Circuit Duration to any Power Supply or Common (ISC)	Indefinite
Ambient Operating Temperature (TA)	–55 to +125°C
Storage Temperature (TS)	–65 to +150°C
Junction Temperature (TJ)	+150°C
Vapor Phase Soldering (2 minutes) TVSOL	TBD

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNITS
Power Supply (V_{AA}) 100, 80, 66 MHz PRVTS	+4.75	5.0	5.25	V
Ambient Operating Temperature (TA)	0	25	70	°C
Output Load (RL)		37.5		Ω
Voltage Reference (V_{REF}) (SC11482/483/484 only)	+1.14	1.235	1.26	V
Current Reference (I_{REF}) (SC12482/483/484 only) Standard RS-343A PS/2 Compatible	 –3 –3	 –8.39 –8.88	 –10 –10	 mA mA

DC ELECTRICAL CHARACTERISTICS

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Resolution (each DAC)					
SC11484/SC12484		8	8	8	Bits
SC11482/SC11483/SC12482/SC12483		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	I_L				
SC11484/SC12484				±1	LSB
SC11483/SC12483				±1/2	LSB
SC11482/SC12482				±1/4	LSB
Differential Linearity Error	D_L				
SC11484/SC12484				±1	LSB
SC11483/SC12483				±1/2	LSB
SC11482/SC12482				±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} + 0.5	V
Input Low Voltage	V_{IL}	GND – 0.5		0.8	V
Input High Current (V_{IN} = 2.4 V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4 V)	I_{IL}			–1	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}			7	pF

DC ELECTRICAL CHARACTERISTICS (continued)

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SC11482/SC11484/SC12482/SC12484					
SETUP = V_{AA}		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
SC11483/SC12483		0	0	0	µA
Blank Level					
SC11482/SC11484/SC12482/SC12484		6.29	7.62	8.96	mA
SC11483/SC12483		0	5	50	µA
Sync Level (SC11482/489 only)		0	5	50	µA
LSB Size					
SC11484/SC12484 (8/$\overline{6}$ = Logical One)			69.1		µA
SC11482/SC11483/SC12482/SC12483			279.68		µA
DAC to DAC Matching			2	5	%
Output Compliance	V_{OC}	–1.0		+1.5	V
Output Impedance	RA_{OUT}		10		kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}			30	pF
Voltage Reference Input Current	IV_{REF}		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / $\%\Delta V_{AA}$

NOTE: Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, 8/$\overline{6}$ = Logical one. For 28-pin DIP version of the SC11483 and 44-pin PLCC version of the SC12482/SC12483/SC12484, I_{REF} = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

*Since the SC11482/SC11483/SC12482/SC12483 have 6-bit DACs (and the SC11484/SC12484 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

ANALOG OUTPUT LEVELS—PS/2 COMPATIBILITY

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SC11482/SC11484/SC12482/SC12484					
SETUP = V_{AA}		1.01	1.51	2.0	mA
SETUP = GND		0	5	50	µA
SC11483/SC12483		0	5	50	µA
Blank Level					
SC11482/SC11484/SC12482/SC12484		6.6	8	9.4	mA
SC11483/SC12483		0	5	50	µA
Sync Level (SC11482/SC11484/SC12482/SC12484 only)		0	5	50	µA

NOTE: Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, 8/$\overline{6}$ = Logical one. For 28-pin DIP version of the SC11483 and 44-pin PLCC version of the SC12482/SC12483/SC12484, I_{REF} = 8.88 mA.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	110 MHz Devices			80 MHz Devices			66 MHz Devices			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Clock Rate Pseudo Color	F_{MAX}			110			80			66	MHz
Clock Rate HiCOLOR Mode 1	F_{MAX}			66			50			50	MHz
Clock Rate HiCOLOR Mode 2	F_{MAX}			110			80			80	MHz
RS_0–RS_2 Setup Time	1	10			10			10			ns
RS_0–RS_2 Hold Time	2	10			10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20			20	ns
Read Data Hold Time	6	5			5			5			ns
Write Data Setup	7	10			10			10			ns
Write Data Hold Time	8	10			10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			4•P13			ns
Pixel and Control Setup Time	11	2.5			3			3			ns
Pixel and Control Hold Time (Pseudo Color and HiCOLOR Mode 2)	12	2.5			3			3			ns
Pixel and Control Setup Time LSB HiCOLOR Mode 1	20	-1.0			-1.0			-1.0			ns
Pixel and Control Hold Time LSB HiCOLOR Mode 1	21	7.0			7.0			7.0			ns
Pixel and Control Setup Time MSB HiCOLOR Mode 1	22	-1.0			-1.0			-1.0			ns
Pixel and Control Hold Time MSB HiCOLOR Mode 1	23	7.0			7.0			7.0			ns
Clock Cycle Time	13	9			12.5			15.5			ns
Clock Pulse Width High Time	14	3.5			4			5			ns
Clock Pulse Width Low Time	15	3.5			4			5			ns
Clock Cycle Time (HiCOLOR Mode 1)	13	15			20			20			ns
Clock Pulse Width High Time HiCOLOR Mode 1	14	6			8			8			ns
Clock Pulse Width Low Time HiCOLOR Mode 1	15	6			8			8			ns
Analog Output Delay	16			30			30			30	ns
Analog Output Rise/Fall Time	17		3			3			3		ns
Analog Output Settling Time*	18		13			15			20		ns
Clock and Data Feedthrough*			-30			-30			-30		dB
Glitch Impulse*			75			75			75		pV–sec
DAC to DAC Crosstalk			-23			-23			-23		dB
Analog Output Skew				2			2			2	ns
SENSE Output Delay	19		1			1			1		µs
Pipeline Delay (Pseudo Color and HiCOLOR Mode 1 and Mode 2)		4		8	4		8	4		8	Clocks
V_{AA} Supply Current**	I_{AA}		180	220		180	220		180	220	mA

TEST CONDITIONS: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, 8/$\overline{6}$ = Logical one. For 28-pin DIP version of SC11483 and 44-pin PLCC version of the SC12482/SC12483/SC12484, I_{REF} = -8.39 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D_0–D7 output load ≤ 50 pF. See timing notes in Figures 7 and 8.

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

** At F_{MAX}, I_{AA} (typ) at V_{AA} = 5.0 V. I_{AA} (max) at V_{AA} = 5.25 V.

TIMING WAVEFORMS

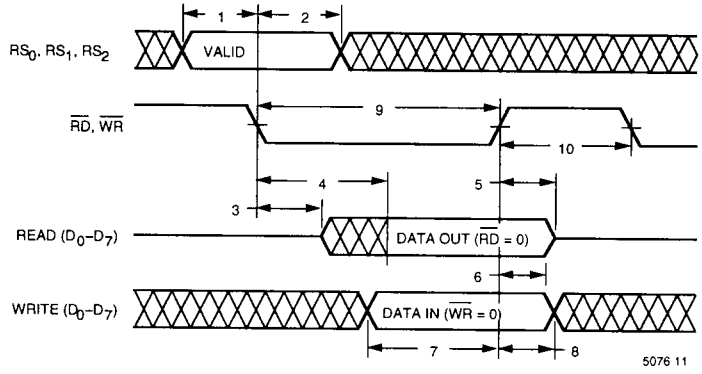


Figure 7. MPU Read/Write Timing

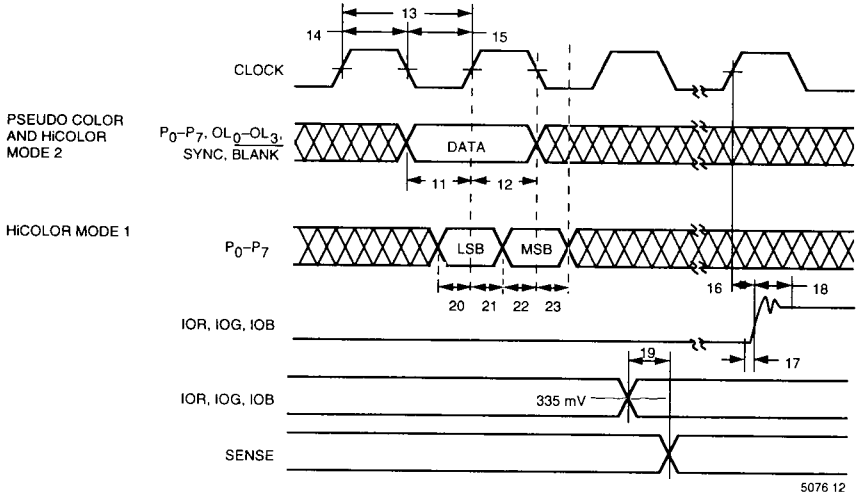


Figure 8. Video Input/Output Timing

NOTE 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

NOTE 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB. (SC11484/SC12484), ± 1/4 LSB (SC11482/SC12482), or ± 1/2 LSB (SC11483/SC12483).

NOTE 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

TIMING WAVEFORMS (continued)

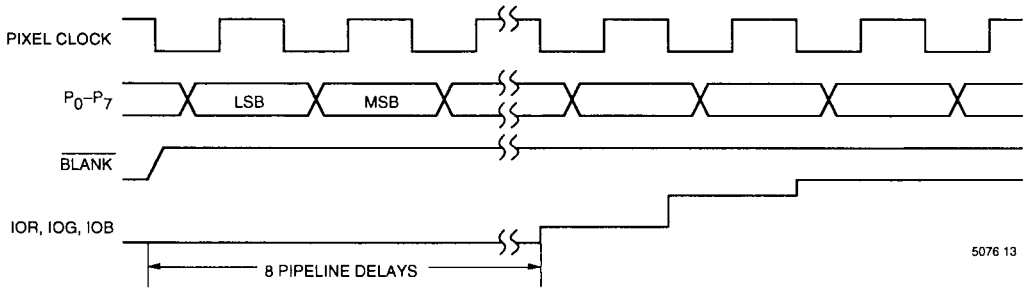


Figure 9. HiCOLOR Mode 2 Timing

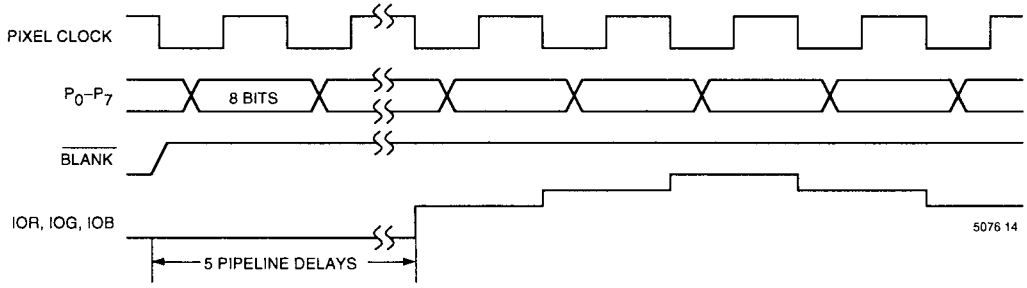


Figure 10. Pseudo Color Mode Timing

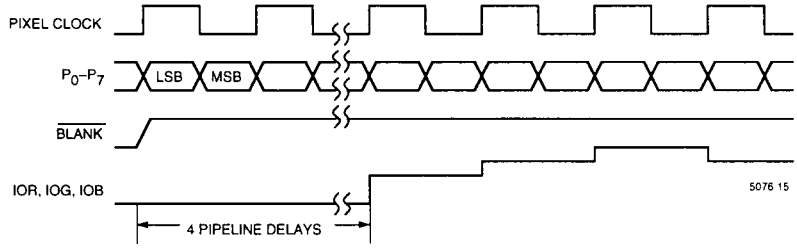


Figure 11. HiCOLOR Mode 1 Timing

ORDERING INFORMATION

PART NO.	Color Lookup Table	Ref. Type	Overlay Registers	SYNC. GEN.	PIXEL CLOCK (MAX) PSEUDO COLOR	PIXEL CLOCK (MAX) HiCOLOR Mode 1	PIXEL CLOCK (MAX) HiCOLOR Mode 2	PACKAGE	AMBIENT TEMP. RANGE
SC11482CV-110	256 x 18	V_{REF}	15 x 18	yes	110 MHz	66 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11482CV-80	256 x 18	V_{REF}	15 x 18	yes	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11482CV-66	256 x 18	V_{REF}	15 x 18	yes	66 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CV-110	256 x 18	V_{REF}	—	no	110 MHz	66 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CV-80	256 x 18	V_{REF}	—	no	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CV-66	256 x 18	V_{REF}	—	no	66 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CN-80	256 x 18	I_{REF}	—	no	80 MHz	50 MHz	80 MHz	28-pin 0.6" Plastic DIP	0° to +70°C
SC11483CN-66	256 x 18	I_{REF}	—	no	66 MHz	50 MHz	80 MHz	28-pin 0.6" Plastic DIP	0° to +70°C
SC11484CV-110	256 x 24	V_{REF}	15 x 24	yes	110 MHz	66 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11484CV-80	256 x 24	V_{REF}	15 x 24	yes	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11484CV-66	256 x 24	V_{REF}	15 x 24	yes	66 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12482CV-110	256 x 18	I_{REF}	15 x 18	yes	110 MHz	66 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12482CV-80	256 x 18	I_{REF}	15 x 18	yes	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12482CV-66	256 x 18	I_{REF}	15 x 18	yes	66 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12483CV-110	256 x 18	I_{REF}	—	no	110 MHz	66 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12483CV-80	256 x 18	I_{REF}	—	no	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12483CV-66	256 x 18	I_{REF}	—	no	66 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12484CV-110	256 x 24	I_{REF}	15 x 24	yes	110 MHz	66 MHz	110 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12484CV-80	256 x 24	I_{REF}	15 x 24	yes	80 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C
SC12484CV-66	256 x 24	I_{REF}	15 x 24	yes	66 MHz	50 MHz	80 MHz	44-pin Plastic J-Lead	0° to +70°C