MOTOROLA

4-Wide 4-3-3-3 Input "OR-AND" Gate

Military 10H519

ELECTRICALLY TESTED PER:
5962-8772801

The 10H519 is a 4-wide 4-3-3-3 input **OR/AND** gate with one input from two gates common to pin 10.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

2

- Propagation Delay, 1.0 ns Typical
- 160 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8772801
3) 883: 10H519/BXAJC
X = CASE OUTLINE AS FOLLOWS:

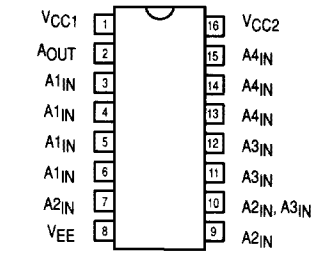
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

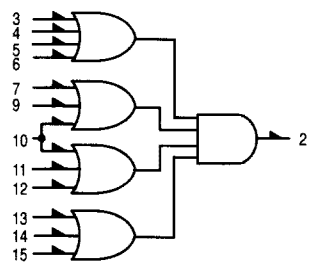
PIN ASSIGNMENTS

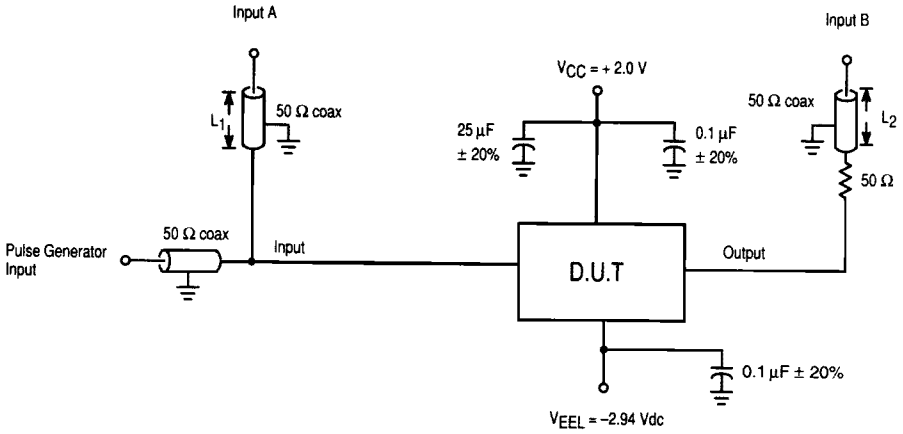
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$A1_{IN}$	3	7	4	GND
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A1_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$	9	13	12	OPEN
$A2_{IN}$, $A3_{IN}$	10	14	13	GND
$A3_{IN}$	11	15	14	OPEN
$A3_{IN}$	12	16	15	OPEN
$A4_{IN}$	13	1	17	OPEN
$A4_{IN}$	14	2	18	OPEN
$A4_{IN}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. All other outputs loaded 100 Ω to GND.
2. $L_1 = L_2$: Matched for equal time delays.
3. $P_W \geq 20$ ns.
4. P_{RF} = 1.0 MHz.
5. $t_r = t_f$ = 1.0 ns ± 0.1 ns.

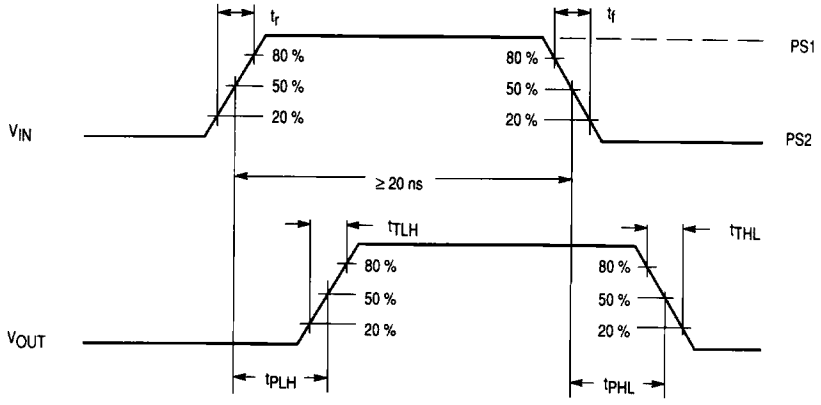


Figure 1. Switching Test Circuit and Waveforms

10H519
QUIESCENT LIMIT TABLE*

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	3 – 7 9 – 15				8		1, 16	2
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	3, 7, 10 11, 13	3 – 7 9 – 15			8		1, 16	2
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	3 – 7 9 – 15	3 – 7 9 – 15	3 – 7 9 – 15		8	8	1, 16	2
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	3 – 7 9 – 15	3 – 7 9 – 15		3 – 7 9 – 15	8	8	1, 16	2
I_{EE}	Power Supply Current	–26		–29		–29		mA					8		1, 16	8
I_{IH}	Input Current High		295		500		500	µA	3 – 7 9 – 15				8		1, 16	3 – 7 9 – 15
I_{IH1}	Input Current High		360		610		610	µA	10				8		1, 16	10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 – 7 9 – 15				8	1, 16	3 – 7 9 – 15

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Test Temperature	Test Voltage Values (Volts)								
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T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T
t_{TLH}	Rise Time	0.8	2.0	0.8	2.3	0.8	1.9	ns	10	2	1, 16	8	4, 14	2
t_{THL}	Fall Time	0.8	2.0	0.8	2.3	0.8	1.9	ns	10	2	1, 16	8	4, 14	2
t_{PLH}	Propagation Delay Pin 10	0.75	2.25	0.8	2.55	0.75	2.2	ns	4	2	1. 16	8	7, 12, 13	2
t_{PHL}	Propagation Delay Pin 10	0.75	2.25	0.8	2.55	0.75	2.2	ns	4	2	1. 16	8	7, 12, 13	2
t_{PHL}	Propagation Delay Exclude Pin 10	0.75	2.5	0.8	2.8	0.75	2.4	ns	4	2	1. 16	8	7, 12, 13	2
t_{PLH}	Propagation Delay Exclude Pin 10	0.75	2.5	0.8	2.8	0.75	2.4	ns	4	2	1. 16	8	7, 12, 13	2