

## Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

# Bt461

# Bt462

**170 MHz**  
**Monolithic CMOS**  
**1K x 8 Color Palette**  
**RAMDAC™**

## Distinguishing Features

- 170/160, 135, 110, 80 MHz Operation
- 3:1, 4:1, or 5:1 Pixel Input Muxing
- Single 8-bit D/A Converter
- 1024 x 8 Primary Color Palette RAM
- 256 x 8 Alternate Color Palette RAM
- 32 x 8 Overlay Color Palette RAM
- RS-343A-Compatible Output
- Pixel Panning Support
- Programmable Setup (0 or 7.5 IRE)
- Bit Plane Read and Blink Masks
- Two Load Color Palette Modes
- Standard MPU Interface
- 132-pin PGA or PQFP Package

## Applications

- High-Resolution Color Graphics
- True-Color Graphics Systems
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

## Related Products

- Bt431, Bt438, Bt439
- Bt459, Bt460, Bt468

## Product Description

The Bt461/462 single-channel RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL-compatible interface (up to 45 MHz) to the frame buffer, while maintaining the 170 MHz video data rates required for sophisticated color graphics.

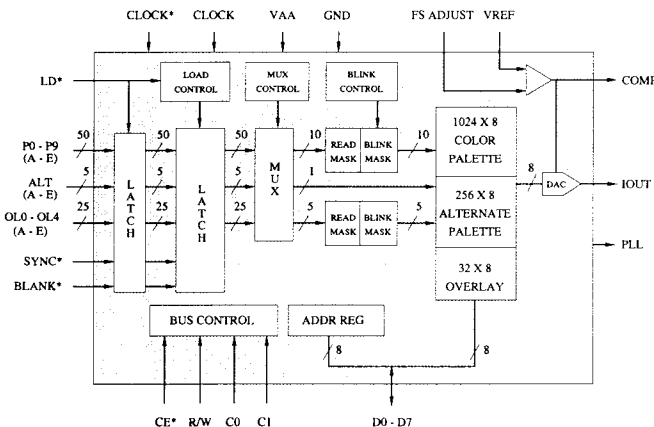
On-chip features include a 1024 x 8 dual-port color palette RAM; a 256 x 8 dual-port alternate color palette RAM; 32 x 8 overlay color palette RAM; programmable 3:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports; bit plane masking and blinking; programmable setup (0 or 7.5 IRE); and pixel panning support.

The Bt462 also supports an optional underlay mode. Only 15 overlays are available when the underlay is used.

Color data may be written to and read from the Bt461/462 by the MPU each cycle, or during red, green, and blue cycles. The MPU interface operates asynchronously to the pixel data, simplifying system design.

The PLL current output enables the synchronization of multiple Bt461/462s with subpixel resolution.

## Functional Block Diagram



**Circuit Description**

**MPU Interface**

As illustrated in the functional block diagram, the Bt461/462 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As presented in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 10-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

The two modes in which the MPU reads and writes color data to the device, as controlled by command register\_0, are as follows: The first mode (normal mode), loads color data into the device each write cycle, and outputs color data from the device each read cycle. The second mode (RGB mode) loads color data into the device in red, green, and blue write cycles, and outputs data from the device using red, green, blue read cycles. The device is configured to respond only to the color cycle specified by the command register.

**Reading/Writing Color Data (Normal Mode)**

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or the overlay palette RAM. The address register then increments to the next location, which the MPU may modify by writing another color. Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (8 bits each of red, green, and blue) may be read or written to three Bt461/462s in a single MPU cycle. In this application, the CE\* inputs of all three Bt461/462s are connected together. If only an 8-bit data bus is available, the CE\* inputs must be individually selected during the appropriate color write cycle (red CE\* during red write cycle, green CE\* during green write cycle, and blue CE\* during blue write cycle).

When accessing the primary color palette RAM, the address register resets to \$0000 after a read or write cycle to location \$03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each read or write cycle.

ADDR0-15	C1	C0	Addressed by MPU
\$xxxx	0	0	address register low (ADDR0-7)
\$xxxx	0	1	address register high (ADDR8-9)
\$0000-\$00FF	1	0	alternate color palette RAM
\$0100	1	0	overlay color 0
:	:	:	:
\$011F	1	0	overlay color 31
\$0200	1	0	ID register
\$0201	1	0	command register_0
\$0202	1	0	command register_1
\$0203	1	0	command register_2
\$0204	1	0	pixel read mask register low
\$0205	1	0	pixel read mask register high
\$0206	1	0	pixel blink mask register low
\$0207	1	0	pixel blink mask register high
\$0208	1	0	overlay read mask register
\$0209	1	0	overlay blink mask register
\$020C	1	0	test register
\$0000-\$03FF	1	1	primary color palette RAM

**Table 1. Address Register (ADDR) Operation.**

## Circuit Description (continued)

### Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or overlay RAM. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. Reading color data is similar to writing it, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt461/462 is programmed to be a red, green, or blue RAMDAC and will respond only to the assigned color read or write cycle. In this application, the Bt461/462s share a common 8-bit data bus. The CE\* inputs of all three Bt461/462s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the primary color palette RAM, the address register resets to \$0000 after a blue read or write cycle to location \$03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits.

The other 10 bits of the address register (ADDR0–9) are accessible to the MPU.

Command register0 is used to specify whether the device loads or outputs data during the red, green, or blue cycle. This mode is useful if only an 8-bit data bus is available, and the software drivers are written for RGB operation.

CE\* must be a logical zero during each of the red, green, and blue read/write cycles.

### Additional Information

Although the color palette RAMs and overlay RAM are dual ported, if the pixel and overlay data are addressing the same palette entry being written to by the MPU during the write cycle, 1 or more of the pixels on the display screen can be disturbed. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as specified in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations. ADDR0 and ADDR8 correspond to D0. ADDR10–ADDR15 are always logical zeros.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt461/462.

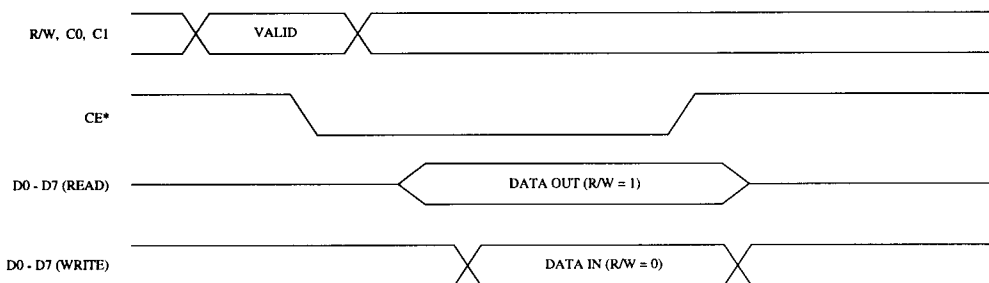


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

**Frame Buffer Interface**

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt461/462 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD\*, sync and blank information, color, and overlay information for 3, 4, or 5 consecutive pixels are latched into the device. With this configuration, the sync and blank timing will be recognized only with 3-, 4-, or 5-pixel resolution. Typically, the LD\* signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs.

Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD\* may be phase-shifted in any amount, relative to CLOCK. This enables the LD\* signal to be de-

rived by externally dividing CLOCK by 3, 4, or 5, independent of the propagation delays of the LD\* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD\*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD\* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 3:1 multiplexing is specified, only one rising edge of LD\* should occur every three clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD\* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD\* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD\* signal and will continuously attempt to resynchronize itself to LD\*.

*The 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.*

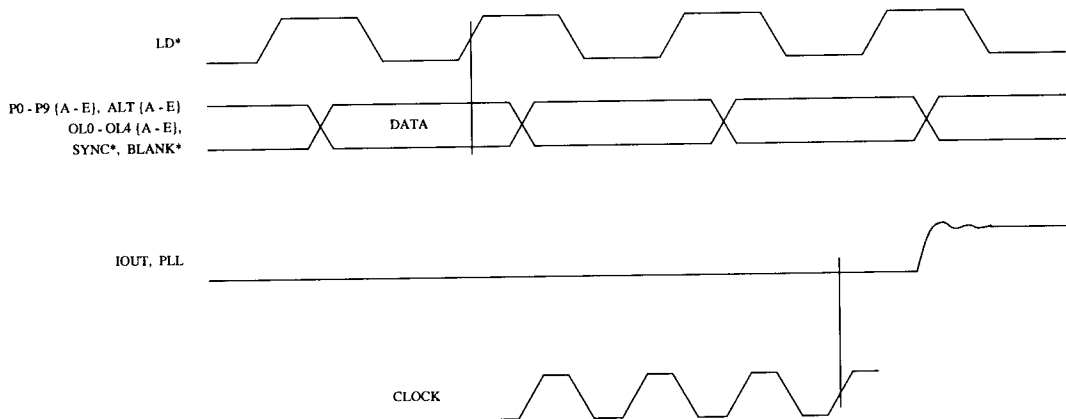


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

**Read and Blink Masking**

Each clock cycle, 10 bits of color information (P0–P9, ALT) and 5 bits of overlay information (OL0–OL4) for each pixel are processed by the read mask, blink mask, and command registers. Through the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that blinking does not cause a color change during the active display time (i.e., in the middle of the screen), the Bt461/462 monitors the BLANK\* input to determine vertical retrace intervals, i.e., that BLANK\* has been a logical zero for at least 256 LD\* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 2 illustrates the truth table used for color selection.

**Alternate Color Palette RAM**

The pixel read mask and blink mask registers can also be used when the pixel inputs are addressing the alternate color palette RAM.

If the ALT enable bit in command register\_0 is a logical one, the alternate color palette RAM may be accessed on a pixel basis. A logical one on an ALT {A–E} input forces the P0–P7 {A–E} inputs to address the alternate color palette RAM. P8 and P9 {A–E} are ignored in this instance. If the ALT enable bit in command register\_0 is a logical zero, the ALT {A–E} inputs are ignored, as specified in Tables 2 and 3.

The primary color palette RAM may be pixel bypassed with the ALT inputs. In this instance, the alternate color palette RAM should be loaded either so that each byte contains its corresponding address (\$00–\$FF) or with a gamma correction factor. The ALT inputs would then specify, on a pixel basis, whether to bypass the primary color palette RAM.

CR04	ALT	CR05	OL0 - OL4	P0 - P9	Addressed by frame buffer
x	x	x	\$1F	\$xxx	overlay color 31
:	:	:	:	:	:
x	x	x	\$01	\$xxx	overlay color 1
x	x	1	\$00	\$xxx	overlay color 0
0	x	0	\$00	\$000	primary RAM location \$000
0	x	x	\$00	\$001	primary RAM location \$001
:	:	:	:	:	:
0	x	x	\$00	\$3FF	primary RAM location \$3FF
x	0	0	\$00	\$000	primary RAM location \$000
x	0	x	\$00	\$001	primary RAM location \$001
:	:	:	:	:	:
x	0	x	\$00	\$3FF	primary RAM location \$3FF
1	1	0	\$00	\$x00	alternate RAM location \$00
:	:	x	:	\$x01	alternate RAM location \$01
:	:	:	:	:	:
1	1	x	\$00	\$xFF	alternate RAM location \$FF

Table 2. Bt461—Palette and Overlay Select Truth Table.

Circuit Description (continued)

CR22	CR04	ALT	CR05	OL4	OL0-OL3	P0-P9	Addressed by Frame Buffer
x : : : : x	x : : : : x	x : : : : x	x : : : x 1	1 : 1 0 : 0	1111 : 0000 1111 : 0000	\$xxx : : : : \$xxx	overlay color 31 : : overlay color 16 overlay color 15 : : overlay color 0
0 x : : x	0 : : : 0	x : : : x	0 x : : x	0 : : : 0	0000 : : : 0000	\$000 \$001 : : \$3FF	primary RAM location \$000 primary RAM location \$001 : : primary RAM location \$3FF
0 x : : x	x : : : x	0 : : : 0	0 x : : x	0 : : : 0	0000 : : : 0000	\$000 \$001 : : \$3FF	primary RAM location \$000 primary RAM location \$001 : : primary RAM location \$3FF
x : : x	1 : : 1	1 : : 1	x : : x	0 : : 0	0000 : : 0000	\$x00 : : \$xFF	alternate RAM location \$00 : : alternate RAM location \$FF
1 : : 1	x : : x	x : : x	x : x 0	0 : 0 1	1111 : 0001 0000	\$xxx : \$xxx \$000	overlay color 15 : : overlay color 1 overlay color 0 (underlay)

Table 3. Bt462—Palette and Overlay Select Truth Table.

## Circuit Description (continued)

### Pixel Panning

To support pixel panning, command register\_1 specifies by what number of clock cycles to pan.

If 0-pixel panning is specified, pixel {A} is output first, followed by pixel {B}, then pixel {C}, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, then pixel {D}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval and will not be on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval and will not be on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

When a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt461/462 during the first LD\* cycle that BLANK\* is a logical zero.

The pixel, overlay, and ALT inputs are all panned.

### Underlay Operation (Bt462 Only)

An underlay plane can be obtained by converting overlay plane 4 (OL4) to underlay operation (command register bit CR22). In this mode of operation, only 15 overlays (OL0–OL3) are available, as specified in Table 3.

During underlay operation, the corresponding overlay plane 4 (OL4) overlay read mask register bit must be a logical zero for proper operation.

Underlays may be displayed on a pixel basis. Both overlays and the underlay may be used simultaneously. The priority of the display information is:

1. Overlays (OL0–OL3)
2. Pixel data (P0–P9)
3. Underlay (OL4)

### Video Generation

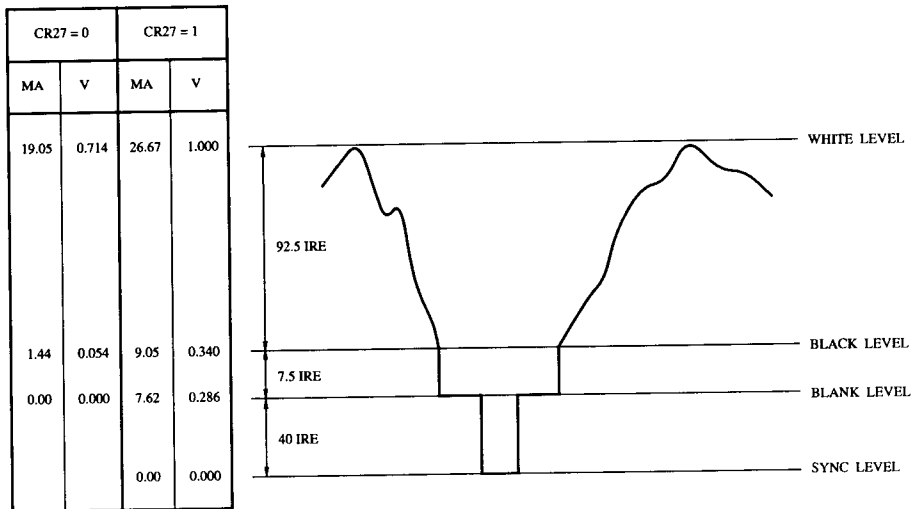
Every clock cycle the selected 8 bits of color information are presented to the 8-bit D/A converter.

The SYNC\* and BLANK\* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Command register2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converter produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 4 and 5 detail how the SYNC\* and BLANK\* inputs modify the output levels.

The D/A converter on the Bt461/462 uses a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description (continued)



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

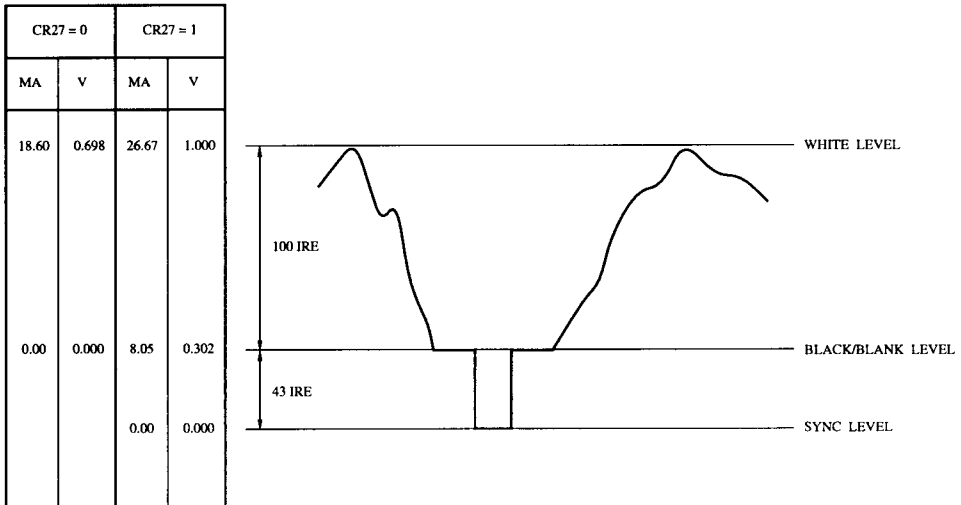
Figure 3. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	\$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	\$00
BLACK - SYNC	1.44	1.44	0	1	\$00
BLANK	7.62	0	1	0	\$xx
SYNC	0	0	0	0	\$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 523 Ω and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



Note: 75 Ω doubly-terminated load, RSET = 495 Ω, and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	\$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	\$00
BLACK - SYNC	0	0	0	1	\$00
BLANK	8.05	0	1	0	\$xx
SYNC	0	0	0	0	\$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

## Internal Registers

### Command Register\_0

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR00 corresponds to data bus bit D0.

CR07, CR06	Multiplex select	<ul style="list-style-type: none"> <li>(00) 3:1 multiplexing</li> <li>(01) 4:1 multiplexing</li> <li>(10) reserved</li> <li>(11) 5:1 multiplexing</li> </ul>	<p>These bits specify whether 3:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 3:1 is specified, the {D} and {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one third the CLOCK rate. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fifth the CLOCK rate.</p> <p>The pipeline delay of the Bt461/462 can be reset to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt461/462 must again be reset to a fixed pipeline delay.</p> <p><i>The 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.</i></p>
CR05	Overlay 0 enable	<ul style="list-style-type: none"> <li>(0) use color palette RAMs</li> <li>(1) use overlay color 0</li> </ul>	<p>When the overlay bits are \$00, this bit specifies whether to use the color palette RAMs or overlay color 0 to provide color information.</p>
CR04	ALT enable	<ul style="list-style-type: none"> <li>(0) disable alternate palette</li> <li>(1) enable alternate palette</li> </ul>	<p>This bit specifies whether the alternate color palette RAM is enabled (logical one) or disabled (logical zero) from being addressed by the ALT {A-E} and P0-P7 {A-E} inputs.</p>
CR03, CR02	Blink rate selection	<ul style="list-style-type: none"> <li>(00) 16 on, 48 off (25/75)</li> <li>(01) 16 on, 16 off (50/50)</li> <li>(10) 32 on, 32 off (50/50)</li> <li>(11) 64 on, 64 off (50/50)</li> </ul>	<p>These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off).</p>
CR01	reserved (logical zero)		
CR00	reserved (logical zero)		

## Internal Registers (continued)

### *Command Register\_1*

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR10 corresponds to data bus bit D0.

CR17–CR15    Pan select

(000)	0 pixels	{pixel A}
(001)	1 pixel	{pixel B}
(010)	2 pixels	{pixel C}
(011)	reserved	
(100)	3 pixels	{pixel D}
(101)	4 pixels	{pixel E}
(110)	reserved	
(111)	reserved	

These bits specify the number of pixels to be panned. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, {pixel C} indicates pixel C will be output first, etc. These bits are typically modified only during the vertical retrace interval.

The pixel, overlay, and ALT inputs are all panned.

CR14–CR10    reserved (logical zero)

## Internal Registers (continued)

**Command Register\_2**

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up. CR20 corresponds to data bus bit D0.

CR27	Sync enable  (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto the video waveform (logical one) or not (logical zero).
CR26	Pedestal enable  (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video waveform. A 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select  (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt461/462 each write cycle, and color data is output each read cycle. If (01), (10), or (11) is specified, the Bt461/462 expects color data to be input and output using (red, green, and blue) cycles. The exact value indicates during which one of the three color cycles it is to load or output color information.
CR23	PLL select  (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses the SYNC* or BLANK* input to generate PLL information.
CR22	Bt461—reserved (logical zero)  Bt462—Underlay enable (0) overlay plane 4 (1) underlay plane 0	This bit is always a logical zero on the Bt461.  On the Bt462, this bit specifies whether overlay plane 4 (OL4) should be converted to an underlay plane (logical one) or used as a normal overlay plane (logical 0).
CR21	reserved (logical zero)	
CR20	Test enable  (0) disable test register (1) enable test register	A logical one enables the P9 {A–E} inputs to serve as a trigger for the test register. A logical zero enables normal operation.

## Internal Registers (continued)

### *ID Register*

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt461/462, the value read by the MPU will be \$4D for the Bt461 and \$4C for the Bt462. Data written to this register is ignored.

### *Pixel Read Mask Register*

The 16-bit pixel read mask register is configured as two 8-bit registers (pixel read mask low and pixel read mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM.

pixel read mask register high								pixel read mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

### *Pixel Blink Mask Register*

The 16-bit pixel blink mask register is configured as two 8-bit registers (pixel blink mask low and pixel blink mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register\_0.

pixel blink mask register high								pixel blink mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

In order for a bit plane to blink, the corresponding bit in the pixel read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after powerup.

## Internal Registers (continued)

### ***Overlay Read Mask Register***

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D4 corresponds to overlay plane 4 (OL4 {A–E}). Each register bit is logically ANDed with the corresponding overlay plane input. Bits D5–D7 are logical zeros. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

On the Bt462, the overlay read mask register for overlay plane 4 (OL4) must be a logical zero when in the underlay mode.

### ***Overlay Blink Mask Register***

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register\_0. D0 corresponds to overlay plane 0 (OL0 {A–E}), and D4 corresponds to overlay plane 4 (OL4 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. Bits D5–D7 are logical zeros. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

### ***Test Register***

The test register enables the MPU to verify that the pixel and overlay ports are addressing the color palette RAM and overlay registers correctly at full speed.

P9 {A–E} is the fast port trigger when CR20 is a logical one. P0–P8 {A–E}, ALT {A–E}, and OL0–OL4 {A–E} address the primary color palette RAM, alternate palette RAM, and overlay registers. A logical one on P9A latches the {A} color data into the test register as it is passed from the color palette to the D/A converter. A logical one on P9B latches the {B} color data into the test register as it is passed from the color palette to the D/A converter, a logical one on P9C latches the {C} color, etc.

To test the entire color palette, bit D1 in the pixel read mask register high (P9) must be a logical zero to test the lower 512 entries. Next, bit D1 in the pixel read mask register high (P9) must be a logical one to test the higher 512 entries. There should be only a single one on the P9 inputs per test read cycle.

A recommended test read cycle is four LD\* cycles long. The test register may be written whenever the test mode is disabled or while in the test mode when no ones are present on the P9 inputs. The test registers are not initialized.

## Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as specified in Tables 4 and 5. BLANK* is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input typically switches off a 40 IRE current source on the IOUT output (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0-P9 {A-E}, OL0-OL4 {A-E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is one third, one fourth, or one fifth the CLOCK rate, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
P0-P9 {A-E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the primary or alternate color palette RAMs is to be used to provide color information (see Table 2). Through this port, 3, 4, or 5 consecutive pixels (up to 10 bits per pixel) are input. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.
OL0-OL4 {A-E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD*. In conjunction with CR05 in command register_0, they specify which palette is to be used for color information, as presented in Table 2. When accessing the overlay palette RAM, the P0-P9 {A-E} and ALT {A-E} inputs are ignored. Overlay information bits (up to 5 bits per pixel) for 3, 4, or 5 consecutive pixels are input through this port. Unused inputs should be connected to GND.
ALT {A-E}	Palette select inputs (TTL compatible). These inputs are latched on the rising edge of LD*. They specify which color palette RAM is to be used for color information, as presented in Table 2. When accessing the alternate color palette RAM, the P8-P9 {A-E} inputs are ignored. Unused inputs should be connected to GND.
IOUT	Analog current output. This high-impedance current source can directly drive a doubly-terminated 75 Ω coaxial cable (Figure 6 in the PC Board Layout Considerations section).
PLL	<p>Phase lock loop output current. This high-impedance current source is used to enable multiple Bt461/462s to be synchronized with subpixel resolution when used with an external PLL. A logical one on the SYNC* or BLANK* input (as specified by CR23 in command register_2) results in no output of current onto this pin, while a logical zero results in the following current output:</p> $\text{PLL (mA)} = 3,227 * \text{VREF (V)} / \text{RSET } (\Omega)$ <p>If subpixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).</p>

## Pin Descriptions (continued)

Pin Name	Description
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 $\mu$ F ceramic capacitor must be connected between this pin and VAA (Figure 6). When the capacitor is connected to VAA rather than to GND, the highest possible power supply noise rejection is provided. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and to maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. <i>The PC Board Layout Considerations section contains critical layout criteria.</i>
FS ADJUST	<p>Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 6). The IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current.</p> <p>The relationship between RSET and the full-scale output current on IOUT for a 7.5 IRE blanking pedestal is:</p> $\text{RSET } (\Omega) = 11,294 * \text{VREF } (\text{V}) / \text{IOUT } (\text{mA})$ <p>The relationship between RSET and the full-scale output current on IOUT for a 0 IRE blanking pedestal is:</p> $\text{RSET } (\Omega) = 10,684 * \text{VREF } (\text{V}) / \text{IOUT } (\text{mA})$
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 5, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 $\mu$ F ceramic capacitor is used to decouple this input to VAA, as shown in Figure 6. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Glitches should be avoided on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be logical zeros. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE* (see Figure 1).
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as presented in Table 1. They are latched on the falling edge of CE*.
D0-D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

## Pin Descriptions (continued)—132-pin PGA Package

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L1	P8A	G14	VAA	J1
SYNC*	K3	P8B	G13	VAA	J2
LD*	A5	P8C	F14	VAA	J3
CLOCK	K1	P8D	F13	VAA	C6
CLOCK*	K2	P8E	E14	VAA	F12
				VAA	M9
P0A	E3	P9A	J13		
P0B	D2	P9B	J14	GND	H1
P0C	D1	P9C	H12	GND	H2
P0D	E2	P9D	H13	GND	H3
P0E	F3	P9E	H14	GND	C7
				GND	G12
P1A	A1	ALTA	L14	GND	M8
P1B	D3	ALTB	K12		
P1C	C2	ALTC	K13	COMP	N9
P1D	B1	ALTD	K14	FS ADJUST	M10
P1E	C1	ALTE	J12	VREF	P9
P2A	A3	OL0A	E1	CE*	P13
P2B	B3	OL0B	F2	R/W	N12
P2C	A2	OL0C	F1	C1	P12
P2D	C3	OL0D	G3	C0	M11
P2E	B2	OL0E	G2		
				D0	L13
P3A	A8	OL1A	M1	D1	M14
P3B	A7	OL1B	L2	D2	L12
P3C	B7	OL1C	N1	D3	M13
P3D	A6	OL1D	L3	D4	N14
P3E	B6	OL1E	M2	D5	P14
				D6	N13
P4A	C9	OL2A	M3	D7	M12
P4B	B9	OL2B	N2		
P4C	A9	OL2C	P1	reserved	G1
P4D	C8	OL2D	P2	reserved	N11
P4E	B8	OL2E	N3	reserved	M7
				reserved	N7
P5A	B11	OL3A	M4	reserved	P7
P5B	A11	OL3B	P3	reserved	P8
P5C	C10	OL3C	N4	reserved	N8
P5D	B10	OL3D	P4		
P5E	A10	OL3E	M5	reserved	B5
				reserved	C5
P6A	A14	OL4A	N5	reserved	A4
P6B	A13	OL4B	P5	reserved	B4
P6C	B12	OL4C	M6	reserved	C4
P6D	C11	OL4D	N6		
P6E	A12	OL4E	P6	reserved	C14
				reserved	C13
P7A	E13	IOUT	P10	reserved	B14
P7B	E12	reserved	P11	reserved	C12
P7C	D14	PLL	N10	reserved	B13
P7D	D13				
P7E	D12				

Pin Descriptions (continued)—132-pin PGA Package

14	P6A	N/C	N/C	P7C	P8E	P8C	P8A	P9E	P9B	ALTD	ALTA	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	P8D	P8B	P9D	P9A	ALTC	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	P9C	ALTE	ALTB	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	N/C	N/C
10	P5E	P5D	P5C									FS ADJ	PLL	IOUT
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	N/C	N/C
7	P3B	P3C	GND									N/C	N/C	N/C
6	P3D	P3E	VAA									OL4C	OL4D	OL4E
5	LD*	N/C	N/C									OL3E	OL4A	OL4B
4	N/C	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	<b>PIA</b>	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C
	A	B	C	D	E	F	G	H	J	K	L	M	N	P

**Bt461/462**

(TOP VIEW)

alignment  
marker  
(on top)

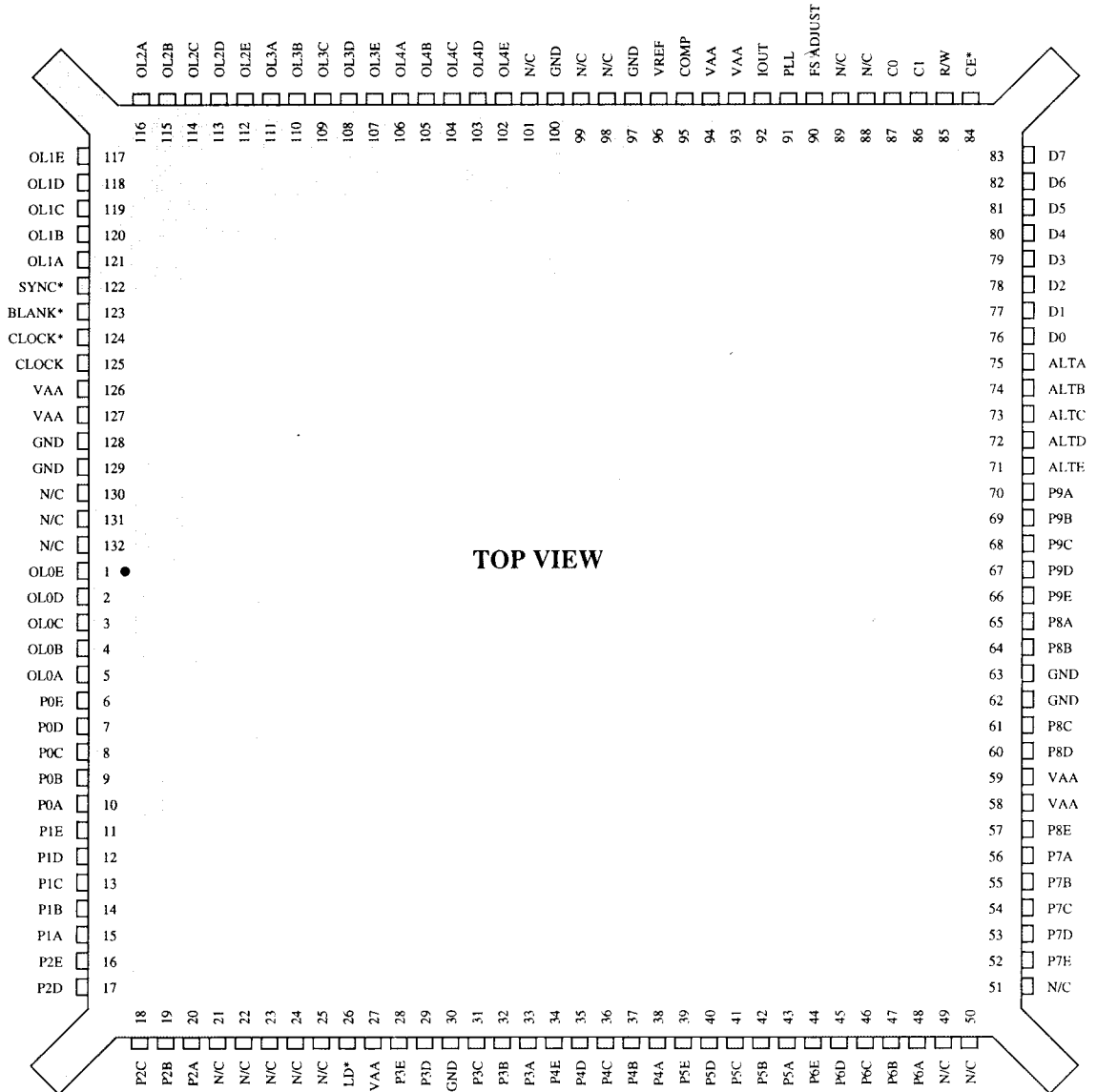
14	D5	D4	D1	ALTA	ALTD	P9B	P9E	P8A	P8C	P8E	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	ALTC	P9A	P9D	P8B	P8D	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	ALTB	ALTE	P9C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	N/C	N/C	C0									P6D	P5A	P5B
10	IOUT	PLL	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	N/C	N/C	GND									P4D	P4E	P3A
7	N/C	N/C	N/C									GND	P3C	P3B
6	OL4E	OL4D	OL4C									VAA	P3E	P3D
5	OL4B	OL4A	OL3E									N/C	N/C	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	N/C
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	POD	POB	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	<b>PIA</b>
	P	N	M	L	K	J	H	G	F	E	D	C	B	A

(BOTTOM VIEW)

Pin Descriptions (continued)—132-pin PQFP Package (Bt462 Only)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	OL0E	44	P6E	88	reserved
2	OL0D	45	P6D	89	reserved
3	OL0C	46	P6C		
4	OL0B	47	P6B	90	FS ADJUST
5	OL0A	48	P6A	91	PLL
				92	IOUT
6	P0E	49	reserved	93	VAA
7	P0D	50	reserved	94	VAA
8	P0C	51	reserved	95	COMP
9	P0B			96	VREF
10	P0A	52	P7E	97	GND
		53	P7D	98	reserved
11	P1E	54	P7C	99	reserved
12	P1D	55	P7B	100	GND
13	P1C	56	P7A	101	reserved
14	P1B				
15	P1A	57	P8E	102	OL4E
		58	VAA	103	OL4D
16	P2E	59	VAA	104	OL4C
17	P2D	60	P8D	105	OL4B
18	P2C	61	P8C	106	OL4A
19	P2B	62	GND		
20	P2A	63	GND	107	OL3E
		64	P8B	108	OL3D
21	reserved	65	P8A	109	OL3C
22	reserved			110	OL3B
23	reserved	66	P9E	111	OL3A
24	reserved	67	P9D		
25	reserved	68	P9C	112	OL2E
		69	P9B	113	OL2D
26	LD*	70	P9A	114	OL2C
27	VAA			115	OL2B
		71	ALTE	116	OL2A
28	P3E	72	ALTD		
29	P3D	73	ALTC	117	OL1E
30	GND	74	ALTB	118	OL1D
31	P3C	75	ALTA	119	OL1C
32	P3B			120	OL1B
33	P3A	76	D0	121	OL1A
		77	D1		
34	P4E	78	D2	122	SYNC*
35	P4D	79	D3	123	BLANK*
36	P4C	80	D4	124	CLOCK*
37	P4B	81	D5	125	CLOCK
38	P4A	82	D6		
		83	D7	126	VAA
39	P5E			127	VAA
40	P5D	84	CE*	128	GND
41	P5C	85	R/W	129	GND
42	P5B	86	C1		
43	P5A	87	C0	130	reserved
				131	reserved
				132	reserved

Pin Descriptions (continued)—132-pin PQFP Package (Bt462 Only)



## PC Board Layout Considerations

### PC Board Considerations

The Bt461 and Bt462 layout should be optimized for lowest noise on their power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane, layer 3 the analog power plane, and the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt461 and Bt462 to be located as close as possible to the power supply connector and the video output connector.

### Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 5.

### Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

### Power Supply Decoupling

The best power supply decoupling performance is obtained by providing a 0.1  $\mu\text{F}$  ceramic capacitor in parallel with a 0.01  $\mu\text{F}$  chip capacitor to decouple each group of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 10  $\mu\text{F}$  capacitor shown in Figure 6 is for low-frequency power supply ripple; the 0.1  $\mu\text{F}$  and 0.01  $\mu\text{F}$  capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

### COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1  $\mu\text{F}$  ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

### Digital Signal Interconnect

The digital inputs to the Bt461 and Bt462 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ring-

## PC Board Layout Considerations (continued)

ing may be reduced by damping the line with a series resistor (30–300  $\Omega$ ).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must be adequately decoupled to prevent the noise generated by the digital devices from coupling into the analog circuitry.

### Analog Signal Interconnect

The Bt461 and Bt462 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

*The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.*

The video output signals should not overlay the analog power plane, to maximize the high-frequency power supply rejection.

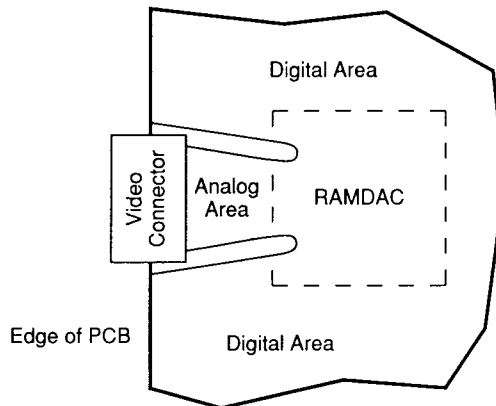
For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

### Analog Output Protection

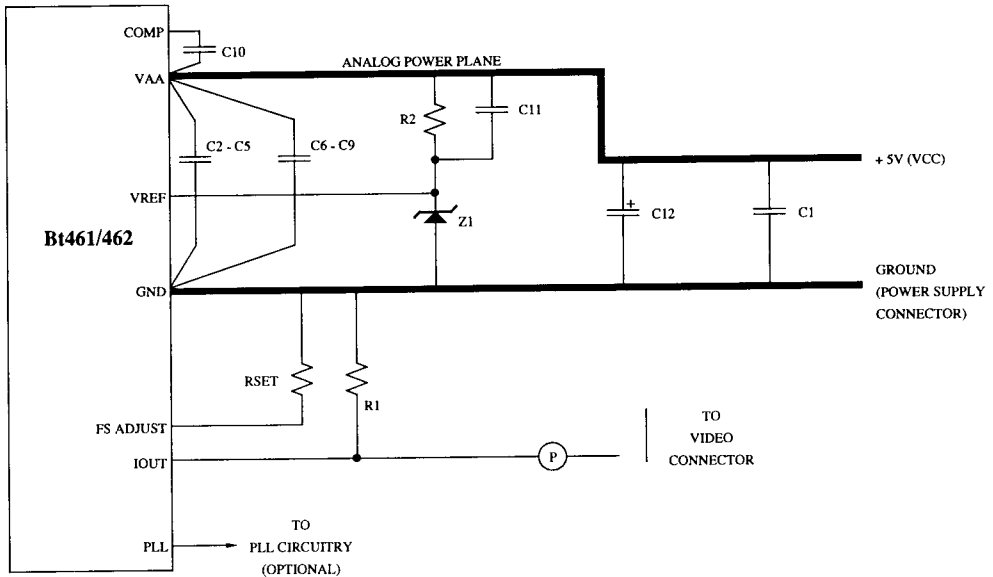
The Bt461 and Bt462 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

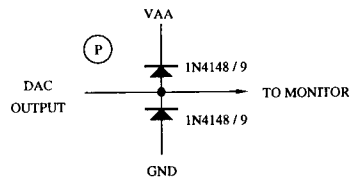


**Figure 5. Sample Layout Showing Power and Ground Plane Isolation Gaps.**

PC Board Layout Considerations (continued)



5



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1  $\mu$ F and 0.01  $\mu$ F capacitors.

Location	Description	Vendor Part Number
C1-C5, C10, C11	0.1 $\mu$ F ceramic capacitor	Erie RPE110Z5U104M50V
C6-C9	0.01 $\mu$ F ceramic chip capacitor	AVX 12102T103QA1018
C12	10 $\mu$ F tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1	75 $\Omega$ 1% metal film resistor	Dale CMF-55C
R2	1000 $\Omega$ 1% metal film resistor	Dale CMF-55C
RSET	523 $\Omega$ 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt461/462.

Figure 6. Typical Connection Diagram and Parts List.

## Application Information

### Nonvideo Applications

The Bt461/462 may be used in nonvideo applications by disabling the video-specific control signals. Bits CR26 and CR27 in command register\_2 should be set to a zero (disabling the BLANK\* and SYNC\* inputs). SYNC\* should be a logical zero, and BLANK\* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$\text{RSET } (\Omega) = 7,457 * \text{VREF (V)} / \text{Iout (mA)}$$

### Using Multiple Devices

When multiple Bt461/462s are used, each Bt461/462 should have its own power plane ferrite bead. In addition, although a single voltage reference may drive multiple devices, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each Bt461/462 has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each Bt461/462 must have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Because of differences in pipelining and analog output delay, it is recommended that Bt461s not be mixed with Bt462s.

### Clock Interfacing

Because of the high clock rates at which the Bt461 and Bt462 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK\*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK\* inputs require termination resistors (220  $\Omega$  to GND) that should be located as close as possible to the clock driver. A 150  $\Omega$  chip resistor connected between the RAMDAC's CLOCK and CLOCK\* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 7.)

Applications of 160 MHz require robust ECL clock signals with strong pulldown (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK\* inputs must be differential signals and greater than 0.6 V peak to peak because of the noise margins of the CMOS process. The Bt461/462 will not function if it uses a single-ended clock with CLOCK\* connected to ground.

Typically, LD\* is generated by dividing CLOCK by 3, 4, or 5 (depending on whether 3:1, 4:1, or 5:1 multiplexing was specified) and translating the result to TTL levels. As LD\* may be phase shifted relative to CLOCK, propagation delays need not be considered when the LD\* signal is derived. LD\* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (e.g., SYNC\* and BLANK\*).

## Application Information (continued)

**Setting the Pipeline Delay**

The pipeline delay of the Bt461, although fixed after a power-up condition, may be anywhere from 6 to 10 clock cycles. The pipeline delay of the Bt462, although fixed after a power-up condition, may be anywhere from 8 to 12 clock cycles. The Bt461/462 contains additional circuitry enabling the pipeline delay to be fixed (8 clock cycles for the Bt461 and 10 clock cycles for the Bt462). The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt461/462.

To reset the Bt461/462, it should be powered up with LD\*, CLOCK, and CLOCK\* running. The CLOCK and CLOCK\* signals should be stopped with CLOCK high and CLOCK\* low for *at least* three rising edges of LD\*. The device can be held with CLOCK and CLOCK\* stopped for an unlimited time.

CLOCK and CLOCK\* should be restarted so that the first edge of the signals is as close as possible to the rising edge of LD\*. (The falling edge of CLOCK leads the rising edge of LD\* by no more than 1 clock cycle or follows the rising edge of LD\* by no more than 1.5 clock cycles.) When the clocks are restarted, the minimum clock pulse width must not be violated.

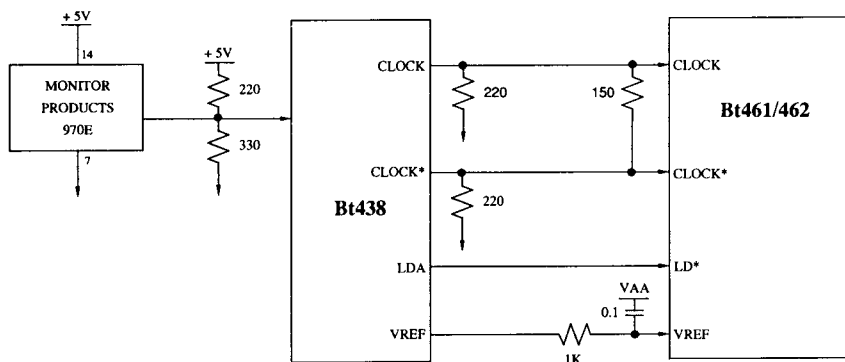
When the Bt461/462 is reset to a fixed pipeline delay, the blink counter circuitry is also reset. If the Bt461/462 is periodically reset (for example, at every vertical sync interval), the on-chip blink counter will not function correctly. In this instance, the blink mask register should be \$00, and the overlay blink enable bits should be logical zeros. Software may control blinking through the read mask register and overlay display enable bits.

In standard operation, the Bt461/462 must be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

**Monochrome Display Applications**

For monochrome display applications where a single Bt461/462 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461/462, and sets the pipeline delay of the Bt461/462 to 8 (Bt461) or 10 (Bt462) clock cycles. The Bt438 may also be used to interface the Bt461/462 to a TTL clock. Figure 7 illustrates use of the Bt438 with the Bt461/462.

When a single Bt461/462 is used, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150  $\Omega$ ).



**Figure 7. Generating the Bt461/462 Clock Signals (Monochrome Application).**

Application Information (continued)

Color Display Applications

For color display applications where up to four Bt461/462s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461/462, synchronizes the Bt461/462s to subpixel resolution, and sets the pipeline delay of the Bt461 to 8 clock cycles and the Bt462 to 10 clock cycles. The Bt439 may also be used to interface the Bt461/462 to a TTL clock. Figure 8 illustrates use of the Bt439 with the Bt461/462.

Subpixel synchronization is supported by the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt461/462, relative to CLOCK. The Bt439 compares the phase of

the PLL signals generated by up to four Bt461/462s. The Bt439 then adjusts the phase of the CLOCK and CLOCK\* signals to each Bt461/462 to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to ensure proper clock alignment.

If subpixel synchronization of multiple Bt461/462s is not necessary, the Bt438 Clock Generator Chip may be used rather than the Bt439. In this instance, the CLOCK, CLOCK\*, and LD\* inputs of up to four Bt461/462s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). Skew must be minimized on the CLOCK and CLOCK\* lines. The PLL outputs are not used and should be connected to GND (either directly or through a resistor up to 150 Ω).

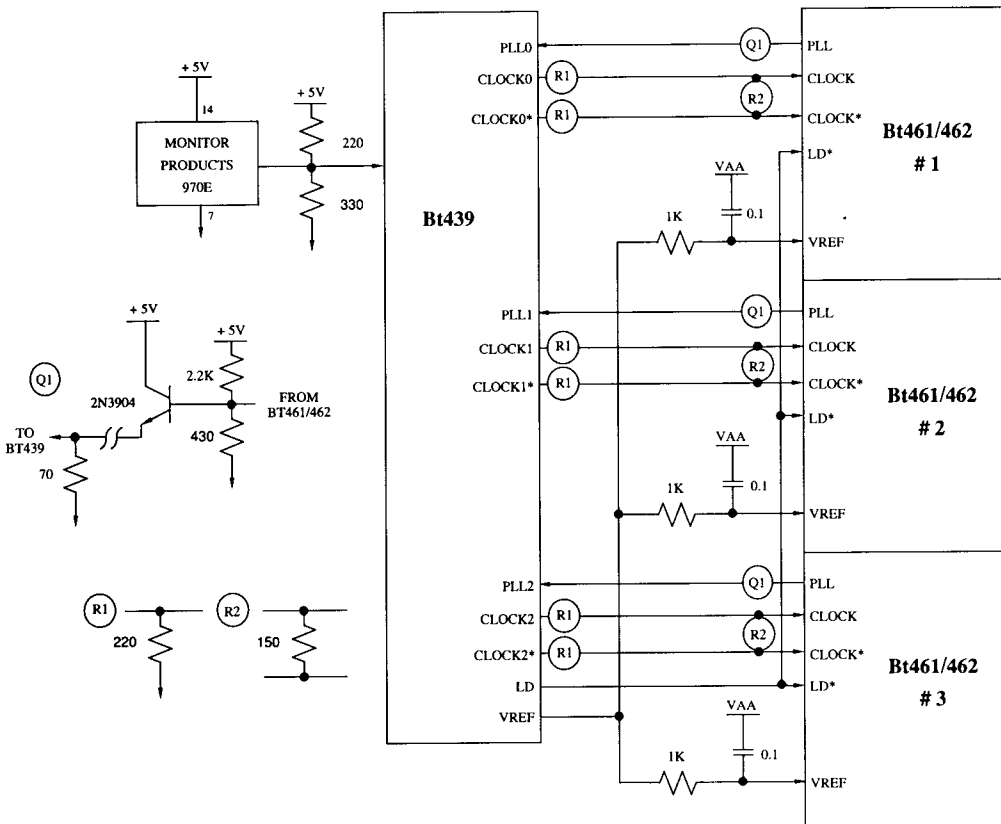


Figure 8. Generating the Bt461/462 Clock Signals (Color Application).

## Application Information (continued)

### Initializing the Bt461/462 (Monochrome)

Following a power-on sequence, the Bt461/462 must be initialized. This sequence will configure the Bt461/462 as follows:

4:1 multiplexed operation  
no overlays  
no pixel masking, no blinking, no panning  
color data written/read every cycle  
sync enabled on IOUT, 7.5 IRE blanking pedestal

#### Control Register Initialization

C1, C0

Write \$01 to address register low	00
Write \$02 to address register high	01
Write \$40 to command register_0	10
Write \$02 to address register low	00
Write \$00 to command register_1	10
Write \$03 to address register low	00
Write \$C0 to command register_2	10
Write \$04 to address register low	00
Write \$FF to pixel read mask low	10
Write \$05 to address register low	00
Write \$03 to pixel read mask high	10
Write \$06 to address register low	00
Write \$00 to pixel blink mask low	10
Write \$07 to address register low	00
Write \$00 to pixel blink mask high	10
Write \$08 to address register low	00
Write \$00 to overlay read mask	10
Write \$09 to address register low	00
Write \$00 to overlay blink mask	10

#### Color Palette RAM Initialization

Write \$00 to address register low	00
Write \$00 to address register high	01
Write data to RAM (location \$000)	11
Write data to RAM (location \$001)	11
:	:
Write data to RAM (location \$3FF)	11

#### Overlay Color Palette Initialization

Write \$00 to address register low	00
Write \$01 to address register high	01
Write data to overlay (location \$00)	10
Write data to overlay (location \$01)	10
:	:
Write data to overlay (location \$1F)	10

#### Alternate Color Palette Initialization

Write \$00 to address register low	00
Write \$00 to address register high	01
Write data to alternate (location \$00)	10
Write data to alternate (location \$01)	10
:	:
Write data to alternate (location \$FF)	10

Application Information (continued)

**Initializing the Bt461/462 (Color)  
8-bit MPU Data Bus**

In this example, three Bt461/462s are being used in parallel to generate true color. An 8-bit MPU data bus is available to access the Bt461/462s.

While accessing the command, read mask, blink mask, control/test, and address register, the MPU must access each Bt461/462 individually. While the MPU is accessing the color palette RAM, alternate RAM, or overlay registers, all three Bt461/462s may be accessed simultaneously.

Following a power-on sequence, the Bt461/462s must be initialized. This sequence will configure the Bt461/462s as follows:

- 4:1 multiplexed operation
- no overlays
- no blinking, no panning
- initialize each one as a red, green, or blue device
- sync on all outputs, 7.5 IRE blanking pedestal

**Control Register Initialization**

Red Bt461/462	C1, C0
Write \$01 to address register low	00
Write \$02 to address register high	01
Write \$40 to command register_0	10
Write \$02 to address register low	00
Write \$00 to command register_1	10
Write \$03 to address register low	00
Write \$D0 to command register_2	10
Write \$04 to address register low	00
Write \$FF to pixel read mask low	10
Write \$05 to address register low	00
Write \$03 to pixel read mask high	10
Write \$06 to address register low	00
Write \$00 to pixel blink mask low	10
Write \$07 to address register low	00
Write \$00 to pixel blink mask high	10
Write \$08 to address register low	00
Write \$00 to overlay read mask	10
Write \$09 to address register low	00
Write \$00 to overlay blink mask	10

Green Bt461/462

Write \$01 to address register low	00
Write \$02 to address register high	01
Write \$40 to command register_0	10
Write \$02 to address register low	00
Write \$00 to command register_1	10
Write \$03 to address register low	00
Write \$E0 to command register_2	10
Write \$04 to address register low	00
Write \$FF to pixel read mask low	10
Write \$05 to address register low	00
Write \$03 to pixel read mask high	10
Write \$06 to address register low	00
Write \$00 to pixel blink mask low	10
Write \$07 to address register low	00
Write \$00 to pixel blink mask high	10
Write \$08 to address register low	00
Write \$00 to overlay read mask	10
Write \$09 to address register low	00
Write \$00 to overlay blink mask	10

Blue Bt461/462

Write \$01 to address register low	00
Write \$02 to address register high	01
Write \$40 to command register_0	10
Write \$02 to address register low	00
Write \$00 to command register_1	10
Write \$03 to address register low	00
Write \$F0 to command register_2	10
Write \$04 to address register low	00
Write \$FF to pixel read mask low	10
Write \$05 to address register low	00
Write \$03 to pixel read mask high	10
Write \$06 to address register low	00
Write \$00 to pixel blink mask low	10
Write \$07 to address register low	00
Write \$00 to pixel blink mask high	10
Write \$08 to address register low	00
Write \$00 to overlay read mask	10
Write \$09 to address register low	00
Write \$00 to overlay blink mask	10



## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

## Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND-0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ				
PGA	TJ			+150	°C
PQFP	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
Air Flow					
PGA		0			l.f.p.m.
PQFP		50			l.f.p.m.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Note 1:* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

## DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
I/O Analog Output Resolution Accuracy Integral Linearity Error Differential Linearity Error Gray Scale Error Monotonicity Coding	IL DL	8	8  guaranteed	8  ±1 ±1 ±5	Bits LSB LSB % Gray Scale Binary
Digital Inputs (except CLOCK, CLOCK*) Input High Voltage Input Low Voltage Input High Current (Vin = 2.4V) Input Low Current (Vin = 0.4V) Input Capacitance (f = 1 MHz, Vin = 2.4V)	VIH VIL IIH IIL CIN	2.0 GND-0.5	4	VAA + 0.5 0.8 1 -1 10	V V μA μA pF
Clock Inputs (CLOCK, CLOCK*) Differential Input Voltage Input High Current (Vin = 4.0V) Input Low Current (Vin = 0.4V) Input Capacitance (f = 1 MHz, Vin = 4.0V)	ΔVIN IKIH IKIL CKIN	.6	4	6 1 -1 10	V μA μA pF
Digital Outputs (D0-D7) Output High Voltage (IOH = -400 μA) Output Low Voltage (IOL = 3.2 mA) 3-state Current Output Capacitance	VOH VOL IOZ CDOOUT	2.4	10	. 0.4 10	V V μA pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
IOUT Analog Output Output Current	IOUT				
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	-1.0		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output Output Current	PLL				
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		-1.0		+2.5	V
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, PLL = 0 mA)			15		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

## AC Characteristics

Bt461 170/ Bt462 160		170/160 MHz Devices			135 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			170/160			135	MHz
LD* Rate	LDmax			42.5/40			45	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	60			60			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	5.88/6.25			7.4			ns
Clock Pulse Width High Time	13	2.6/2.8			3.2			ns
Clock Pulse Width Low Time	14	2.6/2.8			3.2			ns
LD* Cycle Time	15	23.5/25			22.2			ns
LD* Pulse Width High Time	16	11			8			ns
LD* Pulse Width Low Time	17	11			8			ns
Analog Output Delay	18							
Bt461			11			11		ns
Bt462			5			5		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			6			8	ns
Clock and Data Feedthrough (Note 1)			tbd			tbd		dB
Glitch Impulse (Note 1)			50			50		pV - sec
Pipeline Delay								
Bt461		6		10	6		10	Clocks
Bt462		8		12	8		12	Clocks
VAA Supply Current (Note 2)	IAA							
Bt461			350	470		330	445	mA
Bt462			344	388		319	365	mA

See test conditions and notes at the end of this section.

DC specifications to remain unchanged.

## AC Characteristics (continued)

Parameter	Symbol	110 MHz Devices			80 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			110			80	MHz
LD* Rate	LDmax			36.7			26.7	MHz
R/W, C0, C1 Setup Time	1				0			ns
R/W, C0, C1 Hold Time	2				15			ns
CE* Low Time	3	0			60			ns
CE* High Time	4				25			ns
CE* Asserted to Data Bus Driven	5	15			7			ns
CE* Asserted to Data Valid	6			75			100	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	60			50			ns
Write Data Hold Time	9				0			ns
		25						
Pixel and Control Setup Time	10				4			ns
Pixel and Control Hold Time	11	7			2			ns
Clock Cycle Time	12				12.5			ns
Clock Pulse Width High Time	13				5			ns
Clock Pulse Width Low Time	14				5			ns
LD* Cycle Time	15				37.5			ns
LD* Pulse Width High Time	16				12			ns
LD* Pulse Width Low Time	17	35			12			ns
Analog Output Delay	18	0						
Bt461			11			11		ns
Bt462			5			5		ns
Analog Output Rise/Fall Time	19		2			3		ns
Analog Output Settling Time	20	3		8			12	ns
Clock and Data Feedthrough (Note 1)			tbd			tbd		dB
Glitch Impulse (Note 1)		2	50			50		pV - sec
Pipeline Delay								
Bt461				10	6		10	Clocks
Bt462		9.09		12	8		12	Clocks
VAA Supply Current (Note 2)	IAA	4						
Bt461			320	430		300	410	mA
Bt462		4	301	344		267	312	mA

See test conditions and notes on next page.

AC Characteristics (continued)

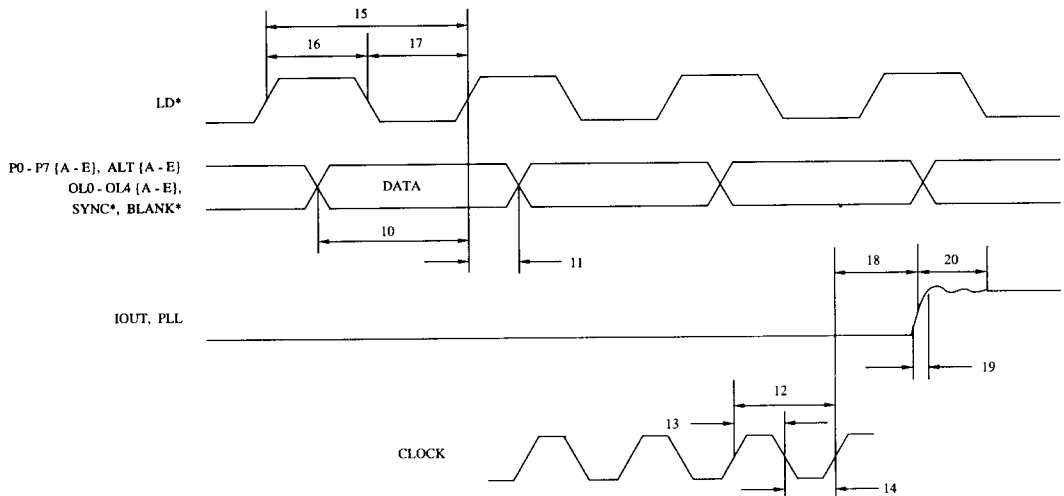
Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V with input rise/fall times ≤ 2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤ 10 pF and D0–D7 output load ≤ 75 pF. See timing waveforms and notes in Figures 9 and 10. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic.

Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 9. Video Input/Output Timing.

Timing Waveforms (continued)

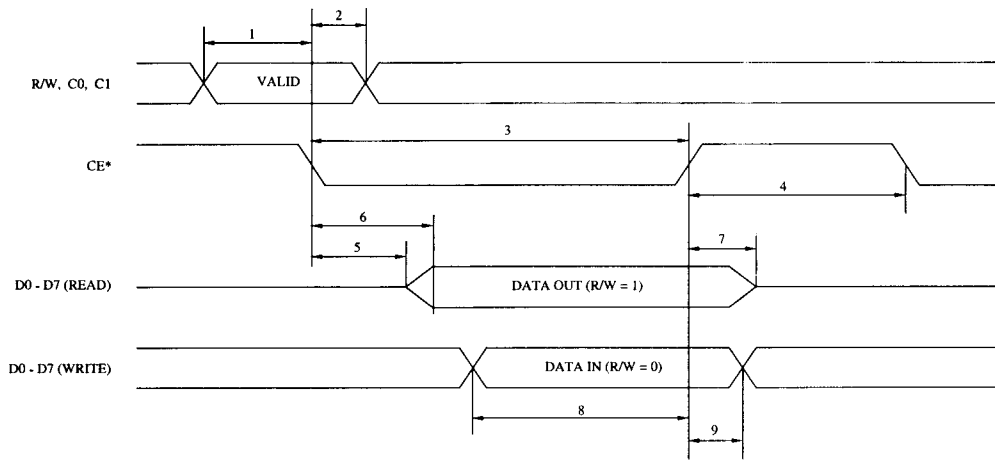


Figure 10. MPU Read/Write Timing Dimensions.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt461KG170	170 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG160	160 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KPF160	160 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF135	135 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF110	110 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF80	80 MHz	132-pin Plastic Quad Flatpack	0° to +70° C