National Semiconductor

PRELIMINARY

NM100492/NM4492 2k x 9 Advanced Self-Timed SRAM

Features

- Extremely fast access time
  - — 5 ns Max (NM4492)
  - — 7 ns Max (NM100492)
- Power supply: −5.2V ± 5% (NM4492)
- Power supply: −4.2V to −4.8V (NM100492)
- Completely self-timed read and write cycle
- On-chip input and output registers
- Modest power consumption—2W at 7 ns, <1.5W at 100 MHz
- On-chip parity checking—with odd address parity mode pin
- Clock enable input simplifies pipeline control
- Scan diagnostics supported by on-chip scan registers
- High speed ceramic flatpak
- High speed TapePak™ package under development
- I/O compatible with F100k standard

General Description

The NM100492/NM4492 is an extremely high performance 2k x 9 SRAM. It is the first of a family of similar 9-bit wide SRAMs designed specifically for very high speed ECL computer applications such as register files, writable control stores, cache RAMs, cache tag RAMs, and address translation lookaside buffers. The NM100492/NM4492 offers several features which are very desirable in such applications.

ADVANCED SELF-TIMED ARCHITECTURE

This advanced self-timed RAM simplifies the system design of extremely fast memory arrays by minimizing the impact of timing skews on the cycle time of the memory array. All input signals (address, data and control signals) are registered on-chip by a transition of the clock. By registering all inputs with minimal setup and hold times (setup + hold = 2 ns) the troublesome skews inherent with traditional static RAM timing requirements are significantly reduced. With skew problems minimized, very short cycle times become practical. Output registers (self-timed on-chip) hold output data valid for an extended portion of the cycle easing system read timing requirements.

HIDDEN WRITE CYCLE MODE

The hidden write cycle timing allows relaxed data bus timing. This will often ease system setup and hold requirements for the data output bus. Hidden write timing is essentially a technique for interleaving reads and writes. This advanced self-timed SRAM supports hidden write timing more conveniently in the system than first generation self-timed SRAM's, due to the unique control signal functions defined for write enable ($\overline{W}$) and chip select ($\overline{S}$). By keeping the output register active (with the last read data) during a write cycle, this device greatly simplifies the timing of interleaved memory architectures. This mode may be very useful in cache and register file applications, where multiple sources and/or destinations may be interleaved within each machine cycle.

PARITY CHECKING

The device also offers several convenient features which may be useful in specific applications. One such feature is the on-chip parity checking function. For systems where parity checking is desirable this device will check for odd parity on the 9-bit data input field, and will check for either even or odd parity (depending on the polarity of the parity mode pin −PM) on the 11-bit address field combined with the address parity input. Odd parity is met when the number of highs in the field is odd. Address parity checking can be conveniently disabled if desired, allowing data field only parity checking. If either the data or address demonstrates a parity error, then the parity error output flag is set. The polarity of the error output flag facilitates emitter dot ORing several error outputs for minimal delay. The parity checking feature is benign in the sense that if parity checking is not desired, the output can simply be ignored without detrimental effects to normal operation.

SERIAL SCAN DIAGNOSTICS REGISTERS

Another convenient feature provided on-chip is the scan diagnostics register. For system designs where scan diagnostics are included, this device allows observing the state of the input registers (scan out) and forcing the state of the input and output registers (scan in). For writable control store applications the control store can be loaded via the serial channel (scan in), simplifying circuit board layout by eliminating the wide parallel data input bus structure. For systems where scan diagnostics are not desired, the scan enable input can simply be left open allowing the on-chip pulldown device to disable scan functions and provide normal SRAM functionality.

PIPELINE CONTROL

Yet a third convenient feature is the clock enable input. This control simplifies starting and stopping pipeline operations in pipelined systems. It reduces, and may eliminate, the need to gate the clock signal external to the RAM. This feature is also benign since the on-chip pulldown device will ensure normal operation if the clock enable is not used.

MODEST POWER CONSUMPTION

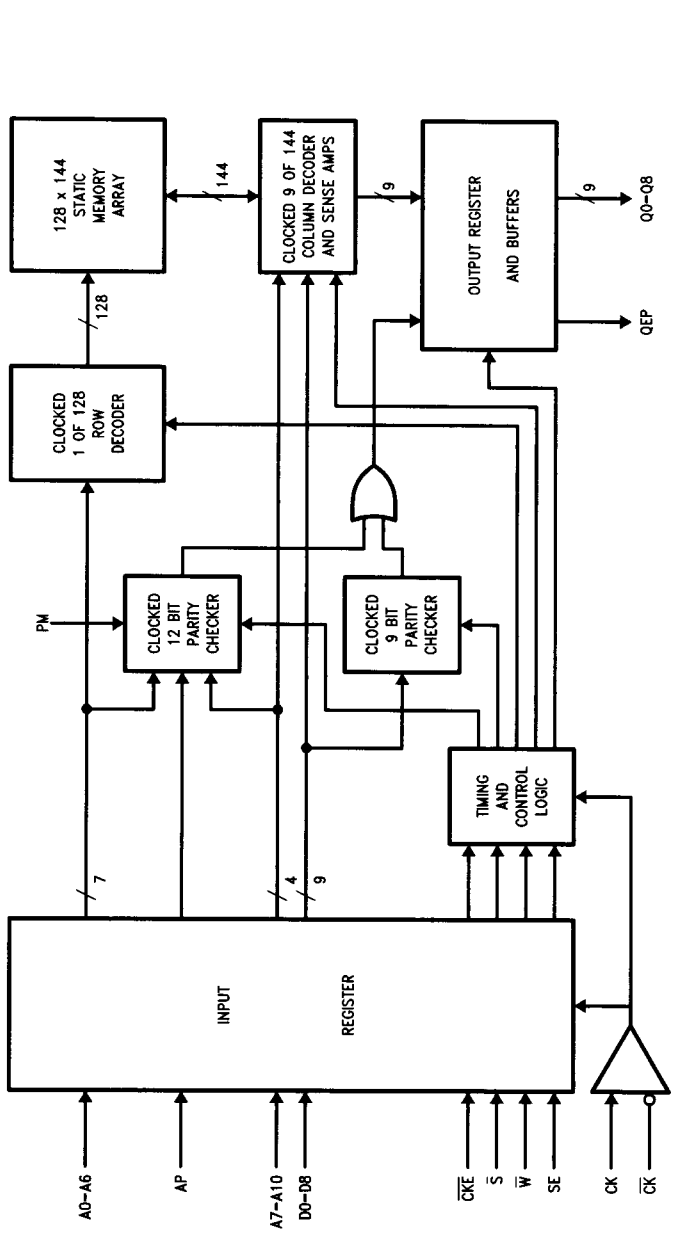
Modest power consumption is achieved without compromising device speed through very unique and innovative circuit design techniques (patents applied for). Power consumption is predominately dependent on clock frequency (1/cycle time) allowing a reduction in power at lower operating frequency.

F100K COMPATIBLE I/O

The device is I/O compatible with standard temperature compensated F100K ECL logic, allowing trouble free interfacing in high performance ECL systems.

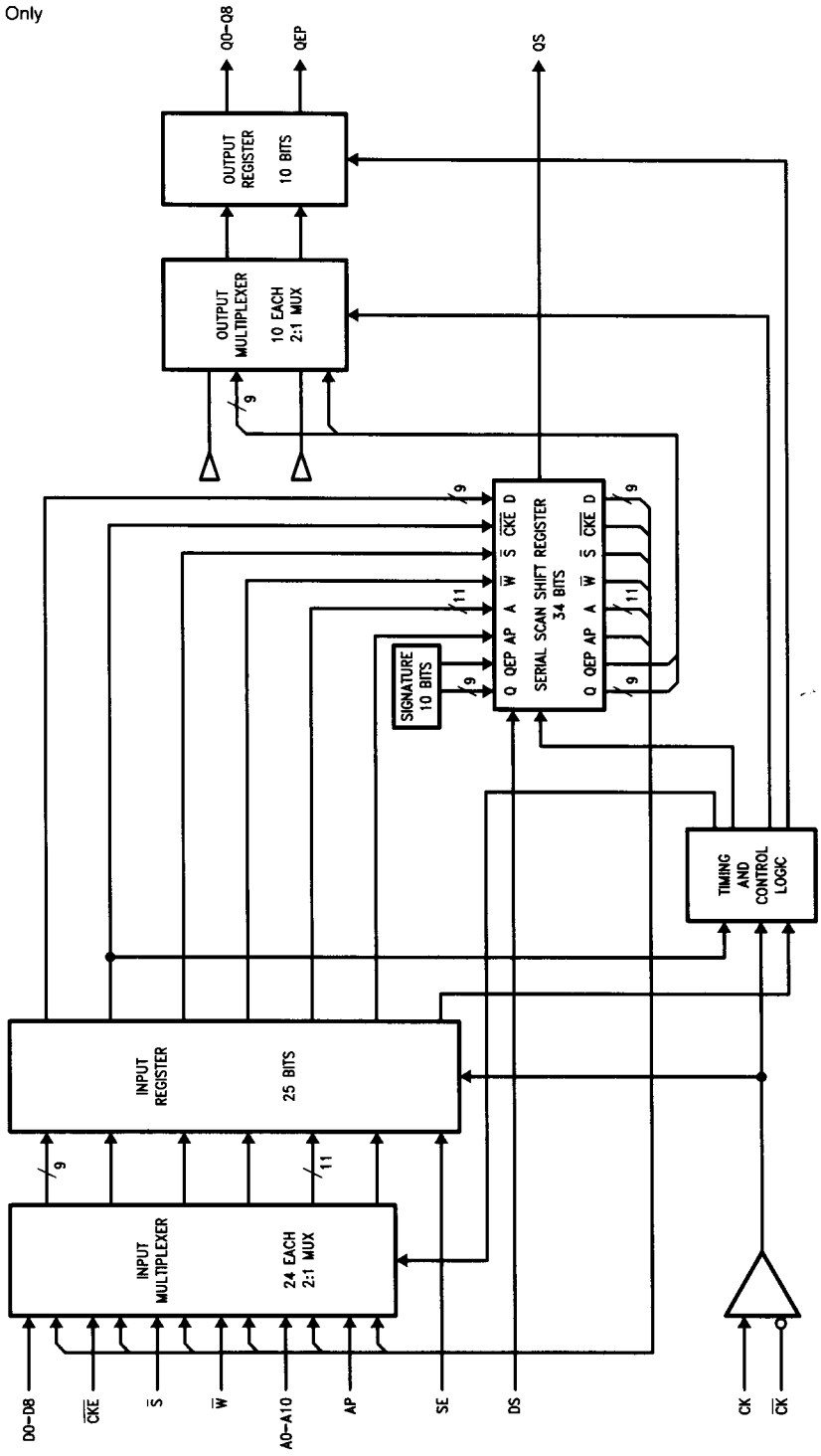
Functional Block Diagram

Scan Functions Excluded



Functional Block Diagram (Continued)

Scan Functions Only



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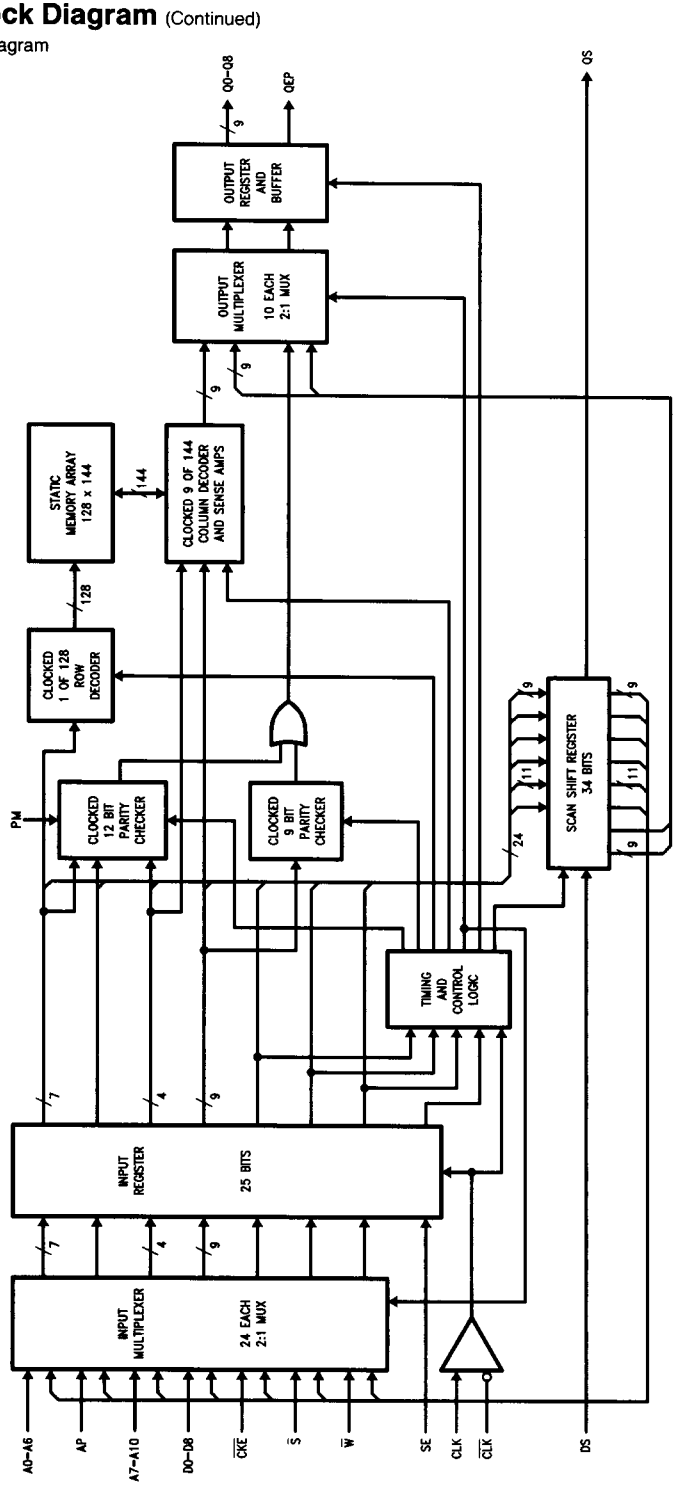
Functional Block Diagram (Continued)

Complete Functional Diagram



Advanced Self-Timed RAM Pin Descriptions

INPUTS

All input signals are registered by the rising edge of the clock, and the falling edge of the clock bar. Address, data in, and control lines are all registered in exactly the same manner, and are all specified for exactly the same input setup and hold requirements.

Pin	Description
A0–A10	**Address Inputs:** Used to select the memory location for storing or retrieving data.
AP	**Address Parity Input:** Should be set/reset to ensure parity when combined with A0–10. May also be tied to V_{EE} to disable parity checking of the address field. An internal pulldown is included to disable address parity checking when this input is not connected.
D0–D8	**Data Inputs:** During a write operation the data inputs are stored in the specified address location.
$\overline{CKE}$	**Clock Enable Input:** When active (low), this input allows the device to function normally with each rising edge of the clock. When inactive, this input will force the device to do nothing on each rising clock edge, thereby providing a convenient means for controlling the clock input to the device. Although this input functions as if it gates the clock on an off, this input actually is registered by the clock exactly as all other inputs and as such has the same input setup and hold requirements as all other inputs. A natural assumption is that gating off the clock with the clock enable control will reduce the device power consumption substantially; but this assumption is in fact false. The state of the clock enable pin has very little effect on power consumption. An internal pulldown device is included to permit normal operation even when not connected.
$\overline{S}$	**Chip Select Input:** Can be used to inhibit a write operation or to force the device outputs to a deselected (low) state when not writing. When active (low), each rising clock edge allows a write or read operation to occur. When inactive, a write operation is precluded. When inactive, and when Write Enable is also inactive, a deselect read operation will force the outputs to the inactive (low) state. An internal pulldown device is included to permit normal operation even when not connected.
$\overline{W}$	**Write Enable Input:** When active (low), each rising clock edge allows a write operation to occur, but when active the write function has no effect on the state of the data output pins. When inactive, each rising clock edge allows either a read operation or a deselect read operation to occur.
PM	**Parity Mode Input:** When tied to V_{EE} device will check for Odd parity on the address field. When tied to V_{CC} device will check for Even parity on the address field.
CK	**Differential Clock Input:** The "true" side of the differential clock input.
$\overline{CK}$	**Differential Clock Input:** The "complement" side of the differential clock input.

Note: Halting the clock does substantially reduce power consumption.

SE	**Scan Enable Input:** Enables the serial scan diagnostics mode. With Scan Enable active (high), the contents of the scan shift register is shifted one position on each rising clock edge. The bit shifted out will appear on the QS pin and the bit shifted in will come from the DS pin. Information serially scanned into the device can be loaded into either the input register or the output register. An internal pulldown device is included to permit normal operation even when not connected.
DS	**Serial Data Input:** When in scan diagnostics mode this input allows serial shifting external data into the scan shift register.

OUTPUTS

QS	**Serial Data Output:** When in scan diagnostics mode this output allows reading internal data directly from the scan shift register. In normal mode, QS will output the same logic level as the last registered value of D8.
Q0–Q8	**Data Outputs:** These represent the contents of the addressed memory location during a read cycle. The outputs will not change unless another read cycle occurs, or unless the outputs are forced inactive (low) by a deselect read operation.
QEP	**Parity Error Output:** Normally low, it goes high when the registered inputs have a parity error. For a read cycle it indicates the address input has a parity error, since data input parity is only checked during write cycles. The parity error output delay approximates access time, appearing close to the time the data word appears in a read cycle. The parity error output signal will remain active (high) for a duration of the one cycle time, after which it may change back to inactive (low) if the next set of inputs contains no parity errors.

POWER SUPPLIES

V_{EE}	Negative Supply
V_{CC}	Positive Supply (Ground)
V_{CCQ}	Positive Supply (Ground) for output buffers only

SHIELD

Used to shield the input pins that are adjacent to V_{CC} and V_{EE} power pins from mutually coupled inductive noise. These pins should be connected to a DC power level or left floating dependent on board layout convenience. Note that the pin marked PM is actually a shield pin but must be connected to the appropiate level to facilitate parity.

V_{CC}REF **V_{CC} Reference:** Positive supply reference for input buffers.

Truth Tables

Recall that all inputs are registered by a rising clock edge. The following truth tables illustrate device operation if the inputs shown are registered; the outputs shown will appear at access time.

NORMAL OPERATIONS

Normal operations are defined by SE = low for prior and current cycle.

Inputs								Outputs		Type of Operation
$\overline{CKE}$	$\overline{S}$	$\overline{W}$	A	AP	PM	D	Data Parity	Q	QEP	
H	X	X	X	X	X	X	(X)	NC	NC	No Operation
L	L	H	V	O	L	X	(X)	V	L	Read
L	L	H	V	E	H	X	(X)	V	L	Read
L	H	H	X	X	X	X	(X)	L	L	Deselect
L	L	H	V	E	L	X	(X)	V	H	Read, A Parity Error
L	L	H	V	O	H	X	(X)	V	H	Read, A Parity Error
L	L	L	V	O	L	V	(O)	NC	L	Write
L	L	L	V	E	H	V	(O)	NC	L	Write
L	H	L	X	X	X	X	(X)	NC	L	Write Inhibit
L	L	L	V	E	L	V	(O)	NC	H	Write, A Parity Error
L	L	L	V	O	H	V	(O)	NC	H	Write, A Parity Error
L	L	L	V	O	L	V	(E)	NC	H	Write, D Parity Error
L	L	L	V	E	H	V	(E)	NC	H	Write, D Parity Error

Special Characters: O = Odd, E = Even, NC = No Change

SCAN MODE OPERATION

Scan operation depends on current and prior states of SE (as registered by the rising edge of the clock), and on the state of the $\overline{CKE}$ bit after scan is completed (as scanned in serially):

Inputs				Outputs			Type of Operation
Prior SE	Current SE	Scanned $\overline{CKE}$	DS	QS	Q	QEP	
L	L	X	X	D8	X	X	Normal Operation
L	H	X	X	D7	NC	NC	Enter scan mode and do first shift
H	H	X	V	V	NC	NC	Serial shift on each clock
H	L	L	X	V	V/NC	V/NC	Exit scan mode; do last shift and then execute instruction scanned into input register; if read or deselect Q and QEP will update, else no change
H	L	H	X	V	V	V	Exit scan mode; do last shift and then copy scan register into Q and QEP; do not execute input instruction

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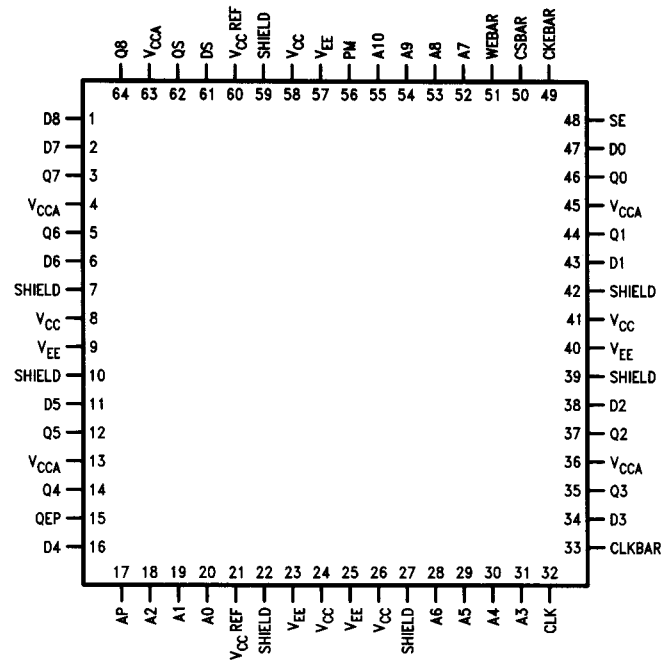
Connection Diagram

Pin Out



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Top View

Note: Pin 26 is reserved for (A11).
Pin 57 is reserved for (A12).

Absolute Maximum Ratings Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C Max
Case Temperature under Bias	0°C to +75°C
V_{EE} Potential (to Ground)	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} − 0.5V to +0.5V
Output Current (DC, High)	−50 mA Max

Power consumption of the device is primarily a function of the clock frequency. Linear derating of the operating current specified less the quiescent current specified by 1.25 mA/MHz will result in a reasonable approximation at the frequency of interest (lower frequency results in lower power).

Operating Voltage

Device	Voltage
NM4492	V_{EE} = −5.2V ±5%
NM100492	V_{EE} = −4.2V to −4.8V

DC Characteristics T_C = 0°C to +75°C

Symbol	Parameter	Conditions	Min	Max	Units
I_{EEO}	Operating Current (−5)	T_{CHCH} = 5 ns	−500		mA
I_{EEO}	Operating Current (−7)	T_{CHCH} = 7 ns	−400		mA
I_{EEO}	Operating Current (−10)	T_{CHCH} = 10 ns	−330		mA
I_{EEQ}	Quiescent Current	Clock = V_{IL}/V_{IH}	−120		mA
I_{IL}	Input Low Current		−50	+170	μA
I_{IH}	Input High Current			+220	μA
V_{OH}	Output HIGH Voltage	50Ω to −2V	−1025	−880	mV
V_{OL}	Output LOW Voltage	50Ω to −2V	−1810	−1620	mV
V_{OHC}	Output HIGH Corner V	50Ω to −2V	−1025		mV
V_{OLC}	Output LOW Corner V	50Ω to −2V		−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV

Read Cycle

DESCRIPTION

A read cycle is performed when the following conditions are present at the time the clock rising edge registers the inputs: $\overline{CKE}$ = Low, $\overline{S}$ = Low, $\overline{W}$ = High, SE = Low and was low for the previous cycle also. At access time the outputs become valid, making a single glitch free transition from the previous state to the new state. A deselect read cycle is very similar to a read cycle except that $\overline{S}$ = High, and the outputs all go inactive (low) at access time. The minimum read cycle time realized in an application is largely a function of the system skews between inputs, and of setup and hold requirements of the device to which the RAM provides data. If the address field and address parity bit combine to parity then the parity error output will not assert, remaining low. The parity error output timing closely approximates access time and meets the same specifications.

AC Characteristics

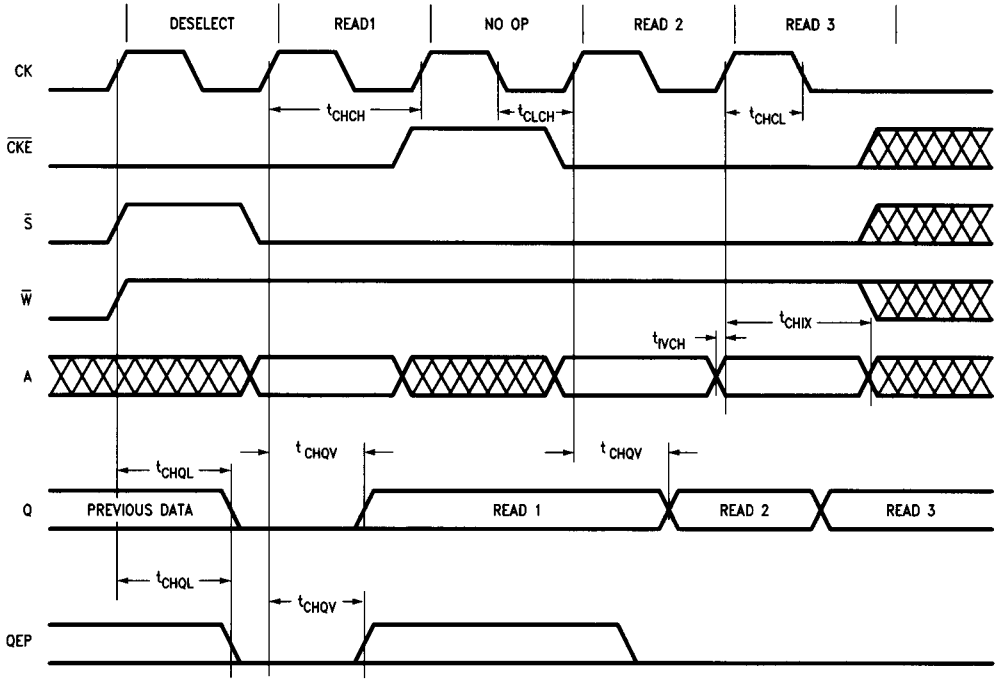
T_C = 0°C to +75°C. Input levels are −0.9V and −1.7V. Timing References are −1.3V (Note 1).

Symbol	Parameter	5 ns (Prelim)		7 ns Device		10 ns Device		Units
		Min	Max	Min	Max	Min	Max	
t_{CHCH}	Cycle Time	5		7		10		ns
t_{CHQV}	Access Time (Note 2)	2.5	5	2.5	7	2.5	10	ns
t_{CHQL}	Disable Time	2.5	5	2.5	7	2.5	10	ns
t_{IVCH}	Input Setup Time	0		0		0		ns
t_{CHIX}	Input Hold Time	2		2.5		3		ns
t_{CHCL}	Clock High Pulse Width	1.5		1.5		2		ns
t_{CLCH}	Clock Low Pulse Width	1.5		1.5		2		ns
t_{CHQEPV}	Parity Access (Note 2)	2.5	5	2.5	7	2.5	10	ns

Output Load: 3.0 pF and 50Ω to −2.0V

Note 1: All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.

Note 2: Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



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Write Cycle

DESCRIPTION

A write cycle is performed when the following conditions are present at the time the clock rising edge registers the inputs: $\overline{CKE}$ = Low, $\overline{S}$ = Low, $\overline{W}$ = Low, SE = Low and was low for the previous cycle also. The minimum write cycle time realized in an application is largely a function of the system skews on the inputs. Notice that a write cycle will not cause a change in any output except the parity error output; data outputs remain unchanged in any case. During writes parity is checked on both the address field (combined with the address parity input) and the data field. The parity error output will not assert if both fields show parity. The parity error output timing closely approximates access time and meets the same access time specifications.

AC Characteristics

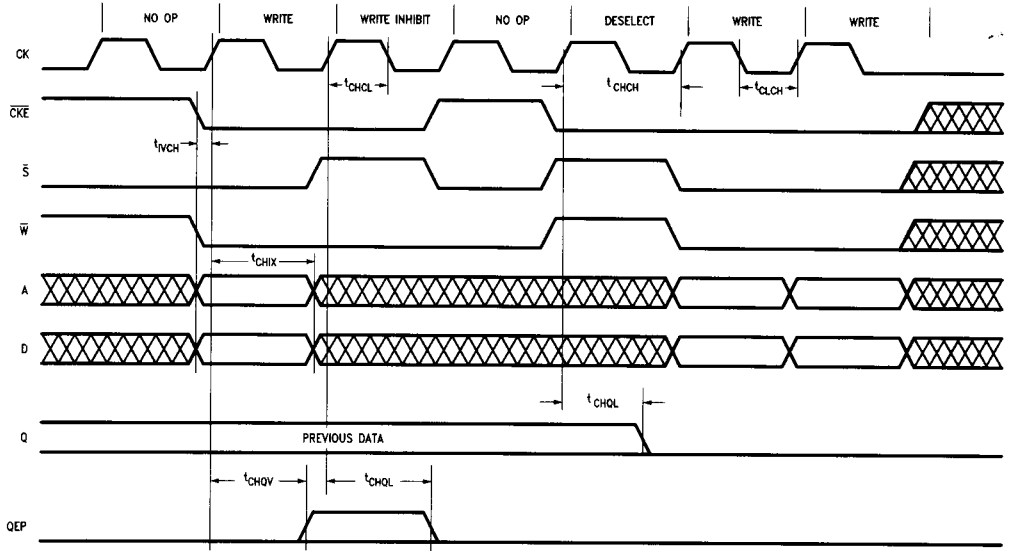
T_C = 0°C to +75°C. Input levels are −0.9V and −1.7V. Timing References are −1.3V (Note 1).

Symbol	Parameter	5 ns (Prelim)		7 ns Device		10 ns Device		Units
		Min	Max	Min	Max	Min	Max	
t_{CHCH}	Cycle Time	5		7		10		ns
t_{IVCH}	Input Setup Time	0		0		0		ns
t_{CHIX}	Input Hold Time	2		2.5		3		ns
t_{CHCL}	Clock High Pulse Width	1.5		1.5		2		ns
t_{CLCH}	Clock Low Pulse Width	1.5		1.5		2		ns
t_{CHQV}	Parity Access Time	2.5	5	2.5	7	2.5	10	ns
t_{CHQL}	Disable Time	2.5	5	2.5	7	2.5	10	ns

Output Load: 3.0 pF and 50Ω to −2.0V

Note 1: All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.

Note 2: Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



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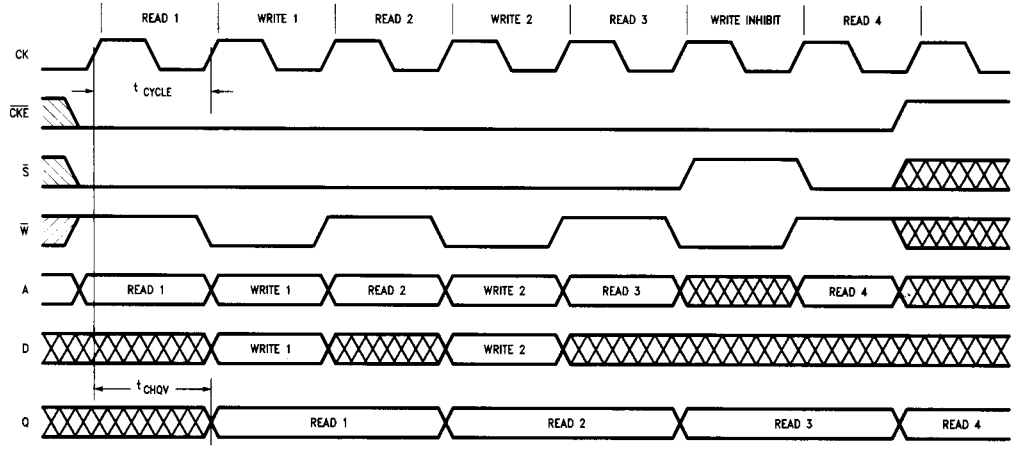
Hidden Write Cycle

The hidden write cycle allows the SRAM to be operated at twice the bandwidth of the data output bus. With relaxed data bus timing (relative to the SRAM address & control input timing) system constraints of setup and hold times may be much more easily met. Hidden write is a technique for interleaving read and write cyles in such a way that the write cycle timing has no effect on the data output bus (read timing). To allow hidden write operation the definition of the functions performed by select ($\overline{S}$) and write ($\overline{W}$) are subtly but importantly different than implemented on common SRAMs.

With hidden write timing there are no unusual restrictions. Consecutive read and write cycles may be at different or at the same address location. If a read is not desired at any given moment a read deselect or a no op may be executed instead. Similarly, if a write is unnecessary a write inhibit or no op may be substituted.

Hidden write can provide throughput enhancement in certain cases. If, for example, the RAM is utilized as a register file, and provides data to a pipelined ALU implemented in a gate array. If the ALU data input register requires 3 ns setup and 3 ns hold, the total data input window required is 4 ns wide. The SRAM maximum access is 7 ns, and the minimum access time is 2.5 ns; the difference is the guaranteed data output valid window. In this example the SRAM must be operated at greater than 9 ns cycle time to allow room for data and clock skews. Depending on system details maybe 10 or 11 ns cycle could be practical. In contrast, using hidden write timing the memory could be run at 7 ns cycles with the data output bus cycle times of 14 ns, easing the ALU setup and hold times while allowing a store and a fetch every 14 ns.



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Scan Mode

DESCRIPTION

The scan mode allows serial input and output for diagnostics or for loading RAM (e.g., in a writable control store application). In overview:

1. The first clock cycle with scan active (SE = High) causes the device to enter scan mode and serially shift.
2. Succeeding clock cycles with scan active cause serial shifting, and
3. The first clock cycle with scan inactive (SE = Low) causes the device to shift and then execute (conditionally) either the scanned in instruction or to force the outputs to a scanned in test vector (see truth table).

Several devices can be linked serially in a scan chain. A detailed description follows:

1. Scan bits are transferred from the input register to the scan serial register at the end of every regular read or write cycle. The device also transfers a fixed scan signature into the remaining bits of the serial scan register in preparation to also shift this data out (the remaining bits are those bits of the serial shift register which correspond with the output register).
2. On the first and each succeeding clock rising edge with scan active (SE = High) the device will shift the serial shift register one bit.
   A. The state of DS is shifted into the chain.
   B. The last bit of the chain is shifted out on QS.
   C. The other outputs remain unchanged. The rest of the RAM executes a no operation. It will not write regardless of the state of the bit in the WE location of the input register.
   D. Any number of shifts can occur in scan mode; two to infinite shifts are possible.
3. The first rising clock edge with scan inactive (SE = Low) causes the device to shift the scan chain and exit scan mode and to conditionally either:
   A. Execute the scanned in instruction (e.g., read, write, deselect) with normal timing response (access, cycle) only if the scanned in bit in the $\overline{CKE}$ location of the input register is active ($\overline{CKE}$ = Low). The output may be affected, according to the instruction executed. The contents of the scan register bits corresponding to the output register are ignored.
   Or:
   B. Transfer the contents of the scan register into the output buffer, and ignore the contents of the input register, only if the scanned in bit in the $\overline{CKE}$ location of the input register is inactive ($\overline{CKE}$ = High).
4. The second and succeeding clock cycles after scan is inactive (SE = Low) are defined as normal mode operations and do not cause any scan functions.

The scan sequence is:

Input DS

to Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, QEP,

to AP, A2, A1, A0, A6, A5, A4, A3, A10, A9, A8, A7,

to $\overline{WE}$, $\overline{CS}$, $\overline{CKE}$,

to D0, D1, D2, D3, D4, D5, D6, D7, D8,

to QS Output

The scan logic is designed to output a sequence of bits recognizable as a scan signature, intended as an aid in fault detection in those cases where the fault causes a malfunction in the serial scan chain. This bit sequence can be easily recognized by the scan diagnostics processor as it is shifted out, providing a reasonably sure method of determining where and/or if the serial scan chain is defective. The scan signature bit sequence corresponds to the outputs:

Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	QEP
H	L	L	H	L	H	L	H	H	L

AC Characteristics

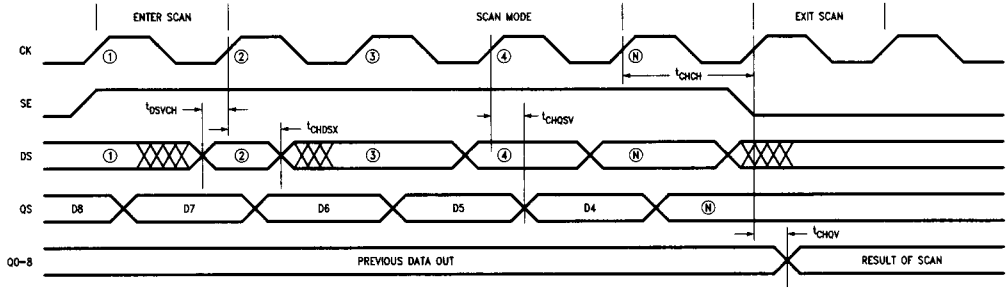
T_C = 0°C to +75°C. Input levels are −0.9V and −1.7V. Timing References are −1.3V (Note 1).

Symbol	Parameter	5 ns (Prelim)		7 ns Device		10 ns Device		Units
		Min	Max	Min	Max	Min	Max	
t_{CHCH}	Serial Scan Mode Cycle Time	5		7		10		ns
t_{DSVCH}	Serial Data Setup Time	0		0		0		ns
t_{CHDSX}	Serial Data Hold Time	2.0		2.5		3		ns
t_{CHQSV}	Serial Output Delay Time (Note 2)	2.5	5	2.5	7	2.5	10	ns

Output Load: 3.0 pF and 50Ω to −2.0V

Note 1: All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.

Note 2: Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



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