FUJITSU MICROELECTRONICS
DATA SHEET

DS04-29138-3E

ASSP

Spread Spectrum Clock Generator

MB88182

■ DESCRIPTION

MB88182 is the multi-output clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator.
It is possible to set the frequency in the built-in register using the I^2C bus that can vary depending on the application.

■ FEATURES

- Built-in PLL : 3
  Without spread-spectrum function : 1 (PLL)
  With spread-spectrum function : 2 (SSCG1, SSCG2)

- Clock output pins : 5 pins
  CLK1 : Clock output when setting to CLK1 (PLL).
  CLK2 : Clock output when setting to CLK2 (SSCG1) .
  CLK3 : Clock output when setting to CLK3 (SSCG2) .
  CLK4 : Clock output when setting to CLK4 (SSCG2) .

Note: It is not possible to output CLK3 and CLK4 at the same time.
CKREF : Buffered output for CKIN clock.

- Power down pins : 5 pins
  XPD1 : Control the stop state of PLL and the CLK1 output.
  XPD2 : Control the stop state of SSCG1 and the CLK2 output.
  XPD3 : Control the stop state of the CLK3 output.
  XPD4 : Control the stop state of the CLK4 output.

Note: Halting both CLK3 and CLK4 stops operating the SSCG2.
XPDREF: Control the stop state of the CKREF output.

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- Modulation enable pins : ENS
  Switch on and off for the modulation (For SSCG1, SSCG2)

- Function to set the output clock frequency
  This has the slave transfer function for the I²C bus, and can set the output frequency of CLK1 (when setting to CLK1), CLK2 (when setting to CLK2), CLK3 (when setting to CLK3) and CLK4 (when setting to CLK4) from the outside.
  Also, it is possible to set the output drive ability of CLK1, CLK2, CLK3 and CLK4.
  Output frequency* : 8 MHz to 100 MHz, internal oscillation frequency : 16 MHz to 168 MHz

*: When VDP is 1.8 V ± 0.15 V, the frequency range to output is 8 MHz to 50 MHz.

Programmable of the parameter of N divider, M divider, K divider
Setting to CLK1 : N divider : 5-bit, M divider : 6-bit, K divider : 5-bit
Setting to CLK2, 3, 4 : N divider : 11-bit, M divider : 12-bit, K divider : 5-bit
Modulation rate : Selectable from no modulation, ±0.25%, ±0.5%, ±0.75%, ±1.0%, ±1.25%, ±1.5% and ±1.75%.

- Input clock 10 MHz to 30 MHz
- Power supply voltage: 1.8 V ± 0.15 V (VDD), 2.6 V ± 0.1 V (VDDE), 1.65 V to 2.7 V (VDP)
- Operating temperature: − 40 °C to + 85 °C
- Power consumption: At operation 18 mW (Power supply voltage:1.8 V (VDD), 2.6 V (VDDE, VDP) normal temperature, no load, CKREF(19.2 MHz), CLK1 (48 MHz, 1.8 V), CLK2 (27 MHz), CLK3 (37 MHz) during the clock output)
  During the power down state for all outputs 0.01 mW (Power supply voltage: 1.8 V (VDD) , 2.6 V (VDDE, VDP), normal temperature)
- Cycle-Cycle Jitter : Less than 100 ps-rms
- Package : BCC20 (3.50 mm × 3.50 mm, Lead pitch 0.50 mm, Mounting height 0.60 mm)
  QFN24 (2.50 mm × 3.50 mm, Lead pitch 0.40 mm, Mounting height 0.80 mm)

■ PRODUCT LINEUP

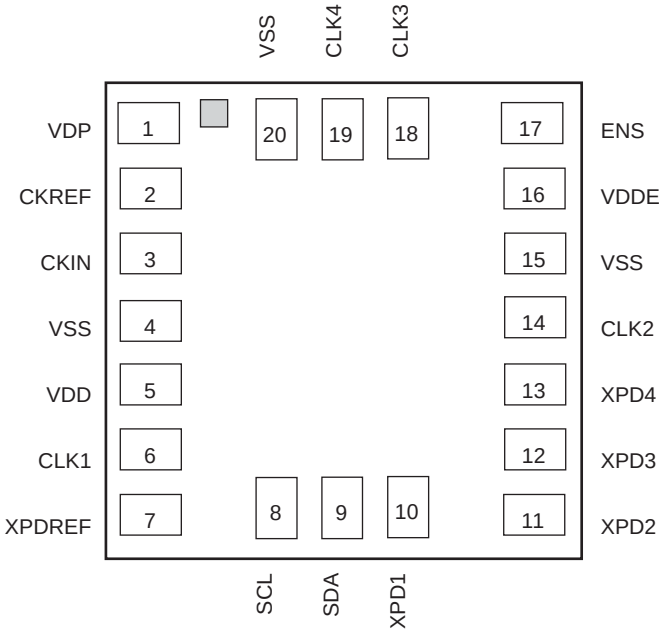
MB88182 has the following lineups corresponding to the different voltages of CLK1 pin and I²C addresses.

Part number		CLK1	CLK2	CLK3/CLK4/CKREF	I²C address
BCC20 package	QFN24 package				
MB881821APVA1	MB881821AWQN	1.8 V	2.6 V	VDP level (1.8 V / 2.6 V)	1001111_B
MB881822APVA1	MB881822AWQN	2.6 V			
MB881821BPVA1	MB881821BWQN	1.8 V			1011111_B
MB881822BPVA1	MB881822BWQN	2.6 V			

■ PIN ASSIGNMENT

• BCC20

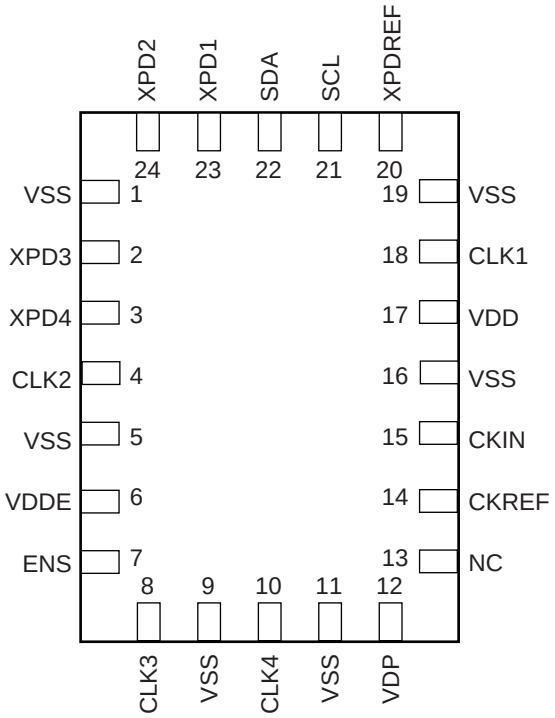
(TOP VIEW)



(LCC-20P-M06)

• QFN24

(TOP VIEW)

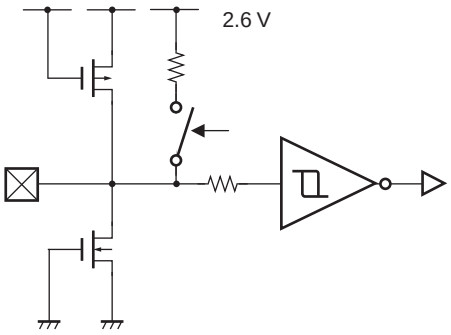
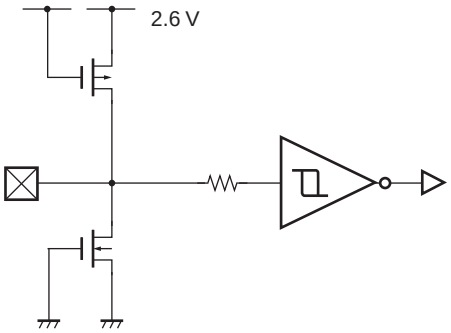
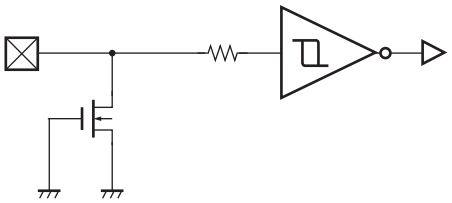
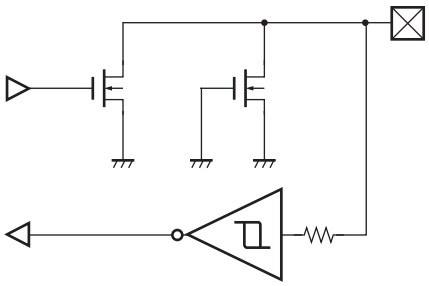


(LCC-24P-M61)

■ PIN DESCRIPTION

Pin name	I/O	Pin no.		Description
		BCC20	QFN24	
VDP	—	1	12	Power supply pin (2.6 V / 1.8 V)
NC	—	—	13	NC pin
CKREF	O	2	14	Reference clock output pin
CKIN	I	3	15	Clock input pin (19.2 MHz)
VSS	—	4	16	GND pin
VDD	—	5	17	Power supply pin (1.8 V)
CLK1	O	6	18	Clock output pin 1
VSS	—	—	19	GND pin
XPDREF	I	7	20	CKREF Power down pin
SCL	I	8	21	I^2C bus clock input pin
SDA	I/O	9	22	I^2C bus data I/O pin
XPD1	I	10	23	CLK1 Power down pin
XPD2	I	11	24	CLK2 Power down pin
VSS	—	—	1	GND pin
XPD3	I	12	2	CLK3 Power down pin
XPD4	I	13	3	CLK4 Power down pin
CLK2	O	14	4	Clock output pin 2
VSS	—	15	5	GND pin
VDDE	—	16	6	Power supply pin (2.6 V)
ENS	I	17	7	Modulation enable pin
CLK3	O	18	8	Clock output pin 3
VSS	—	—	9	GND pin
CLK4	O	19	10	Clock output pin 4
VSS	—	20	11	GND pin

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
XPDREF XPD1 XPD2 XPD3 XPD4		• CMOS hysteresis input • With pull-up resistor (20 kΩ) The pull-up resistor is cut off during the “L” input.
ENS		CMOS hysteresis input
SCL		CMOS hysteresis input
SDA		• CMOS hysteresis input • N-ch open drain output • I_{OL} = 4 mA

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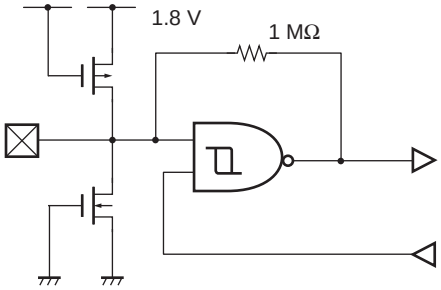
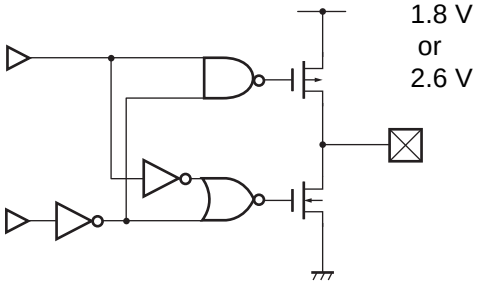
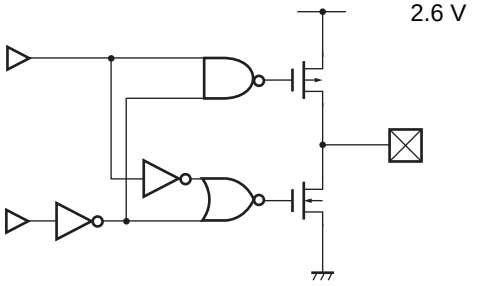
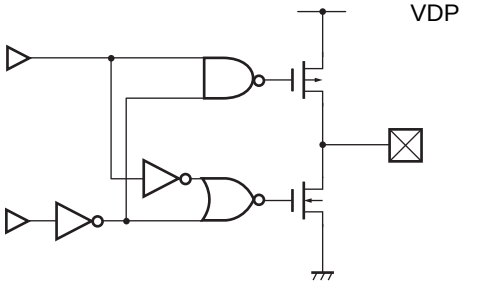
Pin	Circuit type	Remarks
CKIN		• Feedback resistors 1 MΩ • Possible to input clock via the coupling capacity
CLK1		• CMOS output • I_{OH} = – 2 mA or – 4 mA • I_{OL} = 2 mA or 4 mA (Switchable by the output drive ability setting bit) • Operates at 1.8 v or 2.6 v depending on the part number.
CLK2		• CMOS output • I_{OH} = – 2 mA or – 4 mA • I_{OL} = 2 mA or 4 mA (Switchable by the output drive ability setting bit)
CLK3 CLK4		• CMOS output • At VDP = 2.6 V ± 0.1 V I_{OH} = – 2 mA or – 4 mA I_{OL} = 2 mA or 4 mA (Switchable by the output drive ability setting bit) • At VDP = 1.8 V ± 0.15 V I_{OH} = – 1 mA or – 2 mA I_{OL} = 1 mA or 2 mA

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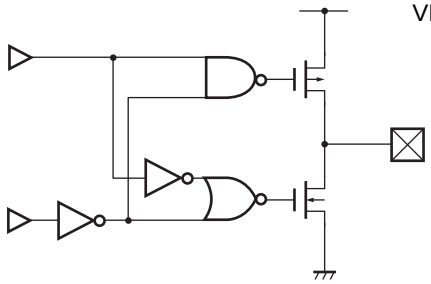
Pin	Circuit type	Remarks
CKREF		• CMOS output • At VDP = 2.6 V ± 0.1 V I_{OH} = – 2 mA I_{OL} = 2 mA • At VDP = 1.8 V ± 0.15 V I_{OH} = – 1 mA I_{OL} = 1 mA

■ HANDLING DEVICES

(1) Preventing latch-up

A latch-up may occur in a CMOS IC if a voltage greater than power supply voltage or a voltage less than GND is applied to an input or output pin, or if an above-rating voltage is applied between power supply and GND. A latch-up, if it occurs, significantly increases the power-supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the absolute maximum rating.

(2) Handling control input pins

The input pins (ENS, XPD1, XPD2, XPD3, XPD4, and XPDREF) of this device should be high or low level preventing the pins from being undefined by connecting a pull-down or pull-up resistor, or performing level input by control signals.

The wait time for clock stabilization is needed after turning the power on or when changing the setting of ENS pin or power down control pins (XPD1, XPD2, XPD3, XPD4, and XPDREF). Please use the clock after the lock-up time has passed. (The lock-up time varies depending on the setting value to the respective register. Please confirm the recommended value with the Fujitsu Microelectronics support tool.)

(3) Power supply pins

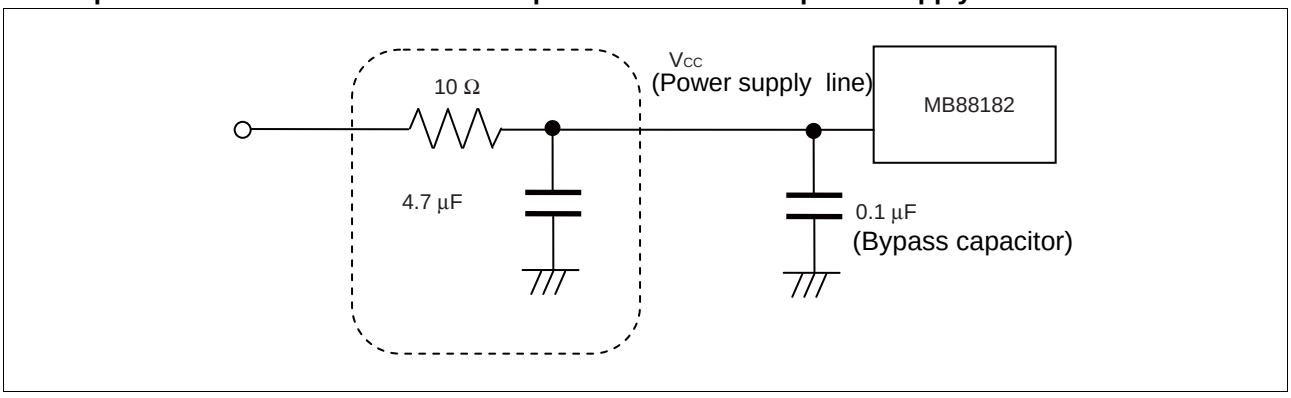
Ensure that the impedance of the connection from the power supply source to the power supply pins on the device is as low as possible.

We recommend connecting the electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between power supply and GND near the device, as a bypass capacitor.

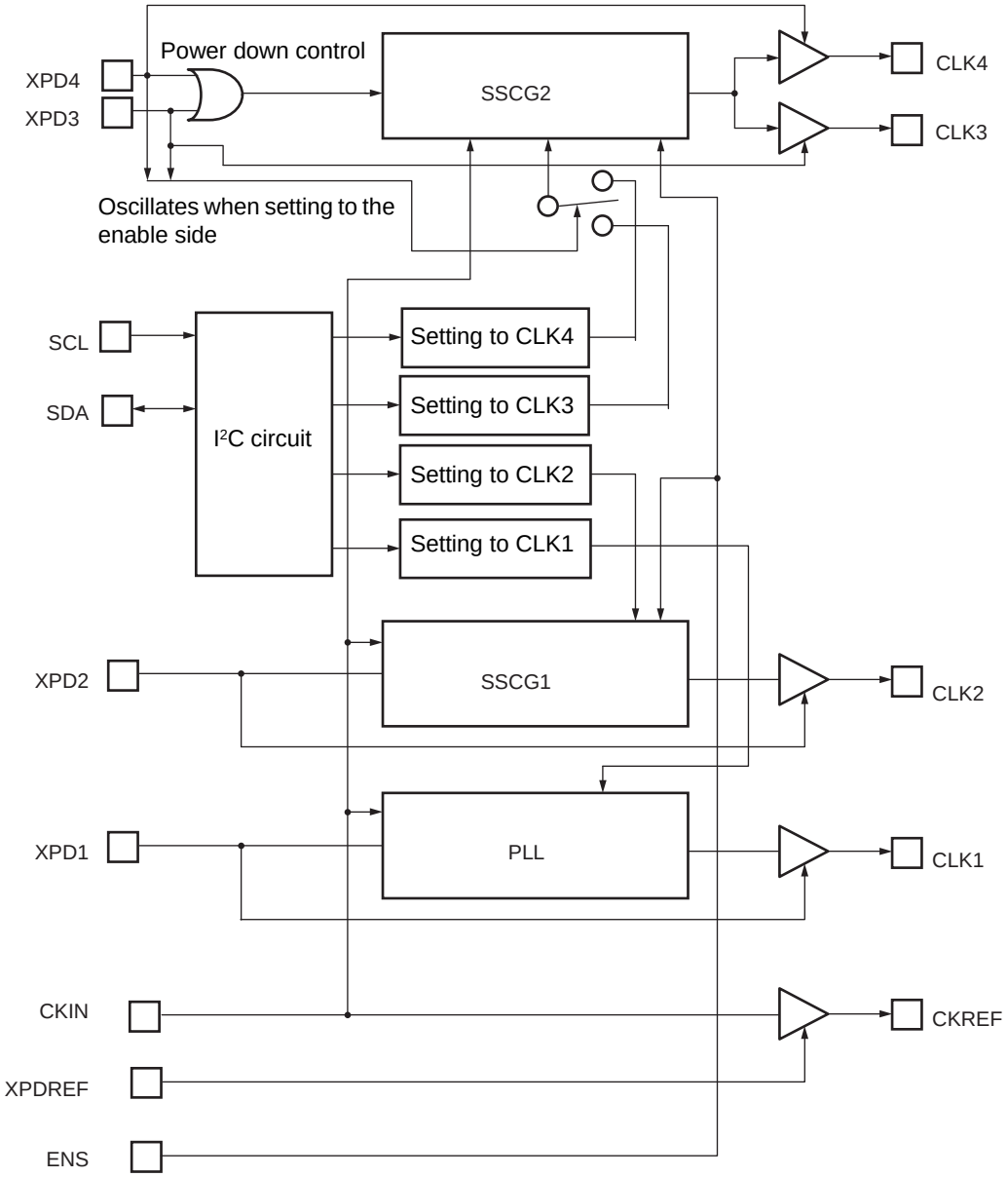
We also recommend inserting a low pass filter less than 3.4 kHz of a cutoff frequency to the power-supply line of MB88182 for not being affected by the power-supply noise on the customer's system.

The supply voltage to MB88182 is decreased when a resistor is inserted; therefore, please use the resistor less than 10 Ω in case of inserting a resistor. (An example of recommended combination is 4.7 μF for a capacitance and 10 Ω for a resistor.)

- **Example of recommended circuit of low pass filter to remove power-supply noise**



■ BLOCK DIAGRAM



■ PIN SETTING

ENS Modulation enable setting

ENS	Modulation
0	No modulation
1 (2.6 V)	Modulation

When setting “0” to the ENS pin, the spectrum will not spread.
The setting is for CLK2 (SSCG1) and CLK3, and CLK4 (SSCG2).

XPD Power down setting

XPDREF	0	CKREF is fixed to the output “L”.
	1 (2.6 V)	CKREF is the clock output.
XPD1	0	PLL1 is in the power down state. CLK1 is fixed to the output “L”.
	1 (2.6 V)	PLL1 and CLK1 are in operation.
XPD2	0	SSCG1 is in the power down state. CLK2 is fixed to the output “L”.
	1 (2.6 V)	SSCG1 and CLK2 are in operation.
XPD3	0	CLK3 is fixed to the output “L”.
	1 (2.6 V)	SSCG2 and CLK3 are in operation.
XPD4	0	CLK4 is fixed to the output “L”.
	1 (2.6 V)	SSCG2 and CLK4 are in operation.

The pin in XPDREF, XPD1, XPD2, XPD3 and XPD4 is connected to the pull-up resistor.
However, the pull-up resistor is cut off during “0” input.
When both XPD3 and XPD4 are “0”, SSCG2 is in the power down state.

■ SETTING REGISTER

<Memory map>

Setting register for CLK2, CLK3, CLK4 (All registers have the same configurations.)

Address	Function	Remarks
bit0 to 11	M divider setting (12-bit)	Selectable in the range of 100 to 3600
bit12 to 22	N divider setting (11-bit)	Selectable in the range of 3 to 2047
bit23 to 27	K divider setting (5-bit)	Selectable in the range of 1 to 32
bit28 to 30	L divider setting (3-bit)	Modulation frequency setting (selectable in the range of 1 to 8)
bit31 to 34	Charge Pump setting (4-bit)	Charge pump current setting due to internal oscillation frequency and M divider setting
bit35 to 40	VCO Gain setting (6-bit)	Gain setting due to internal oscillation frequency
bit41 to 43	Modulation rate setting (3-bit)	modulation off, ± 0.25%, ± 0.50%, ± 0.75%, ± 1.00%, ± 1.25%, ± 1.50%, ± 1.75% are selectable
bit44	Output drive setting	0 : Ability small, 1 : Ability large
bit45	Slewing rate setting	0 : Slewing rate low, 1 : Slewing rate high
bit46, 47	Invalid bit	When in writing : The written data is ignored. When in reading : Undefined

CLK1 setting register

Address	Function	Remarks
bit0 to 5	M divider setting (6-bit)	Selectable in the range of 3 to 52
bit6 to 10	N divider setting (5-bit)	Selectable in the range of 3 to 31
bit11 to 15	K divider setting (5-bit)	Selectable in the range of 1 to 32
bit16 to 19	Charge Pump setting (4-bit)	Charge pump current setting due to internal oscillation frequency and M divider setting
bit20 to 25	VCO Gain setting (6-bit)	Gain setting due to internal oscillation frequency
bit26	Output drive setting	0 : Ability small, 1 : Ability large
bit27	Slewing rate setting	0 : Slewing rate low, 1 : Slewing rate high
bit28 to 31	Invalid bit	When in writing : The written data is ignored. When in reading : Undefined

Note: The bit's initial value in a register is undefined. Therefore, if the power down of clock output is released before the register setting, the clock is output with settings unintended. The power down of the clock output for CLK1, CLK2, CLK3 and CLK4 should be released after setting to registers.

<Frequency setting>

When setting each divider parameter of the oscillator to a register, the output frequency can be set.
Internal oscillation frequency and output frequency can be calculated with following formula:

Internal oscillation frequency (fvco*) = Input frequency (fin) × M/N

* : Please set the fvco range from 16 MHz to 168 MHz.

Output frequency (fout*) = fvco/K

* : Please set the fout range from 8 MHz to 100 MHz.

Set the output frequency to 8 MHz to 50 MHz for CLK3 and CLK4 setting registers when VDP is 1.8 V ± 0.15 V.

(Setting example)

fin : 19.2 MHz, fout : 29.6 MHz

M divider parameter : 222 (= $0DE_H$) , N divider parameter : 144 (= 090_H) , K divider parameter : 1 (= 01_H)

(19.2 × 222 / 144) / 1 = 29.6 (MHz) (fvco : 19.2 × 222 / 144 = 29.6 (MHz))

Note: The recommended setting value of the VCO gain and the M divider depends on the internal oscillation frequency.
Also, the recommended setting value of the Charge Pump depends on the setting values of the VCO gain and the M divider. Please confirm the recommended value with the Fujitsu Microelectronics support tool.
Contact the sales representatives for details on the support tools.

<Modulation frequency setting>

Modulation frequency can be set by writing L divider parameter to the register.

The average of modulation frequency can be calculated with following formula:

$$\frac{\text{Input frequency}}{266 \times L} \quad (L = 1, 2, 3, 4, 5, 6, 7, 8)$$

(Setting example) fin : 19.2 MHz, average of modulation freq. 19.2 / (266 × 6) × 1000 = Approximately 12.0 (kHz)

bit30	bit29	bit28	L divider parameter
0	0	0	8
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6 (Recommended value)
1	1	1	7

<Modulation rate setting>

Modulation rate can be selectable from no modulation, ± 0.25%, ± 0.50%, ± 0.75%, ± 1.00%, ± 1.25%, ± 1.50%, ± 1.75%.

bit43	bit42	bit41	Modulation rate setting
0	0	0	No modulation
0	0	1	± 0.25%
0	1	0	± 0.50%
0	1	1	± 0.75%
1	0	0	± 1.00%
1	0	1	± 1.25%
1	1	0	± 1.50%
1	1	1	± 1.75%

<Charge Pump setting, VCO gain setting>

Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

<Output drive ability setting>

Output drive ability of clock output pin can be selected.

bit44	Output drive ability
0	Small
1	Large

<Slew rate setting>

Slew rate of clock output pin can be selected.

bit45	Slew rate
0	Low
1	High

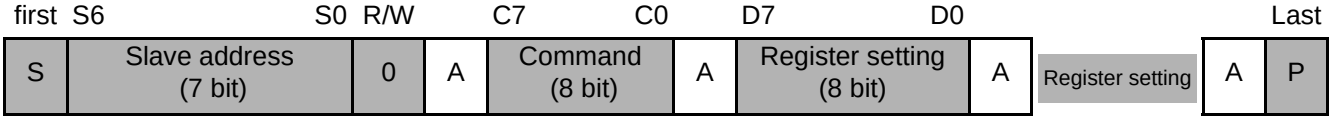
■ I²C

This device contains the I²C macro and enables the slave transfer operation. The I²C is set to the corresponding registers via the I²C bus.

<Bus specification>

- The transfer rate should be in either standard mode or the fast mode (The high speed mode is not supported) .
- 7-bit address specified (The general call and the 10-bit address specifications are not supported).

<Bus format when writing register>



: Transmit from master device : Transmit from this device (slave)

S : START condition A : Acknowledge P : STOP condition

<Slave address>

When receiving the slave address, the address is compared with the address in the following table. If the slave address matches the address in the table only, I²C judges to access to this device.

Slave address (7-bit)							
S6	S5	S4	S3	S2	S1	S0	Part number
1	0	0	1	1	1	1	MB881821APVA1/MB881822APVA1
1	0	1	1	1	1	1	MB881821BPVA1/MB881822BPVA1

<Select R/W>

“0” : Write to slave device
“1” : Read from slave device

<Command>

Set for the CLK2, CLK3 and CLK4 setting registers with either individual or successive settings. Settings other than those in the following table are prohibited.

Command (8-bit)									
C7	C6	C5	C4	C3	C2	C1	C0	Transfer bytes	
0	0	0	0	0	0	0	1	4	Set to CLK1 setting register
0	0	0	0	0	0	1	0	6	Set to CLK2 setting register
0	0	0	0	0	1	0	0	6	Set to CLK3 setting register
0	0	0	0	1	0	0	0	6	Set to CLK4 setting register
0	0	0	0	1	1	1	1	22	Successive set to all registers
0	0	0	0	Other than “0000” or those above				10 to 18	Successive set to the register corresponding to the bit which is set “1”.

<Register setting for writing data>

Transfer data from the upper address. When writing successively to the setting registers of multiple clocks, the data will be written from the setting registers CLK1, CLK2, CLK3 and to CLK4 in order.

<Bus format for reading register>

first	S6	S0	R/W	D7	D0	D7	D0		Last	
S	Slave address (7 bit)	1	A	CLK1 setting register bit31-24 output	A	CLK1 setting register bit23-16 output	A	output register values	A	P

▮ : Transmit from master device ▯ : Transmit from this device (slave)

S : START condition A : Acknowledge P : STOP condition

When reading data, the data will be output from the upper address of the CLK1 setting register, then CLK2 setting register, CLK3 setting register, CLK4 setting register, in order. The data will be output 22 bytes in total.

Note: When all outputs in this device are powered down, the I^2C function also stops. Therefore, setting by the I^2C should be performed when the CKREF clock is being output.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Pin	Rating		Unit
			Min	Max	
Power supply voltage*1	V_{DD}	VDD	– 0.5	+ 2.5	V
	V_{DDE}	VDDE	– 0.5	+ 4.0	V
	V_{DP}	VDP	– 0.5	+ 4.0	V
Input voltage*1	V_I	CKIN	V_{SS} – 0.5	V_{DD} + 0.5	V
		XPDREF, XPD1, XPD2, XPD3, XPD4, SCL, SDA	V_{SS} – 0.5	V_{DDE} + 0.5	V
Output voltage*1	V_O	CLK1	V_{SS} – 0.5	V_{DD} + 0.5*2 V_{DDE} + 0.5*3	V
		CLK2, SDA	V_{SS} – 0.5	V_{DDE} + 0.5	V
		CLK3, CLK4, CKREF	V_{SS} – 0.5	V_{DP} + 0.5	V
Storage temperature	T_{ST}	—	– 55	+ 125	°C
Operation junction temperature	T_J	—	– 40	+ 125	°C
Output current	I_O	—	– 13	+ 13	mA
Overshoot	V_{IOVER}	XPDREF, XPD1, XPD2, XPD3, XPD4, SCL, SDA	—	V_{DDE} + 1.0 ($t_{OVER} \leq$ 50 ns)	V
Undershoot	V_{IUNDER}		V_{SS} – 1.0 ($t_{UNDER} \leq$ 50 ns)	—	V

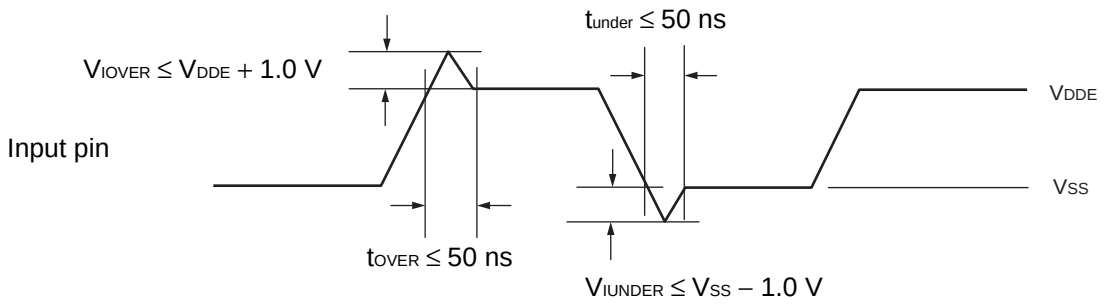
*1 : The parameter is based on V_{SS} = 0.0 V.

*2 : Part number: MB881821A/MB881821B

*3 : Part number: MB881822A/MB881822B

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot / Undershoot



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin	Condition	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	VDD	—	1.65	1.8	1.95	V
	V_{DDE}	VDDE	—	2.5	2.6	2.7	
	V_{DP}	VDP	—	1.65	1.8	1.95	
				2.5	2.6	2.7	
"H" level input voltage	V_{IH1}	CKIN	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
	V_{IH2}	ENS, XPDREF, XPD1, XPD2,XPD3, XPD4	—	$V_{DDE} \times 0.8$	—	$V_{DDE} + 0.3$	
	V_{IH3}	SDA, SCL	—	$V_{DDE} \times 0.7$	—	$V_{DDE} + 0.3$	
"L" level input voltage	V_{IL1}	CKIN	—	Vss – 0.3	—	$V_{DD} \times 0.2$	V
	V_{IL2}	ENS, XPDREF, XPD1, XPD2, XPD3, XPD4	—	Vss – 0.3	—	$V_{DDE} \times 0.2$	
	V_{IL3}	SDA, SCL	—	Vss – 0.3	—	$V_{DDE} \times 0.3$	
Input clock amplitude level	V_{IC}	CKIN	During clock input of capacitive coupling	0.45	—	V_{DD}	V p-p
Input coupling capacity	C_C	— *		20	—	—	pF
Input clock duty cycle	t_{DCI}	CKIN	19.2 [MHz]	40	50	60	%
Operating temperature	T_a	—	—	– 40	—	+ 85	°C

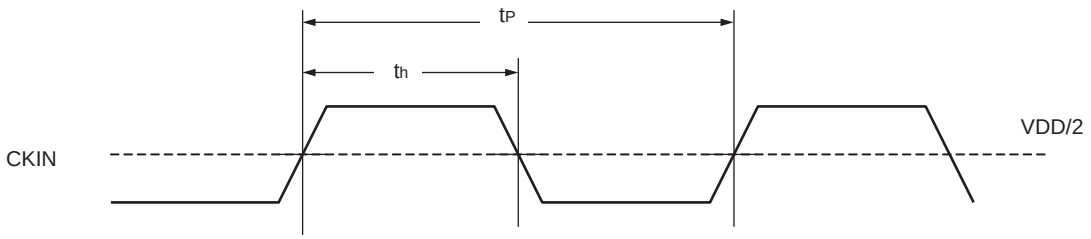
* : Capacity value when clock signal is input to the CKIN pin via coupling capacity.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_h/t_p$)



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

(Ta = − 40 °C to + 85 °C, VDD = 1.8 V ± 0.15 V, VDDE = 2.6 V ± 0.1 V, VDP = 2.6 V ± 0.1 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	VDD*1	CKREF = 19.2 MHz, CLK1 = 48 MHz*2, CLK2 = 27 MHz, CLK3 = 37 MHz, CLK4 output stop, output no load, CKIN direct input	—	7	11	mA
	I_{CCE}	VDDE		—	0.5	—	
	I_{CCP}	VDP		—	0.9	—	
	I_{CCH}	VDD	When all clock output disable	—	2	50	µA
	I_{CCEH}	VDDE		—	1	5	
	I_{CCPH}	VDP		—	1	5	
Output voltage	V_{OH1}	CLK1*3, CLK2, CLK3, CLK4	Driving ability small setting “H” level output I_{OH} = − 2 mA	V_{DDE} − 0.2 V_{DP} − 0.2	—	V_{DDE} V_{DP}	V
	V_{OL1}		Driving ability small setting “L” level output I_{OL} = 2 mA	V_{SS}	—	0.2	
	V_{OH2}		Driving ability large setting “H” level output I_{OH} = − 4 mA	V_{DDE} − 0.2 V_{DP} − 0.2	—	V_{DDE} V_{DP}	
	V_{OL2}		Driving ability large setting “L” level output I_{OL} = 4 mA	V_{SS}	—	0.2	
	V_{OH1}	CKREF	“H” level output I_{OL} = − 2 mA	V_{DP} − 0.2	—	V_{DP}	V
	V_{OL1}		“L” level output I_{OL} = 2 mA	V_{SS}	—	0.2	
	V_{OH3}	CLK1*2	Driving ability small setting “H” level output I_{OH} = − 2 mA	V_{DD} − 0.2	—	V_{DD}	V
	V_{OL3}		Driving ability small setting “L” level output I_{OL} = 2 mA	V_{SS}	—	0.2	
	V_{OH4}		Driving ability large setting “H” level output I_{OH} = − 4 mA	V_{DD} − 0.2	—	V_{DD}	
	V_{OL4}		Driving ability large setting “L” level output I_{OL} = 4 mA	V_{SS}	—	0.2	

(Continued)

(Continued)

(Ta = − 40 °C to + 85 °C, VDD = 1.8 V ± 0.15 V, VDDE = 2.6 V ± 0.1 V, VDP = 2.6 V ± 0.1 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output voltage	V_{OL2}	SDA	"L" level output I_{OL} = 4 mA	V_{SS}	—	0.2	V
Pull-up resistance value*4	R_{PU}	XPDREF, XPD1, XPD2, XPD3, XPD4	$V_{IH} = V_{DDE} \times 0.8$	10	20	30	kΩ
Input capacitance	C_{IN}	CKIN, ENS, XPDREF, XPD1, XPD2, XPD3, XPD4, SDA, SCL	T_a = + 25 °C $V_{DD} = V_{DDE} = V_I$ = 0 V f = 1 MHz	—	—	10	pF

*1 : Excluding power supply current in the CLK1 output

*2 : Part number: MB881821APVA1/MB881821BPVA1

*3 : Part number: MB881822APVA1/MB881822BPVA1

*4 : The pull up resistor for each pin is cut off when the pin input is in "L" level.

(Ta = − 40 °C to + 85 °C, VDP = 1.8 V ± 0.15 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output voltage	V_{OH5}	CLK3, CLK4	Driving ability small setting "H" level output I_{OH} = − 1 mA	V_{DP} − 0.2	—	V_{DP}	V
	V_{OL5}		Driving ability small setting "L" level output I_{OL} = 1 mA	V_{SS}	—	0.2	
	V_{OH6}		Driving ability large setting "H" level output I_{OH} = − 2 mA	V_{DP} − 0.2	—	V_{DP}	
	V_{OL6}		Driving ability large setting "L" level output I_{OL} = 2 mA	V_{SS}	—	0.2	
	V_{OH5}	CKREF	"H" level output I_{OL} = − 1 mA	V_{DP} − 0.2	—	V_{DP}	V
	V_{OL5}		"L" level output I_{OL} = 1 mA	V_{SS}	—	0.2	

• **AC characteristics 1**

(Ta = − 40 °C to + 85 °C, VDD = 1.8 V ± 0.15 V, VDDE = 2.6 V ± 0.1 V, VDP = 2.6 V ± 0.1 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f_{IN}	CKIN	—	10	19.2	30	MHz
Output frequency	f_{OUT}	CKREF	Load capacitance 15 pF or less	10	19.2	30	MHz
		CLK1*1	Load capacitance 15 pF or less	8	—	100	
		CLK1*2, CLK2, CLK3, CLK4	Load capacitance 15 pF or less	8	—	90	
			Load capacitance 10 pF or less	8	—	100	
Output slewing rate	SR	CLK1*1	Slewing rate low, Driving ability small setting 15 pF load capacitance 8 MHz to 70 MHz	0.32	—	—	V/ns
			Slewing rate high, Driving ability small setting 15 pF load capacitance 8 MHz to 70 MHz	0.33	—	—	
			Slewing rate low, Driving ability large setting 15 pF load capacitance 8 MHz to 80 MHz	0.37	—	—	
			Slewing rate high, Driving ability large setting 15 pF load capacitance 8 MHz to 100 MHz	0.43	—	—	

(Continued)

(Ta = − 40 °C to + 85 °C, VDD = 1.8 V ± 0.15 V, VDDE = 2.6 V ± 0.1 V, VDP = 2.6 V ± 0.1 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output slewing rate	SR	CLK1*2, CLK2, CLK3, CLK4	Slewing rate low, Driving ability small setting 15 pF load capacitance 8 MHz to 50 MHz	0.31	—	—	V/ns
			Slewing rate high, Driving ability small setting 15 pF load capacitance 8 MHz to 60 MHz	0.33	—	—	
			Slewing rate low, Driving ability large setting 15 pF load capacitance 8 MHz to 60 MHz	0.46	—	—	
			Slewing rate high, Driving ability large setting 15 pF load capacitance 8 MHz to 90 MHz	0.50	—	—	
			Slewing rate high, Driving ability large setting 10 pF load capacitance 90 MHz to 100 MHz	0.63	—	—	
		CKREF	15 pF load capacitance	0.33	—	—	
Output impedance	Z_O	CLK1*1	Driving ability small setting	—	40	—	Ω
			Driving ability large setting	—	28	—	
		CLK1*2	Driving ability small setting	—	60	—	
			Driving ability large setting	—	30	—	
		CLK2, CLK3, CLK4	Driving ability small setting	—	60	—	
			Driving ability large setting	—	30	—	
		CKREF	—	—	60	—	

(Continued)

(Continued)

(Ta = − 40 °C to + 85 °C, VDD = 1.8 V ± 0.15 V, VDDE = 2.6 V ± 0.1 V, VDP = 2.6 V ± 0.1 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output clock duty cycle	t_{DCC}	CLK1*1	V_{DD} / 2*3	40	—	60	%
			V_{DD} / 2*4	45	—	55	
		CLK1*2	V_{DDE} / 2*3	40	—	60	
			V_{DDE} / 2*4	45	—	55	
		CLK2, CLK3, CLK4	V_{DDE} / 2, V_{DP} / 2*3	40	—	60	
			V_{DDE} / 2, V_{DP} / 2*4	45	—	55	
		CKREF	V_{DP} / 2	t_{DCI} – 5*5	—	t_{DCI} + 5*5	
Modulation frequency	F_{MOD}	CLK2, CLK3, CLK4	—	fin/ (224 × L) (224 × L)	fin/ (266 × L) (266 × L)	fin/ (308 × L) (308 × L)	kHz (clks)
Lock-up time*6	t_{LK}	CLK1	—	—	—	0.3	ms
		CLK2, CLK3, CLK4	—	—	—	16	ms
Cycle-cycle jitter	t_{JC}	CLK1, CLK2, CLK3, CLK4	No load capacitance	—	—	100	ps-rms
CKREF Power down	t_{RPD}	CKREF	—	—	—	$t_P \times 2 + 2$	ns
CKREF Power down release	t_{ROE}	CKREF	—	—	—	$t_P \times 2 + 2$	ns

*1: Part number: MB881821APVA1/MB881821BPVA1

*2: Part number: MB881822APVA1/MB881822BPVA1

*3 : When K divider parameter = 1 and output frequency is above 50 MHz.

*4 : When K divider parameter ≠ 1, or K divider parameter = 1 and output frequency is 50 MHz or less.

*5 : Duty cycle of the CKREF output depends on the t_{DCI}, input clock duty cycle.

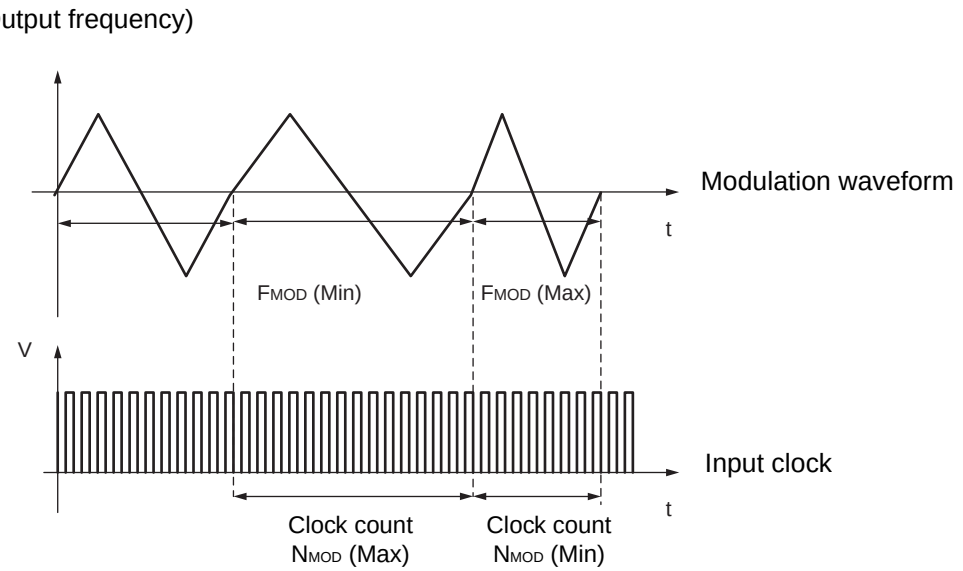
*6 : The wait time for clock stabilization is needed after turning the power on or when changing the setting of ENS/ power down pins. The lock-up time varies depending on the setting value to the respective register. Please confirm the recommended value with the Fujitsu Microelectronics support tool. Contact the sales representatives for details on the support tools.

(Ta = − 40 °C to + 85 °C, VDP = 1.8 V ± 0.15 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output frequency	f_{OUT}	CLK3, CLK4	Load capacitance 10 pF or less	8	—	50	MHz
			Load capacitance 15 pF or less	8	—	40	
Output slewing rate	SR	CLK3, CLK4	Slewing rate low, Driving ability small setting 15 pF load capacitance 8 MHz to 25 MHz	0.13	—	—	V/ns
			Slewing rate high, Driving ability small setting 15 pF load capacitance 8 MHz to 30 MHz	0.14	—	—	
			Slewing rate low, Driving ability large setting 15 pF load capacitance 8 MHz to 30 MHz	0.19	—	—	
			Slewing rate high, Driving ability large setting 15 pF load capacitance 8 MHz to 40 MHz	0.22	—	—	
			Slewing rate high, Driving ability large setting 10 pF load capacitance 8 MHz to 50 MHz	0.29	—	—	
		CKREF	15 pF load capacitance	0.14	—	—	
Output impedance	Z_O	CLK3, CLK4	Driving ability small setting	—	80	—	Ω
			Driving ability large setting	—	40	—	
		CKREF	—	—	80	—	
Output clock duty cycle	t_{DCC}	CLK3, CLK4	V_{DP} / 2	45	—	55	%
		CKREF	V_{DP} / 2	t_{DCI} − 5*	—	t_{DCI} + 5*	
CKREF Power down	t_{RPD}	CKREF	—	—	—	$t_P \times 2 + 2$	ns
CKREF Power down release	t_{ROE}	CKREF	—	—	—	$t_P \times 2 + 2$	ns

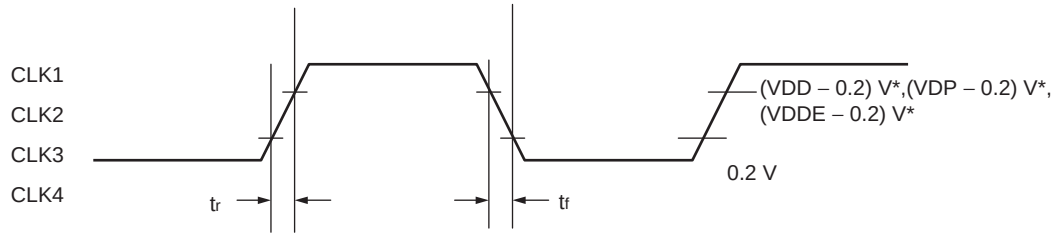
* : Duty cycle of the CKREF output depends on the t_{DCI}, input clock duty cycle.

<Definition of modulation frequency and number of input clocks per modulation>



This product contains the modulation period to realize the efficient EMI reduction.
The modulation period F_{MOD} depends on the input frequency and changes between F_{MOD} (Min) and F_{MOD} (Max). Furthermore, the typical value of the electrical characteristics is equivalent to the average value of the modulation period F_{MOD}.

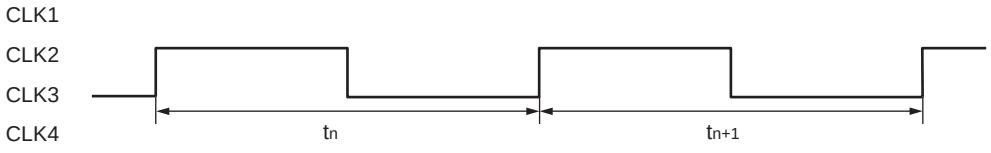
<Output slew rate (SR) >



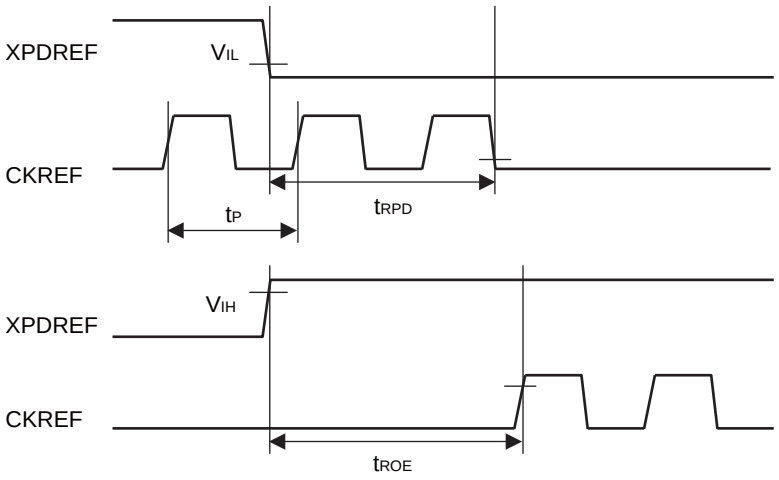
* : The value is differ depending on the power supply pin.
CLK1 : (VDD – 0.2)V or (VDDE – 0.2)V (depending on models)
CLK2 : (VDDE – 0.2)V
CLK3 : CLK4: (VDP – 0.2)V

Note: SR = (power supply voltage – 0.4) / t_r, SR = (power supply voltage – 0.4) / t_f

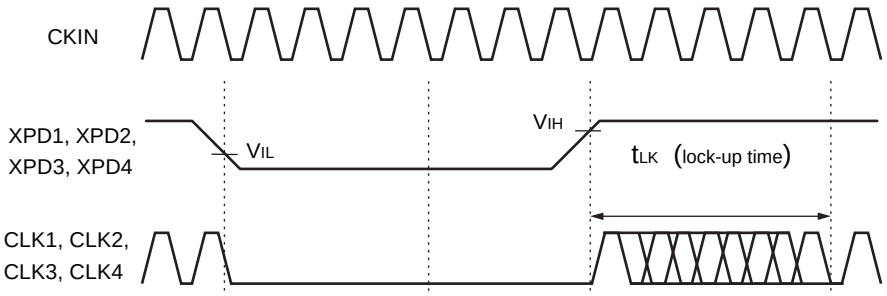
<Cycle-cycle jitter ($t_{JC} = |t_n - t_{n+1}|$)>



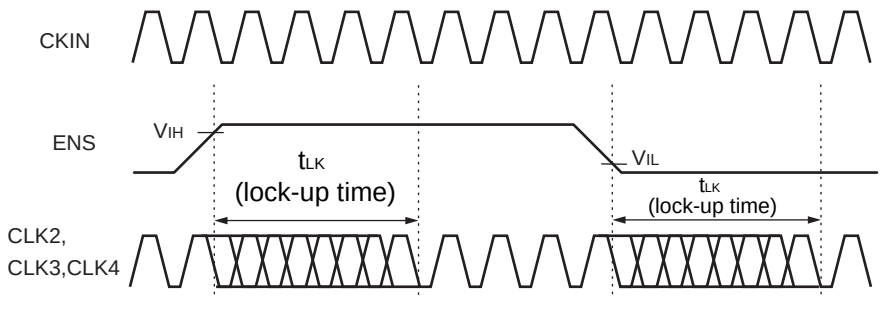
<Output timing with XPDREF control>



<Lock-up time>



If the power down control is performed on pins XPD1, XPD2, XPD3 and XPD4, the desired clock frequency will be obtained once the power down pin becomes at the “H” level and after the lock-up time t_{LK} has passed at maximum.



If the ENS pin setting changes during the normal operation, setting clocks CLK2, CLK3 and CLK4 will be output once the ENS pin level is decided and after lock-up time t_{LK} has passed at maximum.

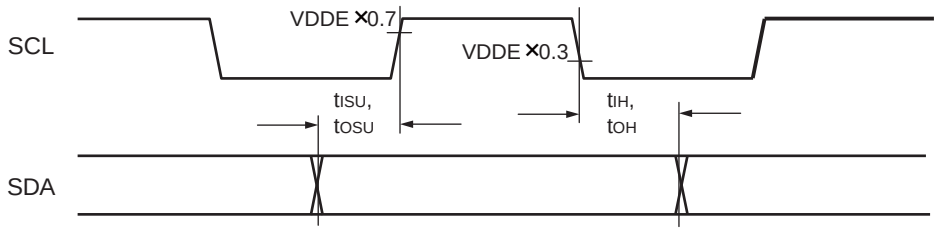
Note: When the ENS pin setting is changed, the stabilization wait time is needed for the output clock from CLK2, CLK3 and CLK4 pins. During the stabilization wait time, the output frequency, output clock duty cycle, modulation frequency, and cycle-cycle jitter cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.

• **AC characteristics 2 (Serial timing)**

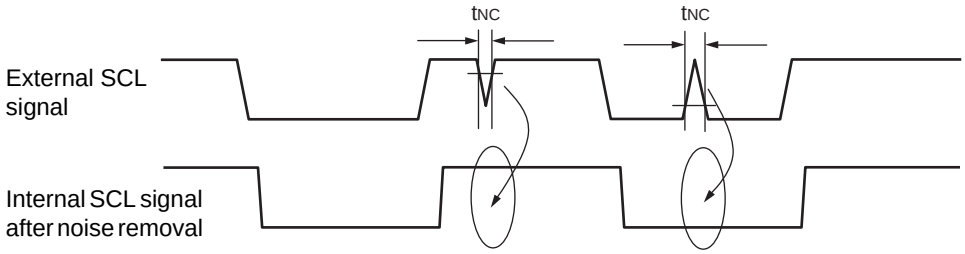
(Ta = − 40 °C to + 85 °C, VDD = 1.8 V ± 0.15 V, VDDE = 2.6 V ± 0.1 V)

Parameter	Symbol	Pin	Conditions	Value		Unit
				Min	Max	
SCL clock frequency	f_{SCL}	SCL	—	0	400	kHz
During data input set up time	t_{ISU}	SDA	—	100	—	ns
During data input hold time	t_{IH}	SDA	—	0	—	ns
Noise removal width	t_{NC}	SDA SCL	—	100	160	ns
Input hysteresis	V_{HYS}	SDA SCL	—	0.3	—	V
(Repeat) START condition hold time	t_{STAH}	SDA SCL	—	0.5	—	µs
Repeat START condition setup time	t_{STASU}	SDA SCL	—	0.5	—	µs
SCL clock “L” width	t_{CL}	SCL	—	1	—	µs
SCL clock “H” width	t_{CH}	SCL	—	0.5	—	µs
STOP condition setup time	t_{STOSU}	SDA SCL	—	0.5	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SDA SCL	—	1	—	µs
During bus drive set up time	t_{OSU}	SDA	Bus load: under 400 pF, Resistor value for bus pull-up: at least 750 Ω	1	—	µs
During bus drive hold time	t_{OH}	SDA		0	0.6	µs
During bus drive fall time	t_{OF}	SDA		—	300	ns

• During data input/bus drive

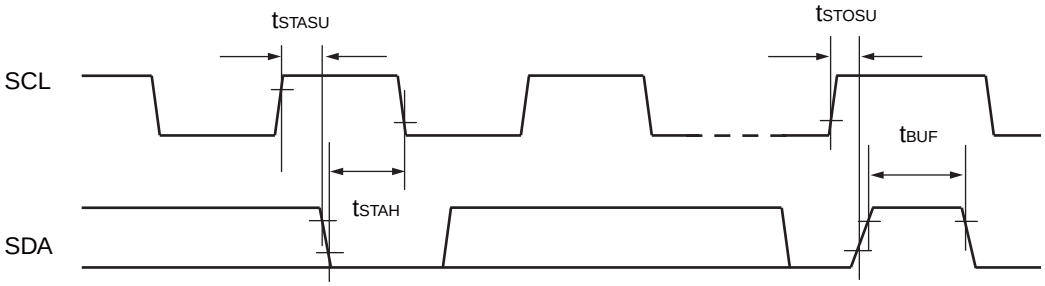


• Noise cancel operation

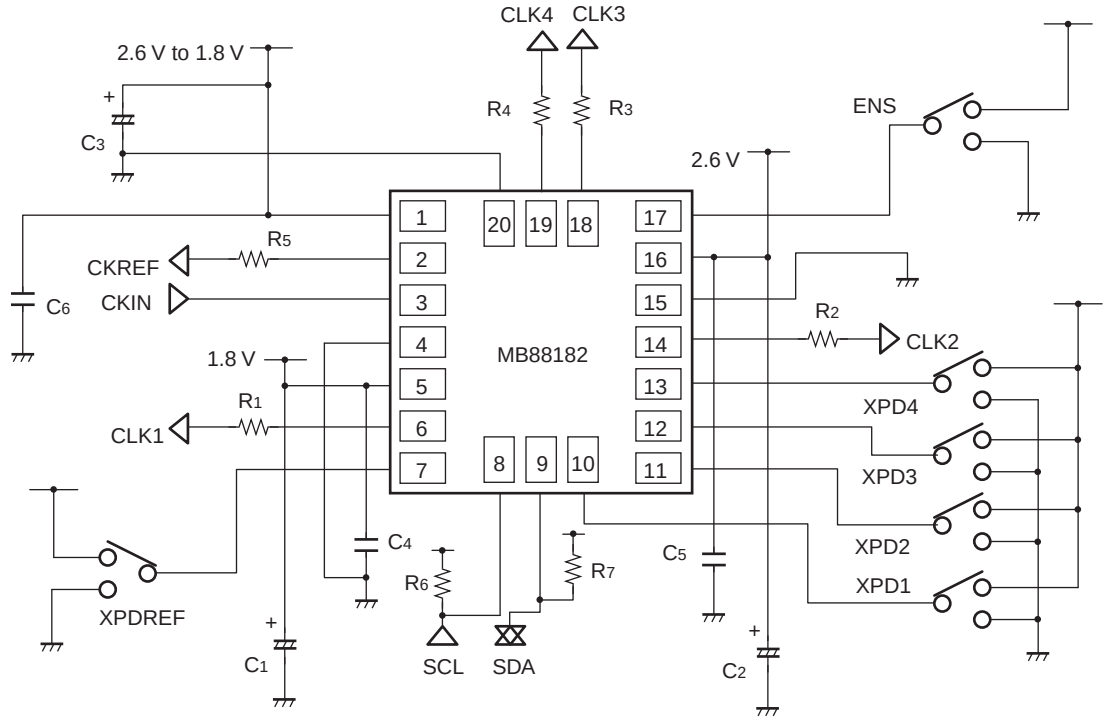


The pulse in the t_{NC} range is removed.

• (Repeat) Start operation, Stop operation



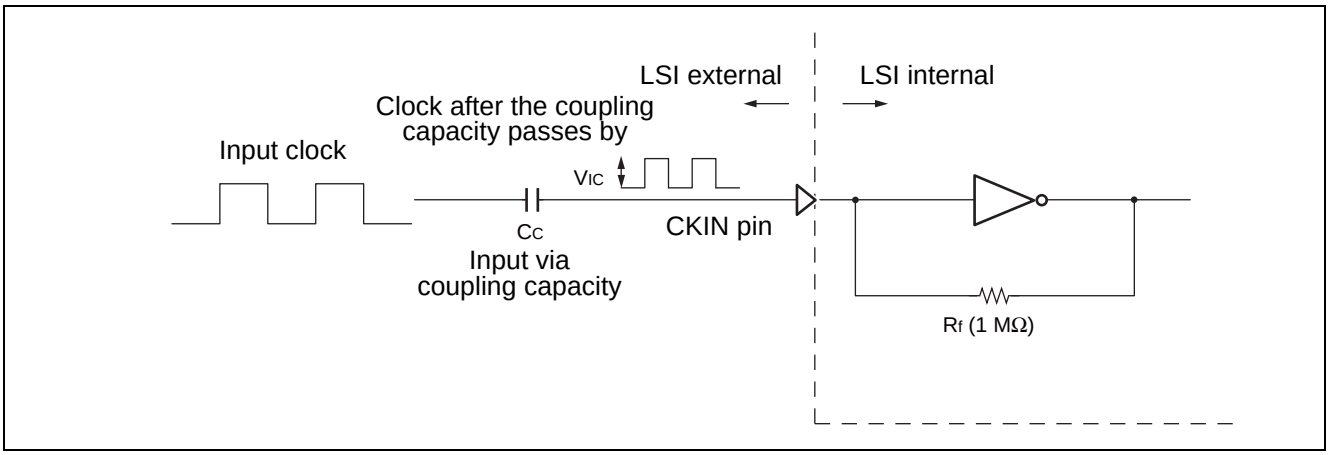
■ RECOMMENDED CIRCUIT



C_1, C_2, C_3	: Capacitor of 10 µF or higher
C_4, C_5, C_6	: Capacitor of about 0.01 µF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
R_1, R_2, R_3, R_4, R_5	: Impedance matching resistor for board pattern
R_6, R_7	: I^2C bus Pull-up resistor

■ CLOCK INPUT VIA COUPLING CAPACITY

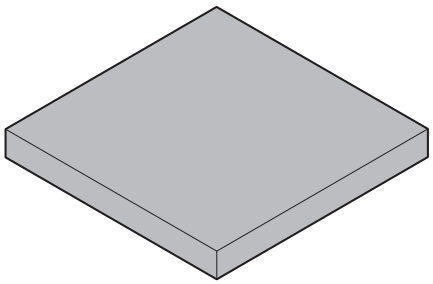
It is possible to input clocks to the CKIN pin via the coupling capacity as shown in the following figure. The device input part contains the CMOS inverter and the feedback resistor (1 MΩ). The clock input via the coupling capacity operates near the threshold level of the CMOS inverter, therefore the current for the capacity connection clock input increases compared to the normal input.

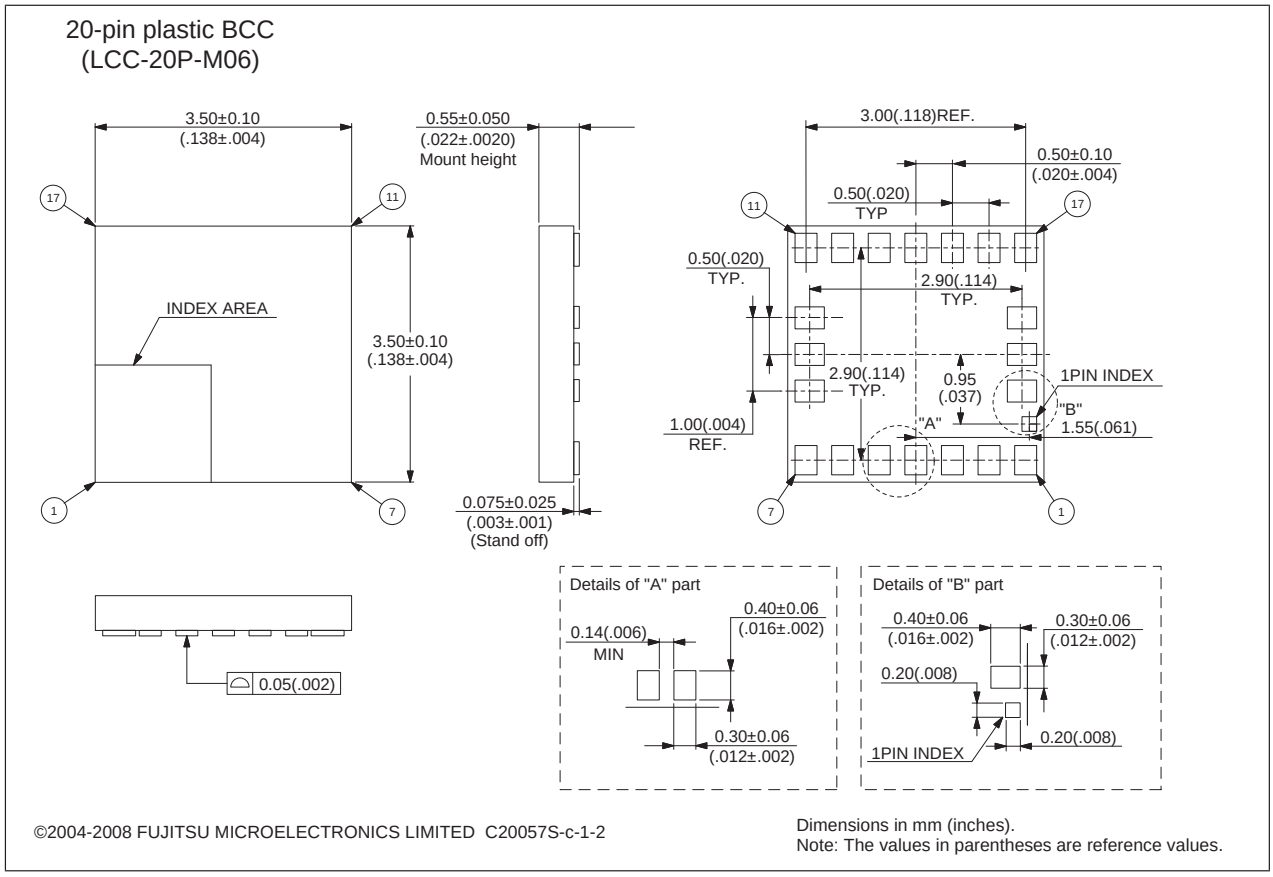


■ ORDERING INFORMATION

Part number	Package
MB881821APVA1-GE1 MB881821APVA1-G-ERE1 MB881821APVA1-G-EFE1 MB881821BPVA1-GE1 MB881821BPVA1-G-ERE1 MB881821BPVA1-G-EFE1 MB881822APVA1-GE1 MB881822APVA1-G-ERE1 MB881822APVA1-G-EFE1 MB881822BPVA1-GE1 MB881822BPVA1-G-ERE1 MB881822BPVA1-G-EFE1	20-pin plastic BCC (LCC-20P-M06)
MB881821AWQN-G-JNE1 MB881821AWQN-G-JN-ERE1 MB881821AWQN-G-JN-EFE1 MB881821BWQN-G-JNE1 MB881821BWQN-G-JN-ERE1 MB881821BWQN-G-JN-EFE1 MB881822AWQN-G-JNE1 MB881822AWQN-G-JN-ERE1 MB881822AWQN-G-JN-EFE1 MB881822BWQN-G-JNE1 MB881822BWQN-G-JN-ERE1 MB881822BWQN-G-JN-EFE1	24-pin plastic QFN (LCC-24P-M61)

■ PACKAGE DIMENSION

20-pin plastic BCC		
 (LCC-20P-M06)	Lead pitch	0.50 mm
	Package width × package length	3.50 mm × 3.50 mm
	Sealing method	Plastic mold
	Mounting height	0.60 mm MAX
	Weight	0.01 g



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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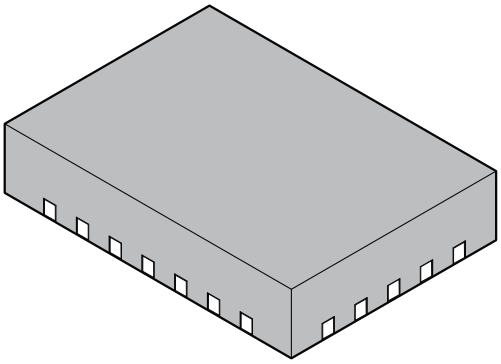
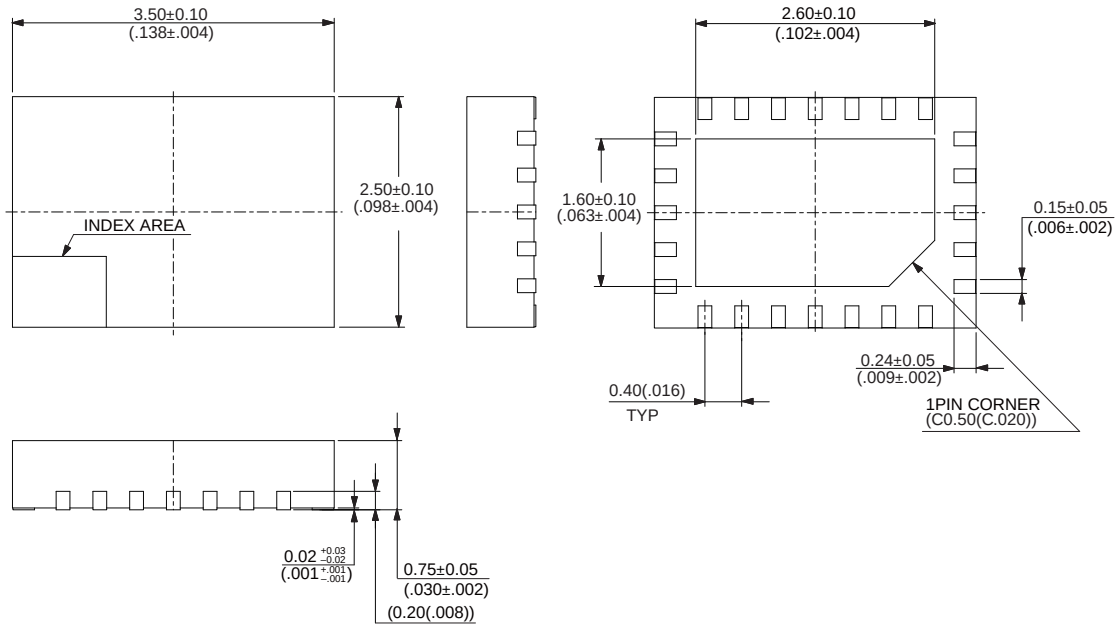
24-pin plastic QFN		
	Lead pitch	0.40 mm
	Package width × package length	2.50 mm × 3.50 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.02 g
(LCC-24P-M61)		

24-pin plastic QFN
(LCC-24P-M61)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

MEMO

FUJITSU MICROELECTRONICS LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-8508, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

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