IXF1110 10-Port Gigabit Ethernet Media Access Controller

Preliminary Datasheet

The IXF1110 is a 10-port 1000 Mbps Ethernet Media Access Controller (MAC) that supports IEEE 802.3 1000 Mbps applications. The device supports a System Packet Interface Level 4 Phase 2 (SPI4-2) system interface to the network processor or ASIC, and implements an internal Serializer/Deserializer (SerDes) to allow direct connection to optical modules. The integration of the SerDes functionality reduces PCB real-estate and system-cost requirements.

Applications

In general, the IXF1110 is appropriate for high-end switching applications where MAC and SerDes functions are not integrated into the system.

- High-End Optical Ethernet Switches
- Multi-Service Optical Ethernet Switches
- High-End Ethernet LAN/WAN Routers

Product Features

- Supports 10 independent 1000 Mbps full-duplex Ethernet MAC ports
- System Packet Interface Level 4 Phase 2 (SPI4-2)
  - —Capable of data transfers up to 12.8 Gbps
  - —Supports dynamic phase alignment
- SerDes interface with GBIC for Ethernet PHY connectivity
- 32-bit CPU interface
- RMON statistics
- JTAG and boundary scan capable
- Compliance with IEEE 802.3x Standard for flow control
- Jumbo frame support for 10 KB packets
- .18 µ CMOS process technology
- SFF-8053, Revision 5.5
- Internal 17.0 KB receive FIFO and 4.5 KB transmit FIFO per channel
- Independent enable/disable of any port
- Detection of short or overly large packets
- Error counters for dropped and errored packets
- CRC calculation and error detection
- Programmable option to:
  - —Filter packets with errors
  - —Filter, broadcast, multicast, and unicast address packets
  - —Automatically pad transmitted packets less than the minimum frame size
- 552-Ceramic Ball Grid Array (CBGA)
- 1.8 V and 2.5 V operation
- Power consumption: 490 mW per-port typical

Notice: This document contains preliminary information on new products. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

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Contents

Figures

Tables

1.0 General Description

The IXF1110 is a 10-port 1000 Mbps Ethernet Media Access Controller (MAC). The 10 Gigabit interface to the network processor is supported through a System Packet Interface Level 4 Phase 2 (SPI4-2), while the media interface is an integrated Serializer/Deserializer (SerDes). Figure 1 illustrates the IXF1110 block diagram and Figure 2 represents the IXF1110 system block diagram.

Figure 1. IXF1110 Block Diagram

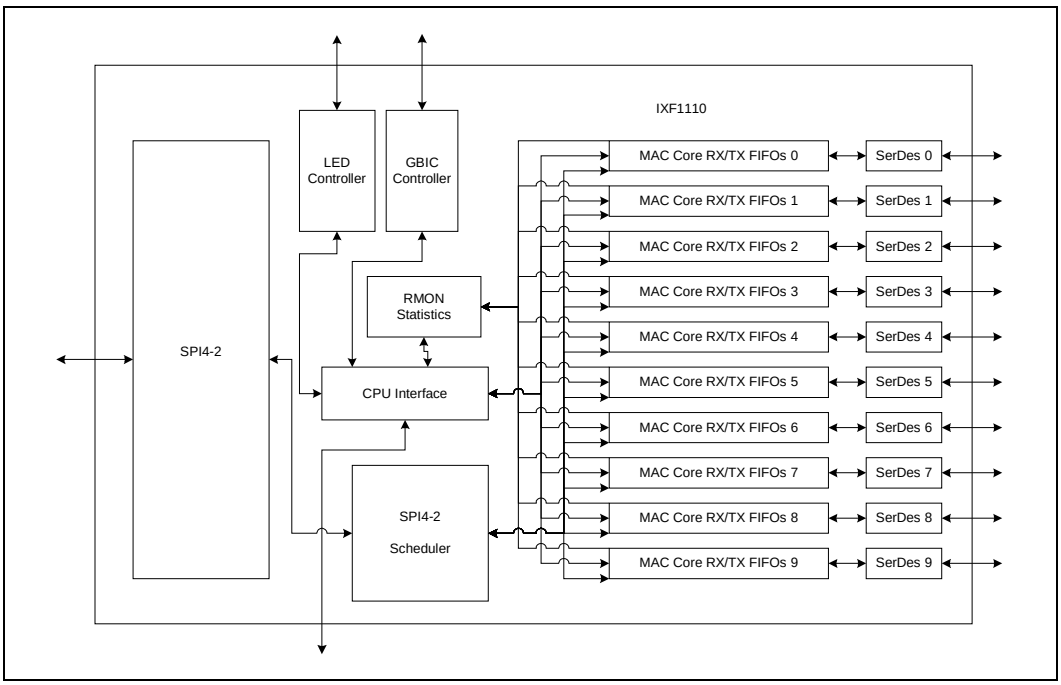


Figure 2. IXF1110 System Block Diagram

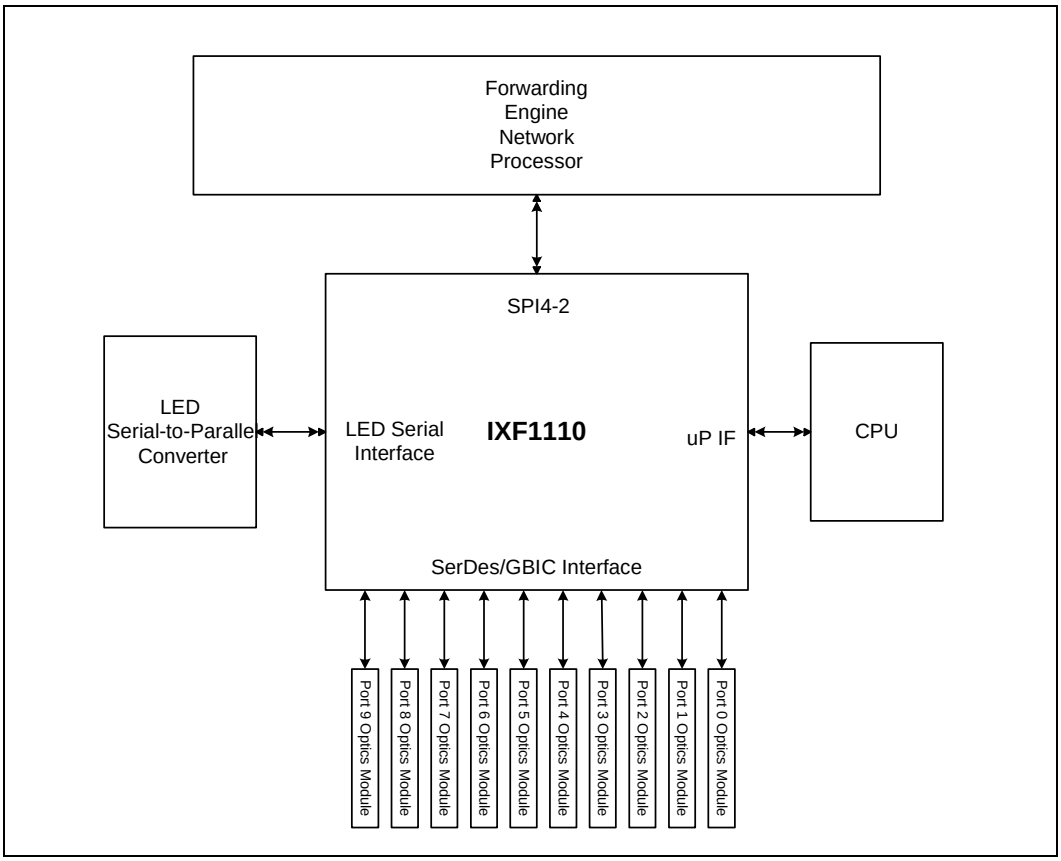
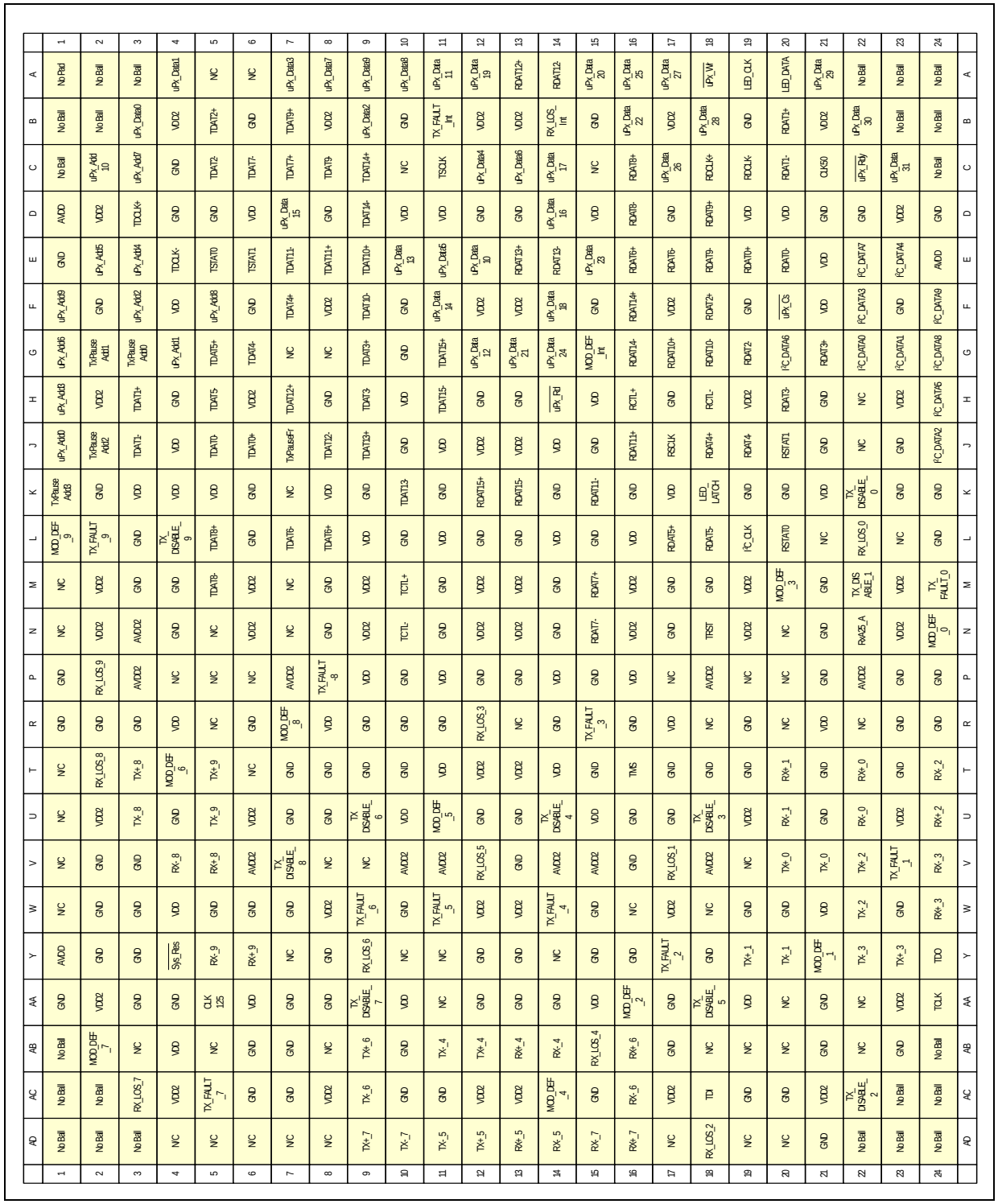


Figure 3 provides the physical layout of the balls, labeled with their ball number (matrix layout) and signal name.

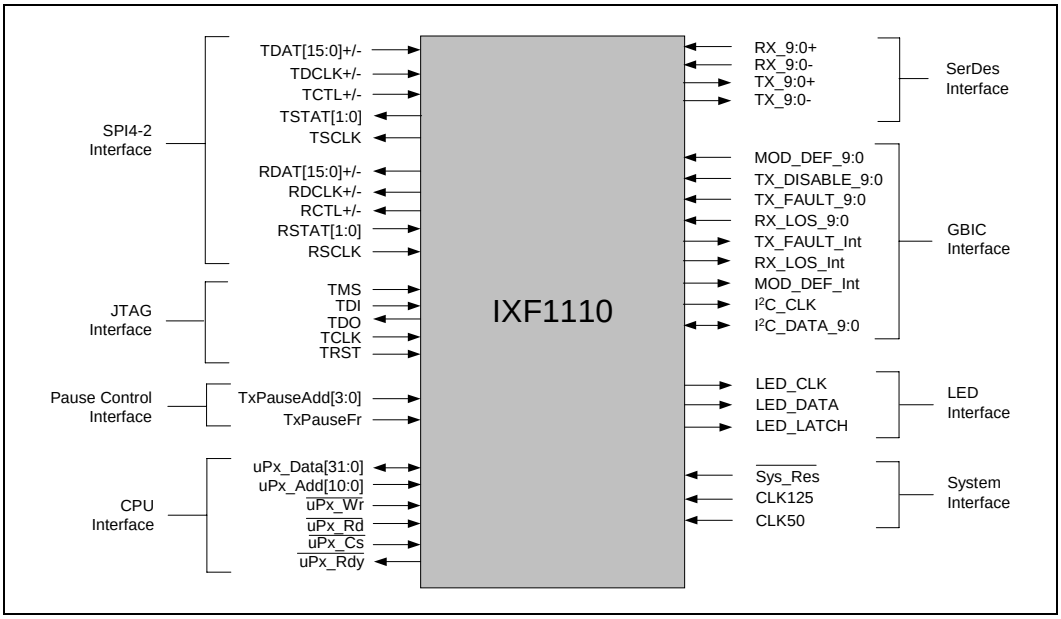
Figure 3. IXF1110 552-Ceramic Ball Grid Array (CBGA) Assignments (Top View)



2.0 Pin Assignments and Signal Descriptions

Figure 4 and Table 1 through Table 3 on page 19 provide the signal pins used by the IXF1110.

Figure 4. IXF1110 Pinout Diagram



2.1 Signal Name Conventions

Signal names may contain either a port designation (media interface) or a serial designation (System Interface). Signal naming conventions are as follows:

Port Designation. Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by an underscore and the Port Designation. For example, GBIC Serial Data signals would be identified as I^2C_DATA_0, I^2C_DATA_1, etc.

Serial Designation. A set of signals that are not tied to any specific port are designated by the Signal Mnemonic, followed by a bracketed serial designation. For example, SPI4-2 Transmit Data Bus signals would be identified as TDAT[15:0].

Table 1. IXF1110 Signal Pins

Ball Designator	Signal Name	Type	Standard	Signal Description
SPI4-2 Interface				
G11, C9, J9, H7, E8, E9, B7, L5, C7, L8, G5, F7, G9, B5, H3, J6	TDAT15+, TDAT14+, TDAT13+, TDAT12+, TDAT11+, TDAT10+, TDAT9+, TDAT8+, TDAT7+, TDAT6+, TDAT5+, TDAT4+, TDAT3+, TDAT2+, TDAT1+, TDAT0+,	Input	LVDS	**Transmit Data Bus:** Carries payload data and in-hand control words to the IXF1110 link-layer device.
H11, D9, K10, J8, E7, F9, C8, M5, C6, L7, H5, G6, H9, C5, J3, J5	TDAT15-, TDAT14-, TDAT13-, TDAT12-, TDAT11-, TDAT10-, TDAT9-, TDAT8-, TDAT7-, TDAT6-, TDAT5-, TDAT4-, TDAT3-, TDAT2-, TDAT1-, TDAT0-,	Input	LVDS	**Transmit Data Bus:** Carries payload data and in-hand control words to the IXF1110 link-layer device.
D3, E4	TDCLK+, TDCLK-	Input	LVDS	**Transmit Data Clock:** Clock associated with TDAT[15:0] and TCTL. Data and control lines are driven off the rising and falling edges of the clock.
M10, N10	TCTL+, TCTL-	Input	LVDS	**Transmit Control:** TCTL is High when a control word is present on TDAT[15:0]. Otherwise, TCTL is Low.
C11	TSCLK	Input	CMOS 2.5V	**Transmit Status Clock:** Clock associated with TSTAT [1:0].
E6, E5	TSTAT1, TSTAT0	Input	CMOS 2.5V	**Transmit FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.
K12, F16, E13, A13, J16, G17, D18, C16, M15, E16, L17, J18, G21, F18, B20, E19	RDAT15+, RDAT14+, RDAT13+, RDAT12+, RDAT11+, RDAT10+, RDAT9+, RDAT8+, RDAT7+, RDAT6+, RDAT5+, RDAT4+, RDAT3+, RDAT2+, RDAT1+, RDAT0+	Output	LVDS	**Receive Data:** Carries payload data and in-band control from the IXF1110 link-layer device.
K13, G16, E14, A14, K15, G18, E18, D16, N15, E17, L18, J19, H20, G19, C20, E20	RDAT15-, RDAT14-, RDAT13-, RDAT12-, RDAT11-, RDAT10-, RDAT9-, RDAT8-, RDAT7-, RDAT6-, RDAT5-, RDAT4-, RDAT3-, RDAT2-, RDAT1-, RDAT0-	Output	LVDS	**Receive Data:** Carries payload data and in-band control from the IXF1110 link-layer device.
C18, C19	RDCLK+, RDCLK-	Output	LVDS	**Receive Data Clock:** Clock associated with RDAT[15:0] and RCTL. Data and control lines are driven off the rising and falling edges of the clock.

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
H16, H18	RCTL+, RCTL-	Output	LVDS	**Receive Control:** RCTL is High when a control word is present on RDAT[15:0]. Otherwise, RCTL is Low.
J17	RSCLK	Input	CMOS 2.5V	**Receive Status Clock:** Clock associated with RSTAT[1:0].
J20, L20	RSTAT1, RSTAT0	Input	CMOS 2.5V	**Receive FIFO Status:** Carries round-robin FIFO status information, along with associated error detection and framing.
SerDes Interface				
T5, T3, AD9, AB9, AD12, AB12, Y23, V22, Y19, V20	TX_9+, TX_8+, TX_7+, TX_6+, TX_5+, TX_4+, TX_3+, TX_2+, TX_1+, TX_0+	Output	LV PECL	**Transmit Differential Output, Positive:** Carries the 1.25 GHz data to the optics module.
U5, U3, AD10, AC9, AD11, AB11, Y22, W22, Y20, V21	TX_9-, TX_8-, TX_7-, TX_6-, TX_5-, TX_4-, TX_3-, TX_2-, TX_1-, TX_0-	Output	LV PECL	**Transmit Differential Output, Negative:** Carries the 1.25 GHz data to the optics module.
Y6, V5, AD16, AB16, AD13, AB13, W24, U24, T20, T22	RX_9+, RX_8+ RX_7_, RX_6+ RX_5+, RX_4+ RX_3+, RX_2+ RX_1+, RX_0+	Input	LV PECL	**Receive Differential Input, Positive:** Carries the 1.25 GHz data from the optics module.
Y5, V4, AD15, AC16, AD14, AB14, V24, T24, U20, U22	RX_9-, RX_8- RX-7-, RX_6- RX_5-, RX_4- RX_3-, RX_2- RX_1-, RX_0-	Input	LV PECL	**Receive Differential Input, Negative:** Carries the 1.25 GHz data from the optics module.
CPU Interface				
C2 F1 F5 C3 G1 E2 E3 H1 F3 G4 J1	uPx_Add10 uPx_Add9 uPx_Add8 uPx_Add7 uPx_Add6 uPx_Add5 uPx_Add4 uPx_Add3 uPx_Add2 uPx_Add1 uPx_Add0	Input	CMOS 2.5V	**Address bus**
F20	$\overline{\text{uPx\_Cs}}$	Input	CMOS 2.5V	**Chip Select Signal**

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
C23 B22 A21 B18 A17 C17 A16 G14 E15 B16 G13 A15 A12 F14 C14 D14 D7 F11 E10 G12 A11 E12 A9 A10 A8 C13 E11 C12 A7 B9 A4 B3	uPx_Data31 uPx_Data30 uPx_Data29 uPx_Data28 uPx_Data27 uPx_Data26 uPx_Data25 uPx_Data24 uPx_Data23 uPx_Data22 uPx_Data21 uPx_Data20 uPx_Data19 uPx_Data18 uPx_Data17 uPx_Data16 uPx_Data15 uPx_Data14 uPx_Data13 uPx_Data12 uPx_Data11 uPx_Data10 uPx_Data9 uPx_Data8 uPx_Data7 uPx_Data6 uPx_Data5 uPx_Data4 uPx_Data3 uPx_Data2 uPx_Data1 uPx_Data0	Input/ Output	CMOS 2.5V	**Bi-directional data bus**
A18	$\overline{\text{uPx\_Wr}}$	Input	CMOS 2.5V	**Write Strobe**
H14	$\overline{\text{uPx\_Rd}}$	Input	CMOS 2.5V	**Read Strobe**
C22	$\overline{\text{uPx\_Rdy}}$	Output	CMOS 2.5V	**Cycle complete indicator**
Pause Control Interface				
J7	TxPauseFr	Input	CMOS 2.5V	Insert PAUSE frame control signal.
K1 J2 G2 G3	TxPauseAdd3 TxPauseAdd2 TxPauseAdd1 TxPauseAdd0	Input	CMOS 2.5V	Port Selection for PAUSE frames.
GBIC Interface				
L2 P8 AC5 W9 W11 W14 R15 Y17 V23 M24	TX_FAULT_9 TX_FAULT_8 TX_FAULT_7 TX_FAULT_6 TX_FAULT_5 TX_FAULT_4 TX_FAULT_3 TX_FAULT_2 TX_FAULT_1 TX_FAULT_0	Input	CMOS 2.5V	Input used to determine when there is a GBIC transmitter fault.

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
P2 T2 AC3 Y9 V12 AB15 R12 AD18 V17 L22	RX_LOS_9 RX_LOS_8 RX_LOS_7 RX_LOS_6 RX_LOS_5 RX_LOS_4 RX_LOS_3 RX_LOS_2 RX_LOS_1 RX_LOS_0	Input	CMOS 2.5V	Input used to determine when the GBIC receiver loses synchronization.
L1 R7 AB2 T4 U11 AC14 M20 AA16 Y21 N24	MOD_DEF_9 MOD_DEF_8 MOD_DEF_7 MOD_DEF_6 MOD_DEF_5 MOD_DEF_4 MOD_DEF_3 MOD_DEF_2 MOD_DEF_1 MOD_DEF_0	Input	CMOS 2.5V	Input used to determine when a GBIC module is present.
L4 V7 AA9 U9 AA18 U14 U18 AC22 M22 K22	TX_DISABLE_9 TX_DISABLE_8 TX_DISABLE_7 TX_DISABLE_6 TX_DISABLE_5 TX_DISABLE_4 TX_DISABLE_3 TX_DISABLE_2 TX_DISABLE_1 TX_DISABLE_0	Output	CMOS 2.5V	Output used to disable a GBIC module transmitter.
B11	TX_FAULT_Int	Output	CMOS 2.5V	Open drain interrupt output to signal a TX_FAULT condition.
B14	RX_LOS_Int	Output	CMOS 2.5V	Open drain interrupt output to signal a RX_LOS condition.
G15	MOD_DEF_Int	Output	CMOS 2.5V	Open drain interrupt output to signal a MOD_DEF condition.
L19	I^2C_CLK	Output	CMOS 2.5V	Clock used for the I^2C bus interface.
F24 G24 E22 G20 H24 E23 F22 J24 G23 G22	I^2C_DATA_9 I^2C_DATA_8 I^2C_DATA_7 I^2C_DATA_6 I^2C_DATA_5 I^2C_DATA_4 I^2C_DATA_3 I^2C_DATA_2 I^2C_DATA_1 I^2C_DATA_0	Input/ Output	CMOS 2.5V	Data I/O for the I^2C bus interface.
LED Interface				
A19	LED_CLK	Output	CMOS 2.5V	Clock output for the LED block.
A20	LED_DATA	Output	CMOS 2.5V	Data output for the LED block.
K18	LED_LATCH	Output	CMOS 2.5V	Latch enable for the LED block.

Table 1. IXF1110 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
JTAG Interface				
AA24	TCLK	Input	CMOS 2.5V	JTAG Test Clock
T16	TMS	Input	CMOS 2.5V	JTAG Test Mode Select
AC18	TDI	Input	CMOS 2.5V	JTAG Test Data Input
N18	TRST	Input	CMOS 2.5V	JTAG Test Reset
Y24	TDO	Output	CMOS 2.5V	JTAG Test Data Output
System Interface				
AA5	CLK125	Input	CMOS 2.5V	Input clock to PLL.
C21	CLK50	Input	CMOS 2.5V	Input clock to SPI4-2 RX PLL.
Y4	$\overline{\text{Sys\_Res}}$	Input	CMOS 2.5V	System hard reset (active Low).

Table 2. IXF1110 Power Supply Signal Descriptions

Ball #	Signal Name	Type	Standard	Signal Description
D1, E24, Y1	AVDD	–	–	1.8 V supply for analog circuits.
N3, N22, P3, P7, P18, P22, V6, V10, V11, V14, V15, V18	AVDD2		–	2.5 V supply for analog circuits.
D6, D10, D11, D15, D19, D20, E21, F4, F21, H10, H15, J4, J11, J14, K3, K4, K5, K8, K17, K21, L9, L11, L14, L16, P9, P11, P14, P16, R4, R8, R17, R21, T11, T14, U10, U15, W4, W21, AA6, AA10, AA15, AA19, AB4	VDD	–	–	1.8 V core supply.
B4, B8, B12, B13, B17, B21, D2, D23, F8, F12, F13, F17, H2, H6, H19, H23, J12, J13, M2, M6, M9, M12, M13, M16, M19, M23, N2, N6, N9, N12, N13, N16, N19, N23, T12, T13, U2, U6, U19, U23, W8, W12, W13, W17, AA2, AA23, AC4, AC8, AC12, AC13, AC17, AC21	VDD2	–	–	2.5 V I/O supply.
B6, B10, B15, B19, C4, D4, D5, D8, D12, D13, D17, D21, D22, D24, E1, F2, F6, F10, F15, F19, F23, G10, H4, H8, H12, H13, H17, H21, J10, J15, J21, J23, K2, K6, K9, K11, K14, K16, K19, K20, K23, K24, L3, L6, L10, L12, L13, L15, L24, M3, M4, M8, M11, M14, M17, M18, M21, N4, N8, N11, N14, N17, N21, P1, P10, P12, P13, P15, P21, P23, P24, R1, R2, R3, R6, R9, R10, R11, R14, R16, R19, R23, R24, T7, T8, T9, T10, T15, T17, T18, T19, T21, T23, U4, U7, U8, U12, U13, U16, U17, U21, V2, V3, V13, V16, W2, W3, W5, W6, W7, W10, W15, W19, W20, W23, Y2, Y3, Y8, Y12, Y13, Y15, Y16, Y18, AA1, AA3, AA4, AA7, AA8, AA12, AA13, AA14, AA17, AA21, AB6, AB7, AB10, AB17, AB21, AB23, AC6, AC7, AC10, AC11, AC15, AC19, AC20, AD21	GND	–	–	Ground return for all signals.

Table 3. IXF1110 Unused Balls/Reserved

Ball #	Signal Name	Type	Standard	Signal Description
A5, A6, C10, C15, G7, G8, H22, J22, K7, L21, L23, M1, M7, N1, N5, N7, N20, P4, P5, P6, P17, P19, P20, R5, R13, R18, R20, R22, T1, T6, U1, V1, V8, V9, V19, W1, W16, W18, Y7, Y10, Y11, Y14, AA11, AA20, AA22, AB3, AB5, AB8, AB18, AB19, AB20, AB22, AD4, AD5, AD6, AD7, AD8, AD17, AD19, AD20	N/C	–	–	No connection.
A2, A3, A22, A23, A24, B1, B2, B23, B24, C1, C24, AB1, AB24, AC1, AC2, AC23, AC24, AD1, AD2, AD3, AD22, AD23, AD24	No Ball	–	–	Balls removed from substrate.
A1	No Pad	–	–	Pad removed from substrate.

3.0 Functional Descriptions

3.1 Media Access Controller

3.1.1 General Description

The IXF1110 main functional block consists of a 1000 Mbps Ethernet Media Access Controller (MAC), supporting the following features:

- 1000 Mbps full-duplex operation
- Independent enable/disable of any port
- Detection of length error, runt, or overly large packets
- RMON statistics and error counters
- Cyclic Redundancy Check (CRC) calculation and error detection
- Programmable option to:
  - — Filter packets with errors
  - — Filter, broadcast, multicast, and unicast address packets
  - — Automatically pad transmitted packets less than the minimum frame size
- Compliance with IEEE 802.3x Standard for Flow Control (symmetric pause capability)

The MAC is fully integrated, designed for use with Ethernet 802.3 Frame types, and is compliant with all of the required IEEE 802.3 MAC requirements.

The MAC adds preamble and Start-of-Frame Delimiter (SFD) to all frames sent to it (transmit path) and removes preamble and SFD on all frames received by it (receive path). A CRC check is also applied to all transmit and receive packets. Packets with a bad CRC are marked, counted in the statistics block, and may be optionally dropped.

Note: The MAC operates in full-duplex mode only.

3.1.2 Features

Section 3.1.2.1, “Padding of Undersized Frames on Transmit” on page 21 through Section 3.1.2.4, “PAUSE Command Frames” on page 23 cover the MAC functions.

3.1.2.1 Padding of Undersized Frames on Transmit

The padding feature allows Ethernet frames smaller than 64 bytes to be transferred across the SPI4-2 interface and automatically padded up to 64 bytes by the MAC. This feature is enabled by setting bit 7 of the DiverseConfig Register = 1 (Address Port_Index + 0x18h). See Table 55, “Diverse Config Register (Addr: Port_Index + 0x18)” on page 87.

3.1.2.2 Automatic CRC Generation

The Automatic CRC Generation is used in conjunction with the padding feature to generate and append a correct CRC to any incoming frame from the SPI4-2 interface. This feature is enabled by setting bit 6 of the DiverseConfig Register = 1 (Address Port_Index + 0x18h) (see Table 55, "Diverse Config Register (Addr: Port_Index + 0x18)" on page 87).

Note: When padding of undersized frames on transmit is enabled, the automatic CRC generation must be enabled for proper operation of the IXF1110.

3.1.2.3 Filtering of Receive Packets

This feature allows the MAC to filter receive packets under various conditions and drop the packets via an interaction with the Receive FIFO control.

3.1.2.3.1 Filter on Unicast Packet Match

This feature is enabled when bit 0 of the PacketFilterControl Register = 1. Any frame received in this mode that does not match the StationAddress is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all unicast frames are sent to the SPI4-2 interface.

3.1.2.3.2 Filter on Multicast Packet Match

This feature is enabled when bit 1 of the PacketFilterControl Register = 1. Any frame received in this mode that does not match the PortMulticastAddress is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable register = 1. Otherwise, all multicast frames are sent to the SPI4-2 interface.

3.1.2.3.3 Filter Broadcast Packets

This feature is enabled when bit 2 of the PacketFilterControl Register = 1. Any broadcast frame received in this mode is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all broadcast frames are sent to the SPI4-2 interface.

3.1.2.3.4 Filter VLAN Packets

This feature is enabled when bit 3 of the PacketFilterControl Register = 1. VLAN frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all VLAN frames are sent to the SPI4-2 interface.

3.1.2.3.5 Filter PAUSE Packets

This feature is enabled when bit 4 of the PacketFilterControl Register = 0. PAUSE frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all PAUSE frames are sent to the SPI4-2 interface.

Table 4. Pause Packets Drop Enable Behavior

PauseFramePass	FrameDropEn	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and sent to the switch or Network Processor, regardless of the FrameDropEn setting.
0	1	PAUSE Packets are marked as bad, are dropped in the RX FIFO, and never appear at the SPI4-2 interface.

3.1.2.3.6 Filter CRC Errored Packets

Frames received with an errored CRC are marked as bad frames and may optionally be dropped in the RX FIFO. Otherwise, the frames are sent to the SPI4-2 interface and may be dropped by the switch or system controller (see Table 5).

Table 5. CRC Errored Packets Drop Enable Behavior

CRCErroredPASS	FrameDropEn	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and are sent to the switch or Network Processor regardless of the FrameDropEn setting.
0	1	CRC errored packets are marked as bad, dropped in the RX FIFO, and never appear at the SPI4-2 interface.

3.1.2.4 PAUSE Command Frames

The MAC acts on any PAUSE command frames received from the link partner by checking the entire frame and verifying that it is a valid PAUSE control frame addressed to either the Multicast Address (01-80-c2-00-00-01 as specified in IEEE 802.3, Annex 31B) or the Station Address. If the PAUSE frame is valid, the Transmit side of the MAC pauses for the required number of Pause Quanta, as specified in IEEE 802.3u, Clause 31 (see Table 4).

Note: PAUSE does not begin until completion of the frame currently being transmitted.

3.1.3 Auto-Negotiation

In the IXF1110, auto-negotiation is carried out by an internal state machine within the MAC. The IXF1110 is fully IEEE 802.3z standard compliant.

There are three registers involved in this auto-negotiation process: RxConfigWord, TxConfigWord, and DiverseConfig:

- RxConfigWord performs the operation of the Auto-Negotiation Link Partner Ability Register (see Table 53, “RX Config Word Register (Addr: Port_Index + 0x16)” on page 86)
- TxConfigWord performs the operation of the Auto-Negotiation Advertisement Register (see Table 54, “TX Config Word Register (Addr: Port_Index + 0x17)” on page 87
- DiverseConfig sets the auto-negotiation enable bit (see Table 55, “Diverse Config Register (Addr: Port_Index + 0x18)” on page 87)

The TX Config Word Register must be written to program the modes advertised. The next step is to enable auto-negotiation with the Diverse Config Register. The RX Config Word Register must be polled to determine when auto-negotiation is complete and to determine the link mode. Upon completion, program the following MAC registers to match the results:

- Link: Table 62, “Link LED Enable Register (Addr: 0x502)” on page 98 (Addr 502)
- Flow Control: If the link partner does not support flow control, the FC Enable Register (Addr Port Index + 0x12) must be updated to reflect this change (see Table 50, “FC Enable Register (Addr: Port_Index + 0x12)” on page 85

3.1.4 RMON Statistics Support

3.1.4.1 RMON Statistics

The IXF1110 supplies RMON statistics via the CPU interface. These statistics are available in the form of counter values that can be accessed at specific addresses in the IXF1110 memory map. Once read, these counters automatically reset and begin counting from zero. A separate set of RMON statistics is available for each MAC device in the IXF1110.

Implementation of the RMON Statistics block is similar to the functionality provided by existing Intel switch and router products. This allows the IXF1110 to provide all of the RMON Statistics group as defined by RFC2819.

The following statistics are supported on a per-port basis:

etherStatsDropEvents (RX)	
etherStatsOctets [31:0] (RX)	etherStatsOctets [31:0] (TX)
etherStatsPkts (RX)	etherStatsPkts (TX)
etherStatsBroadcastPkts (RX)	etherStatsBroadcastPkts (TX)
etherStatsMulticastPkts (RX)	etherStatsMulticastPkts (TX)
etherStatsCRCAlignErrors (RX)	etherStatsCRCAlignErrors (TX)
etherStatsUndersizePkts (RX)	etherStatsUndersizePkts (TX
etherStatsOversizePkts (RX)	etherStatsOversizePkts (TX)
etherStatsFragments (RX)	etherStatsFragments (TX)
etherStatsJabber (RX)	etherStatsJabber (TX)
etherStatsPkts64Octets (RX)	etherStatsPkts64Octets (TX)
etherStatsPkts65to127Octets (RX)	etherStatsPkts65to127Octets (TX)
etherStatsPkts128to255Octets (RX)	etherStatsPkts128to255Octets (TX)

etherStatsPkts256to511Octets (RX)	etherStatsPkts256to511Octets (TX)
etherStatsPkts512to1023Octets (RX)	etherStatsPkts512to1023Octets (TX)
etherStatsPkts1024to1518Octets (RX)	etherStatsPkts1024to1518Octets (TX)

Note: A packet transfer with an invalid 10-bit symbol will not always update the statistics registers correctly.

- **Behavior:** The IXF1110 8B10B decoder substitutes a valid code word octet in its place. The packet transfer is aborted and marked as bad. The new internal length of the packet is equal to the byte position where the invalid symbol was. No packet fragments are seen at the next packet transfer.
- **Issue:** If the invalid 10-bit code is inserted in a byte position of 64 or greater, expected RX statistics are reported. However, if the invalid code is inserted in a byte position of less than 64, expected RX statistics are not stored.

3.1.5 Transmit Pause Control Interface

The Transmit Pause Control interface is completely asynchronous. It consists of four address signals (TxPauseAdd[3:0]) and a strobe signal (TxPauseFr). The required address for this interface operation is placed on the TxPauseAdd[3:0] pins and the TxPauseFr is pulsed High and then returned Low. The timing for the interface is shown in Table 7. The valid decodes for the TxPauseAdd[3:0] signals are shown in Table 6. Figure 5 on page 26 displays the Transmit Pause Control interface.

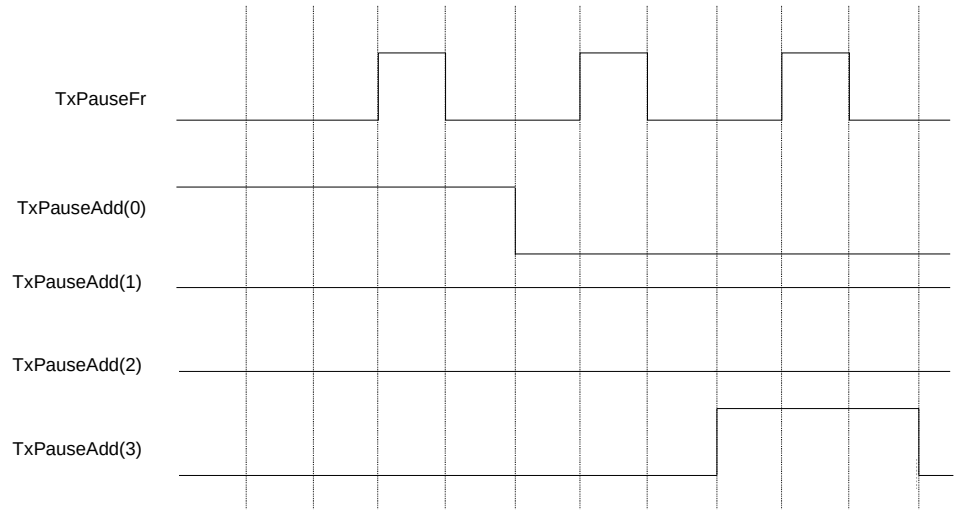
Table 6. Valid Decodes for TxPauseAdd[3:0]

TxPauseAdd[3:0]	Operation of Tx Pause Interface
00h	Sends out a PAUSE frame on every port with a pause_time = ZERO (for example, cancels all previous pause commands).
01h to 0Ah	Sends a PAUSE frame out on the selected port with pause_time = to the value programmed into that port's register set
0Bh to 0Eh	Reserved. These are invalid decodes and should not be used. The Tx Pause Interface will not operate under these conditions.
0Fh	Sends a PAUSE frame out on every port with pause_time = to the value programmed into that ports register set.

Table 7. Interface Timing

Timing Parameter	Min	Max
TxPauseFr pulse width	16 ns	–
TxPauseAdd[3:0] setup time before TxPauseFr rising edge	16 ns	–
TxPauseAdd[3:0] hold time after TxPauseFr rising edge	32 ns	–
Time between TxPauseFr pulses	48 ns	–

Figure 5. Transmit Pause Control Interface



This example shows the following conditions:

Strobe 1:
- Port 0 : Transmit Pause Packet

Strobe 2:
- All Ports : Transmit Pause Packet with pause_time = 0

Strobe 3:
- Port 7 : Transmit Pause Packet

3.2 System Packet Interface Level 4 Phase 2

The System Packet Interface Level 4 Phase 2 (SPI4-2) provides a high-speed connection to a network processor or an ASIC. The interface implemented on the IXF1110 operates at data rates up to 12.8 Gbps and supports up to ten 1 Gbps MAC channels in the IXF1110. The data path is 16 lanes wide in each direction, with each lane operating at up to 800 Mbps. Port addressing, start/end packet control, and error control codes are all transferred “in-band” on the data bus. In-band addressing supports up to 10 ports. Separate transmit and receive FIFO status lines are used for flow control. By keeping the FIFO status information out-of-band, the transmit and receive interfaces may be decoupled to operate independently.

3.2.1 Data Path

Transfer of complete packets or shorter bursts is controlled by the programmed MaxBurst1 or MaxBurst2 in conjunction with the FIFO status bus. The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted between burst transfers only. Once a transfer begins, data words are sent uninterrupted until end-of-packet, or until a multiple of 16 bytes is reached as programmed in MaxBurst1 and MaxBurst2. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words and/or training patterns.

Note: The system designer should be aware that the MAC Transfer Threshold Register must be set to a value which exceeds MaxBurst1 number of bytes. Otherwise, a TX FIFO underrun may result.

The minimum and maximum supported packet lengths are determined by the application. Because the IXF1110 is targeted at the Ethernet environment, the minimum frame size is 64 bytes and the maximum frame size is 1522 bytes for VLAN packets (1518 bytes for non-VLAN packets). For larger frames, adjust the Max Frame Size Register value, seen in Table 49 on page 85. However, for ease of implementation, successive start-of-packets must occur not less than eight cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

Note: Data Packets with frame lengths less than 64 bytes cannot be transferred to the IXF1110 unless packet padding is enabled. If this rule is disregarded, unwanted fragments may be generated on the network at the SerDes interface.

Figure 6 on page 28 shows cycle-by-cycle behavior of the data path for valid state transitions. The states correspond to the type of words transferred on the data path. Transitions from the “Data Burst” state (to “Payload Control” or “Idle Control”) are possible only on the integer multiples of eight cycles (corresponding to multiples of 16-byte segmentations) or upon end-of-packet. A data burst must immediately follow a payload control word on the next cycle. Arcs not annotated correspond to single cycles.

In the IXF1110, the RX FIFO Status channel operates in a “pessimistic mode.” It is termed as pessimistic because it has the longest latency and largest impact on usable bandwidth. However, as a DIP-2 check error is a rare event, there will be no ‘real world’ effect on bandwidth utilization and no possibility of data loss. For example, if there is a DIP-2 check error found, all previously granted credits are cancelled and the internal status for each channel is set to SATISFIED. Any current data burst in transmission is completed. No new credits are granted until a complete FIFO status cycle has been received and validated by a correct DIP-2 check. This is the only method of operation that can eliminate the possibility of an overrun in the link partner device.

Figure 6. Data Path State Diagram

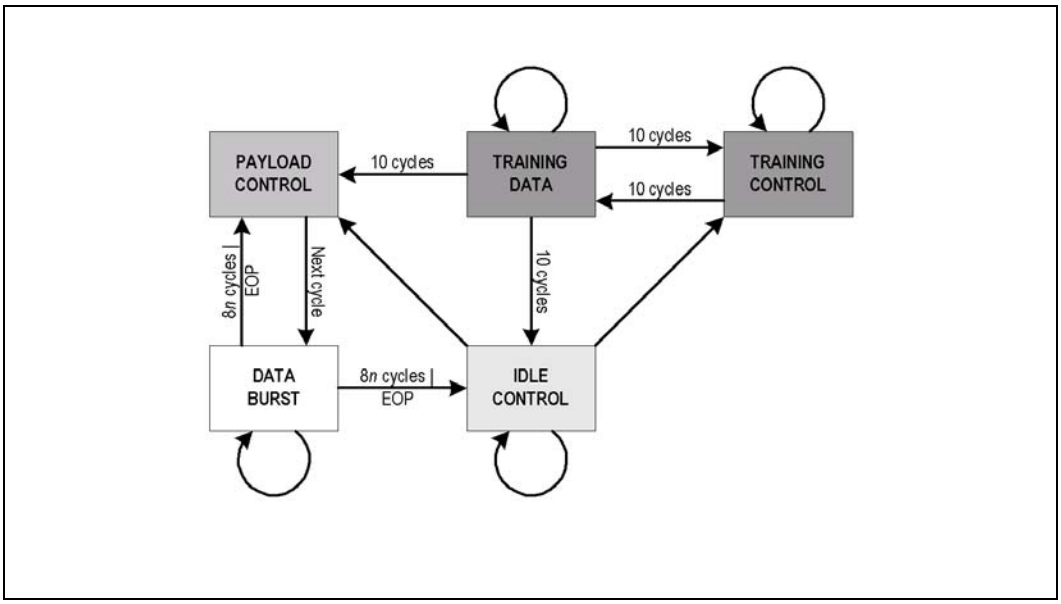
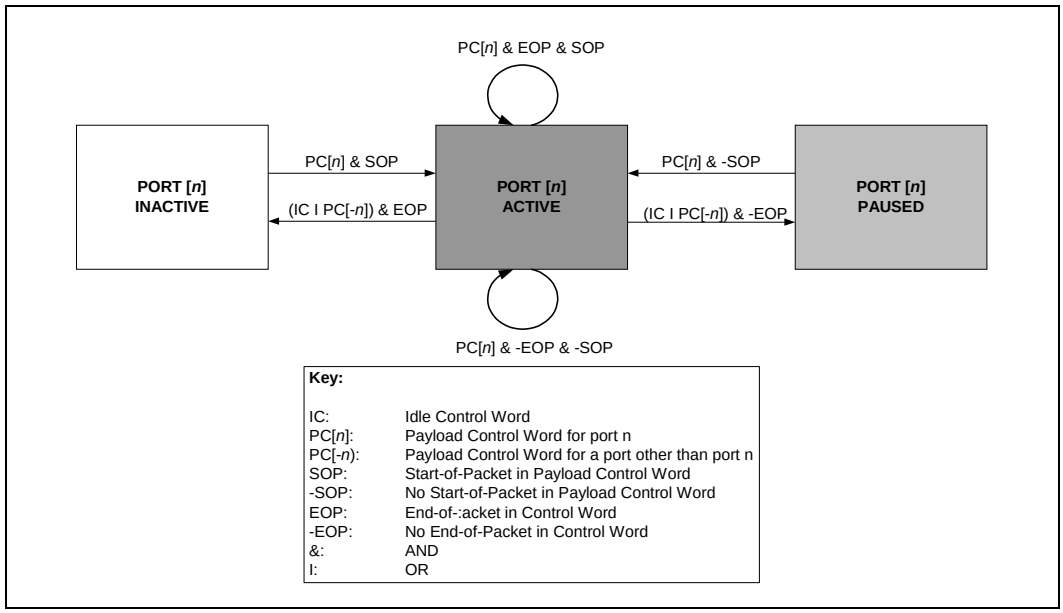


Figure 7 on page 29 shows per-port state transitions at control-word boundaries. At any given time, a port may be active (sending data), paused (not sending data but pending the completion of an outstanding packet), or inactive (not sending data, no outstanding packet).

The SPI4-2 Specification details all available Payload Control Words and should be used to reference the specific meaning of each. The IXF1110 supports all required functions per this specification. However, there are various specifics in the way certain Control Words affect the balance of the IXF1110 operation, such as how the device deals with EOP Aborts.

The SPI4-2 Specification allows the EOP Abort Payload Control word, which signals that the data associated with a particular frame is errored and should be dropped, or errored and dropped by the far-end link partner. In the IXF1110, all TX SPI4-2 transfers that end with an EOP Abort code have the TX SerDes CRC corrupted. This is true regardless of the MAC configuration.

Figure 7. Per-Port State Diagram with Transitions at Control Words



3.2.2 Start-Up Parameters

3.2.2.1 CALENDAR_LEN

CALENDAR_LEN specifies the length of each calendar sequence. As the IXF1110 is a 10-port device, CALENDAR_LEN is fixed at 10 for both TX and RX data paths.

3.2.2.2 CALENDAR_M

CALENDAR_M specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence.

In the IXF1110, the TX path CALENDAR_M is fixed at 1; thus, the port status for ports 0 - 9 will be transmitted only once between the framing and DIP2 cycle of the calendar sequence.

In the IXF1110, the RX path CALENDAR_M is configurable. The default value of expected RX CALENDAR_M is 1 as per the TX path. In Table 81, “SPI4-2 RX Calendar Register (Addr: 0x702)” on page 118, bits 3 to 0 specify CAL_M, which is the number of times the calendar sequence will be repeated over the default value of 1.

The default value for CAL_M is 0, thus the default value of both Tx and RX CALENDAR_M parameters is 1.

3.2.2.3 DIP2_Thr

DIP2_Thr is a parameter specifying the number of consecutive correct DIP2s required by the RX SPI4-2 to validate a calendar sequence and therefore terminate sending training sequences. In Table 81, “SPI4-2 RX Calendar Register (Addr: 0x702)” on page 118, bits 19 to 16 specify this parameter. The default value for DIP2_Thr is 1.

3.2.2.4 Loss_Of_Sync

Loss_Of_Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and therefore restart training sequences. Table 81, “SPI4-2 RX Calendar Register (Addr: 0x702)” on page 118, bits 11 to 8 specify this parameter. The default value for Loss_Of_Sync is 3.

3.2.2.5 DATA_MAX_T

DATA_MAX_T is an RX SPI4-2 parameter specifying the interval between transmission of periodic training sequences. In Table 80, “SPI4-2 RX Training Register (Addr: 0x701)” on page 117, bits 15 to 0 specify this parameter. The default value for DATA_MAX_T is 0x0000, which disables periodic training sequence transmission.

3.2.2.6 REP_T

REP_T is an RX SPI4-2 parameter specifying the number of repetitions of the training sequence to be scheduled every DATA_MAX_T interval. In Table 80, “SPI4-2 RX Training Register (Addr: 0x701)” on page 117, bits 23 to 16 specify this parameter. The default value for REP_T is 0x00.

3.2.2.7 DIP4_UnLock

DIP4_UnLock is a TX SPI4-2 parameter specifying the number of consecutive incorrect DIP4 fields to be detected in order to declare loss of synchronization and drive TSTAT[1:0] bus with framing. In Table 82, “SPI4-2 TX Synchronization Register (Addr: 0x703)” on page 118, bits 7 to 4 specify this parameter. The default value for DIP4_UnLock is 0x4.

3.2.2.8 DIP4_Lock

DIP4_Lock is a TX SPI4-2 parameter specifying the number of consecutive correct DIP4 fields to be detected in order to declare synchronization achieved and enable the calendar sequence. In Table 82, “SPI4-2 TX Synchronization Register (Addr: 0x703)” on page 118, bits 3 to 0 specify this parameter. The default value for DIP4_Lock is 0x5.

3.2.2.9 MaxBurst1

MaxBurst1 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “starving”. Bits 24 to 16 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst1 is 0x006, indicating a MaxBurst1 of 96 bytes [see Section 79, “SPI4-2 RX Burst Size Register (Addr: 0x700)” on page 117].

3.2.2.10 MaxBurst2

MaxBurst2 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “hungry”. Bits 8 to 0 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst2 is 0x002, indicating a MaxBurst1 of 32 bytes (see Section 79, “SPI4-2 RX Burst Size Register (Addr: 0x700)” on page 117).

3.2.3 Training Sequence for Dynamic Phase Alignment (Data Path Deskew)

3.2.3.1 Training at Start-up

The SPI4-2 Specification states that on power-up or after a reset, the training sequence (as defined in the SPI4-2 Specification) is sent indefinitely by the source side until it receives valid FIFO status on the FIFO bus. The specification also states that it is possible for the bus deskew to be completed after one training sequence takes place. Due to some inadequacies in the specification, it is unlikely that the bus can be deskewed in a single training sequence because of the presence of both random and deterministic jitter. The only way to account for the random element is to determine an average over repeated training sequences. Since the required number of repeats is dependent on several characteristics of the system in which the IXF1110 is being used, power on training (or training following loss of synchronization) will continue until synchronization is achieved and the calendar is provisioned. The length of power on training will not be a fixed number of repeats.

The number of training sequence repeats could be fairly large (16, 32, or 64). If this is necessary every time training is required, a significant use of interface bandwidth is needed just to train and deskew the data path. This is only done at power-up or reset for an optimal starting point interface. After this, periodic training provides a better adjustment and a substantially lower bandwidth overhead.

3.2.3.2 Periodic Training

A scheduled training sequence is sent at least once every pre-configured bounded interval (DATA_MAX_T) on both the transmit and receive paths. These training sequences are used by the receiving end of each interface for deskewing bit arrival times on the data and control lines. The sequence allows the receiving end to correct for relative skew difference of up to +/- 1 bit time. The training sequence consists of one (1) idle control word followed by one or more repetitions of a 20-word training pattern consisting of 10 (repeated) training-control words.

The initial idle control word removes dependencies of the DIP-4 in the training control words from preceding data words. Assuming a maximum of +/- bit time alignment jitter on each line, and a maximum of +/- bit time relative skew between lines, there are at least eight bit times when a receiver can detect a training control word prior to deskew. The training data word is chosen to be orthogonal to the training control word. In the absence of bit errors in the training pattern, a receiver should be able successfully to deskew the data and control lines with one training pattern. The sending side of the data path on both the transmit and receive interfaces must schedule the training sequence at least once every DATA_MAX_T cycles.

Note: DATA_MAX_T may be set to zero, disabling periodic training on the interface (refer to Table 80, “SPI4-2 RX Training Register (Addr: 0x701)” on page 117). This is done when a system shows very little drift during normal operation, and no fine-grain correction on an on-going basis is needed. This allows the maximum possible bandwidth for data transfer. The transmit and receive interface training sequences are scheduled independently.

3.2.3.3 Training in a Practical Implementation

The OIF Standard states that it should be possible to train and deskew the data input in a single training cycle. However, from the research carried out and the variances in jitter and skew due to board layout and clock tolerance issues, some sort of averaging over several repeated training patterns is required to reliably determine the optimal point at which to capture the incoming data. This is true for both static alignment and dynamic phase alignment. Therefore, several training patterns are required for an average. The more training patterns, the more accurate the average.

The deskew circuit in the IXF1110 uses dynamic phase alignment with a typical averaging requirement of 32 training patterns required to deliver a reliable result. During power-on training, an unlimited number of training cycles is sent by the data sourcing device. (The standard states that training must be sourced until a calendar has been provisioned.) In the IXF1110, the deskew circuit waits until completion of its programmed average over the training patterns, ensuring that the required number of good DIP-4s is seen. Only then is a calendar provisioned.

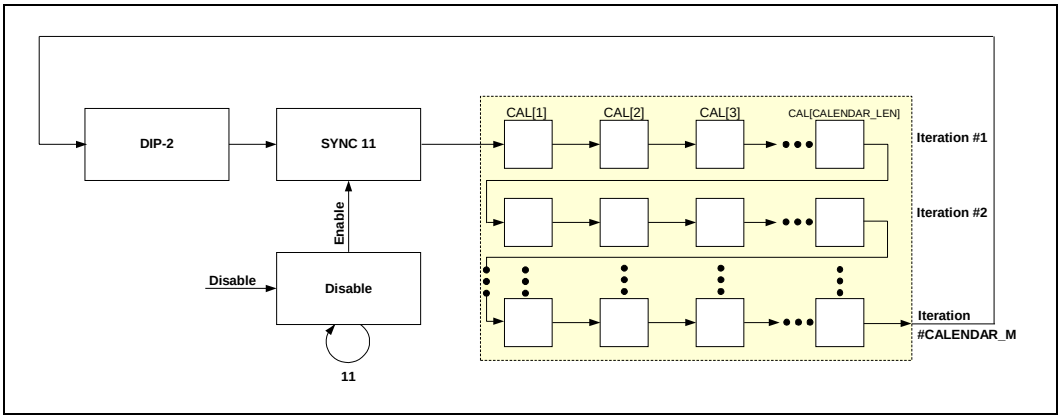
During periodic training, it is important to ensure that the training result is no less accurate than that already used for the initial decision during power-on training. Thus, a similar number of training cycles must be averaged over (32). This could make the overhead associated with periodic training large if it is required to be carried out too often. We therefore recommend that periodic training be scheduled infrequently (DATA_MAX_T = a large number) and that the number of repetitions of training be = 32(α).

3.2.4 FIFO Status Channel

FIFO status information is sent periodically over the TSTAT link from the IXF1110 to the upper layer processor device, and over the RSTAT link from the link processor to the IXF1110. The status channels operate independently.

Figure 8 shows the operation of the FIFO status channel. The sending side of the FIFO status channel is initially in the DISABLE state and sends the “1 1” pattern repeatedly. When FIFO status transmission is enabled, there is a transition to the SYNC state and the “1 1” framing pattern is sent. FIFO status words are then sent according to the calendar sequence, repeating the sequence CALENDAR_M times, followed by the DIP-2 code.

Figure 8. FIFO Status State Diagram

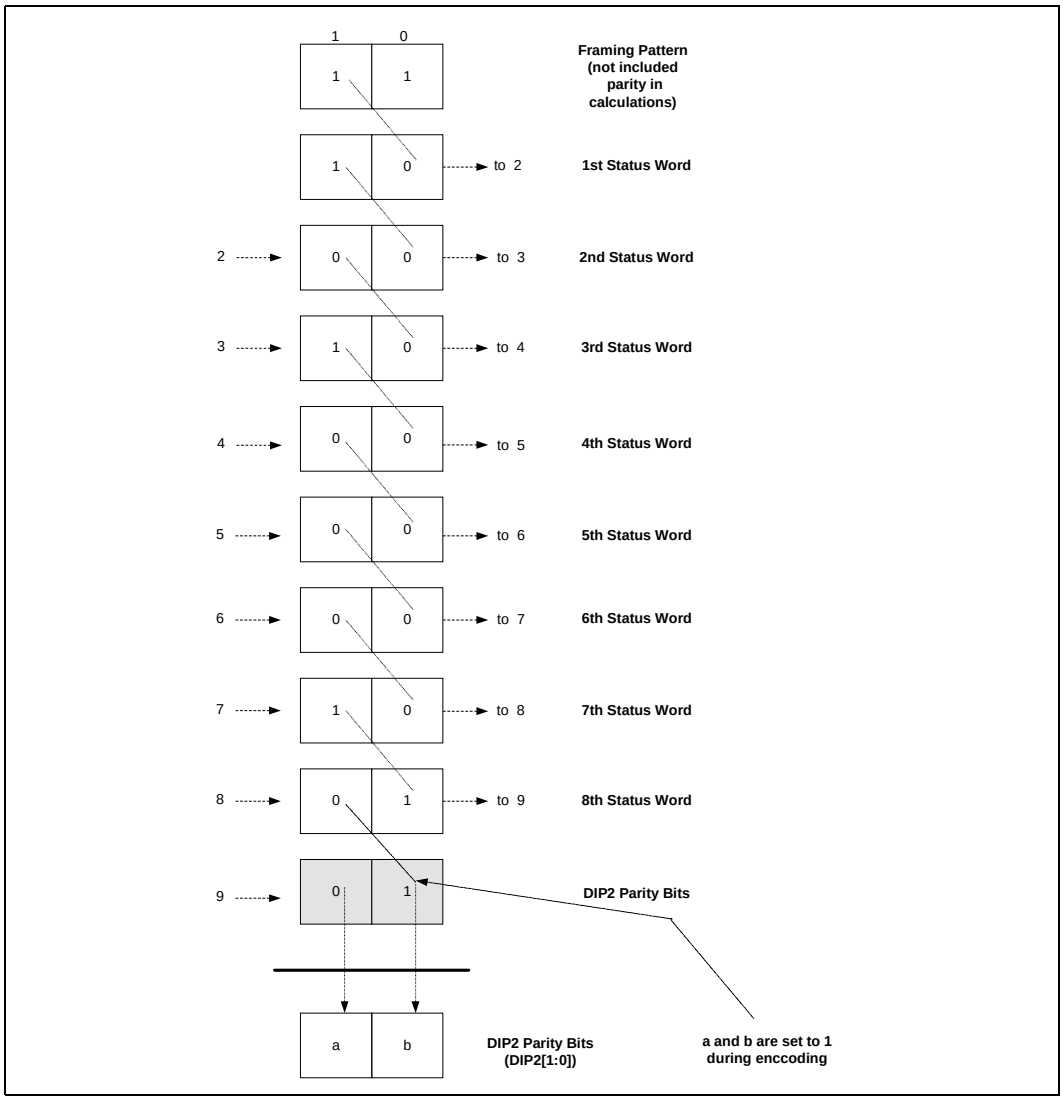


The FIFO status of each port is encoded in a 2-bit data structure, which is defined in Table 8, “FIFO Status Format” on page 34. The most significant bit of each port status is sent over TSTAT[1]/RSTAT[1] and the least significant bit is sent over TSTAT[0]/RSTAT[0]. The “1 1” pattern is reserved for In-band framing, which must be sent once prior to the start of the FIFO status sequence.

Immediately before the “1 1” framing pattern, a DIP-2 odd parity checksum is sent at the end of each complete sequence. The DIP-2 code is computed over all preceding FIFO status indications sent after the last “1 1” framing pattern and diagonally over TSTAT[1]/RSTAT [1] and TSTAT[0]/ RSTAT[0], as shown in Figure 9 on page 33. The first word is at the top of the figure and the last word is at the bottom. The parity bits are computed by summing diagonally. Bits a and b in line 9

correspond to the space occupied by the DIP-2 parity bits and are set to 1 during encoding. The “1 1” framing pattern is not included in the parity calculation. The procedure described applies to either parity generation on the egress path or to check parity on the ingress path.

Figure 9. Example of DIP-2 Encoding



While the parity bits mimic the “1 1” pattern, the receiving end still frames successfully by syncing onto the last cycle in a repeated “1 1” pattern, and by making use of the configured sequence length when searching for the framing pattern.

To permit more efficient FIFO utilization, the MaxBurst1 and MaxBurst2 credits are granted and consumed in increments of 16-byte blocks. For any given port, these credits correspond to the most recently received FIFO status. They are not cumulative and supersede previously granted credits for the given port. A burst transfer shorter than 16 bytes (for example, an end-of-packet fragment) consumes an entire 16-byte credit.

A continuous stream of repeated “1 1” framing patterns indicates a disabled status link. For example, it may be sent to indicate that the data path deskew is not yet completed or confirmed. When a repeated “1 1” pattern is detected, all outstanding credits are cancelled and set to zero.

Table 8. FIFO Status Format

MSB	LSB	Description
1	1	Reserved for framing or to indicate a disabled status link.
1	0	SATISFIED: Indicates that the corresponding port’s FIFO is almost full. When SATISFIED is received, only transfers using the remaining previously granted 16-byte blocks (if any) may be sent to the corresponding port until the next status update. No additional transfers to that port are permitted while SATISFIED is indicated.
0	1	HUNGRY: When HUNGRY is received, transfers for up to MaxBurst2 16-byte blocks, or the remainder of what was previously granted (whatever is greater), may be sent to the corresponding port until the next status update.
0	0	STARVING: Indicates that buffer underflow is imminent in the corresponding PHY port. When STARVING is received, transfers for up to MaxBurst1 16-byte blocks may be sent to the corresponding port until the next status update

The indicated FIFO status is based on the latest available information. A STARVING indication provides additional feedback information, so that transfers are scheduled accordingly. Applications that do not distinguish between HUNGRY and STARVING may only examine the most significant FIFO status bit.

Note: If a port is disabled on the IXF1110, FIFO status for the port is set to SATISFIED to avoid the possibility of any data being sent to it by the controlling device. This applies to the IXF1110 transmit path.

Upon reset, the FIFOs in the data path receiver are emptied, and any outstanding credits are cleared in the data path transmitter. After reset, and before active traffic is generated, the data transmitter sends continuous training patterns. Transmission of the training patterns continues until valid information is received on the FIFO Status Channel. The receiver ignores all incoming data until it has observed the training pattern and acquired synchronization with the data. Synchronization may be declared after a provisional number of consecutive correct DIP-4 code words is seen. Loss of synchronization may be reported after a provisional number of consecutive DIP-4 code words is detected. [For details, see Table 82, “SPI4-2 TX Synchronization Register (Addr: 0x703)” on page 118.]

As stated above, the DIP-4 thresholds are programmable. However, there is a potential issue where it is possible that a given link showing DIP-4 errors may never lose synchronization and re-train to fix the issue. This would mean an on-going and potentially significant loss of data on the link affecting all ports transferring data at that time.

This issue may be seen in two instances:

- During training (most likely periodic training)
- During data transfers where each of the data transfers (MaxBurst1 or MaxBurst2) are separated by more than one idle control word

The mechanism for both issues is the same because data will not change during a repeated period of the same control word being transmitted on the link. If there have been some consecutive DIP-4 errors, they will be incremented towards the Loss-of-Sync threshold. This is most likely to occur from a path requiring deskew. If either a stream of idles or training control words follow the burst and the DIP-4 associated with each of the words is checked, only the first one and the last one will be seen as invalid. Any other control words in the middle will be seen as having a valid DIP-4 and will reset the Loss-of-Sync threshold counter back to zero.

In order to avoid this, the IXF1110 has altered the way in which the check is done for idle control words and training control words. We now only validate the first occurrence of the DIP-4 in both training control words and idle control words for correctness. We do still check each of the words but only use the first occurrence to clear the DIP-4 error counter. Any DIP-4 error in any of these words is still counted towards the Loss-of-Sync threshold counter. It is now impossible to mask the DIP-4 error on our interface.

3.2.5 DC Parameters

For DC parameters on the SPI4-2 interface, please refer to Table 17, “LVTTL I/O Electrical Characteristics” on page 59 and Table 18, “LVDS I/O Electrical Characteristics” on page 59.

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3.3 SerDes Interface

3.3.1 Introduction

The following sections describe the operations supported by each SerDes interface, the configurable options, and register bits that control these options. (A full list of the register addresses and full bit definitions are found in the Register Map (Table 37, “SerDes Block Register Map” on page 81).

The IXF1110 includes ten SerDes interfaces that allow direct connection to optical modules and remove the requirement for external SerDes devices. This increases integration, which reduces the PCB real-estate to implement this function, reduces both silicon and manufacturing costs, and improves reliability.

Each SerDes interface is identical and fully compliant with the relevant IEEE 802.3 Specifications, including auto-negotiation. Each port is also compliant with and supports the requirements of the SFF Committee Gigabit Interface Converter (GBIC) Standards (SFF-8053, revision 5.5).

3.3.2 Features

The SerDes cores are designed to operate in point-to-point data transmission applications. While the core can be used across various media types, such as PCB or backplanes, it is configured specifically for use in 1000BASE-X Ethernet fiber applications in the IXF1110. The following features are supported.

- 10-bit data path, which connects to the output/input of the 8B/10B encoder/decoder PCS that resides in the MAC controller
- Line-clock frequency of 1.25 GHz
- Low power: <200 mW per SerDes channel
- Asynchronous clock data recovery

3.3.3 Functional Description

3.3.3.1 Transmitter Operational Overview

The transmit section of the IXF1110 has to serialize the Ten Bit Interface (TBI) data from the IXF1110 MAC section and outputs this data at 1.25 GHz differential PECL signal levels. The 1.25 GHz differential PECL signals are compliant with SFF-8053 Specification for GBIC Rev 5.5.

The transmitter section takes the contents of the data register within the MAC and synchronously transfers the data out, ten bits at a time Most Significant Bit (MSB) first, followed by the next Least Significant Bit (LSB). When these ten bits have been serialized and have been transmitted the next word of 10 bit data from the MAC is then ready to be serialized for transmission.

The data is transmitted by the high-speed current mode differential PECL output stage using an internal 1.25 GHz clock generated from the 125 MHz clock input.

3.3.3.2 Receiver Operational Overview

The receiver structure performs Clock and Data Recovery (CDR) on the incoming serial data stream. The quality of this operation is a dominant factor for the Bit Error Rate (BER) system performance. Feed forward and feedback controls are combined in one receiver architecture for enhanced performance. The data is over-sampled and a digital circuit detects the edge position in the data stream. A signal is not generated if an edge is not found. A feedback loop takes care of low-frequency jitter phenomenon of unlimited amplitude, while a feed forward section suppresses high-frequency jitter having limited amplitude. The static edge position is held at a constant position in the over-sampled by a constant adjustment of the sampling phases with the early and late signals.

3.4 Gigabit Interface Converter

3.4.1 Introduction

This section describes the connection of the IXF1110 ports to a Gigabit Interface Converter (GBIC) module, and the connections supported for correct operation are detailed. The registers used to write control and read status information are documented (refer to Section 6.5.9, "GBIC Block Register Overview" on page 121).

The GBIC interface allows the IXF1110 a seamless connection to the GBIC modules that form the system's physical media connection, eliminating the need for any FPGAs or CPUs to process data. All required information of the GBIC modules is available to the system CPU via the IXF1110 CPU interface, leading to a more integrated, reliable, and cost-effective system.

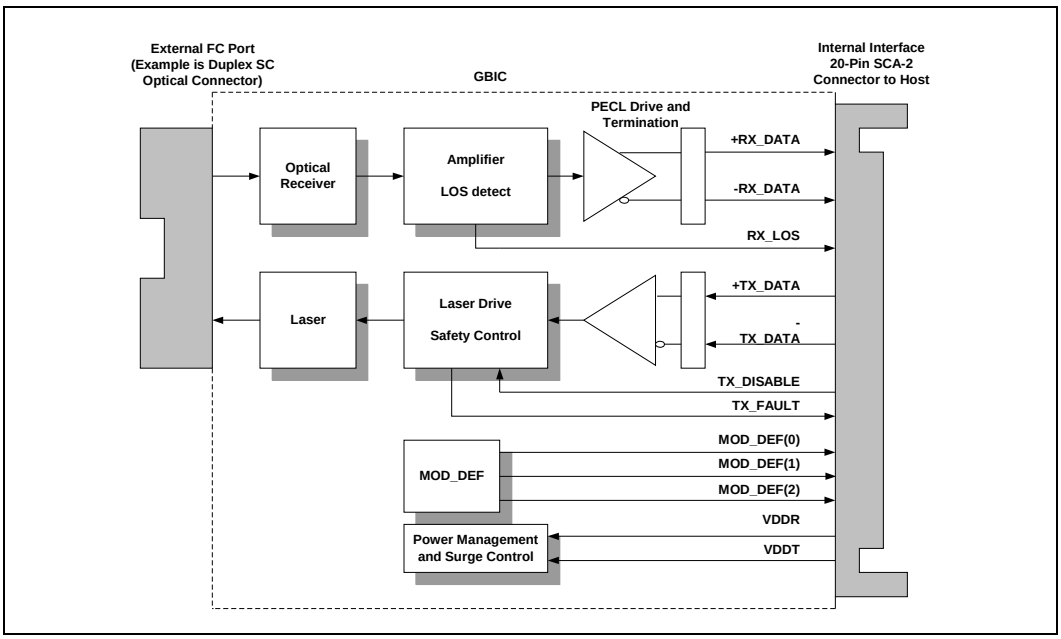
3.4.2 GBIC Description

GBICs were originally designed for fiber channel applications using the Fiber Channel Arbitrated Loop (FC-AL). The design is practical for point-to-point fiber channel implementations and for other high-performance serial technologies, including 1000 Mbps Ethernet.

There are specific mechanical and electrical requirements for the size, form factor, and connections supported on all GBICs. There are also specific requirements for each GBIC that supports a particular media requirement or interface configuration. These requirements are detailed in relevant specifications or manufacturers' datasheets.

The IXF1110 supports all the functions required for full compatibility with GBIC modules supporting the SFF Type 4 Module (refer to SFF-8053, revision 5.5). Figure 10 provides typical GBIC module functionality.

Figure 10. Typical GBIC Module Functional Diagram



3.4.3 IXF1110 Supported GBIC Interface Signals

For GBIC interface operation, three supported signal subgroups are required, allowing a more explicit definition of each function and implementation. The three subgroups are as follows:

- High-Speed Serial Interface
- Low-Speed Status Signaling Interface
- I^2C Module Configuration Interface

Table 9 provides descriptions for IXF1110-to-GBIC module connection pins.

Table 9. IXF1110-to-GBIC Connections

IXF1110 Pin Names	GBIC Module Pin Name	Description	Notes
TX_9:0+	+TX_DAT	Transmit Data, Differential PECL	Output from the IXF1110
TX_9:0-	-TX_DAT		
RX_9:0+	+RX_DAT	Receive Data, Differential PECL	Input to the IXF1110
RX_9:0-	-RX_DAT		
I^2C_CLK	MOD_DEF(1)	I^2C_CLK Output from IXF1110 (SCL)	Output from the IXF1110
I^2C_DATA_9:0	MOD_DEF(2)	I^2C_DATA I/O (SDA)	Input/Output
MOD_DEF_9:0	MOD_DEF(0)	MOD_DEF(0) should be TTL Low level during normal operation.	Input to the IXF1110
TX_DISABLE_9:0	TX_DISABLE	Transmitter Disable, Logic High, Open collector compatible	Output from the IXF1110
TX_FAULT_9:0	TX_FAULT	Transmitter Fault, Logic High, Open collector compatible	Input to the IXF1110
RX_LOS_9:0	RX_LOS	Receiver Loss of Signal, Logic High, Open collector compatible	Input to the IXF1110

3.4.4 Functional Descriptions

3.4.4.1 High-Speed Serial Interface

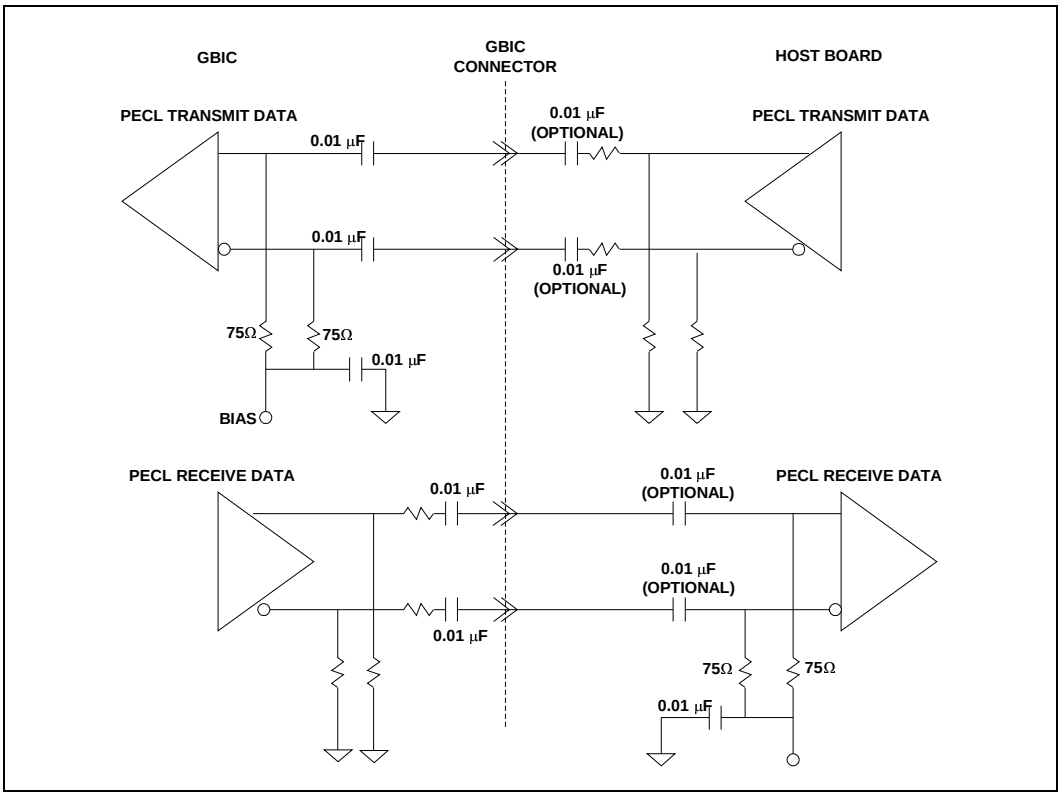
These signals are responsible for transfer of the actual data at 1.25 Gbps. The data is 8B/10B encoded and transmitted differentially at PECL levels per the required specifications. This interface may be either AC or DC coupled (see Table 37, “SerDes Block Register Map” on page 81).

The signals required to implement the high-speed serial interface are:

- TX_9:0+
- TX_9:0-
- RX_9:0+
- RX_9:0-

Figure 11 shows a possible high-speed serial interface implementation (AC-coupled).

Figure 11. Data Path Connection and Termination



3.4.4.2 Low-Speed Status Signaling Interface

The following low-speed signals indicate the state of the line via the GBIC module:

- MOD_DEF_9:0
- TX_FAULT_9:0
- RX_LOS_9:0
- TX_DISABLE_9:0
- MOD_DEF_Int
- TX_FAULT_Int
- RX_LOS_Int

3.4.4.2.1 MOD_DEF_9:0

These signals are direct inputs to the IXF1110 and are pulled to a logic Low level during normal operation, indicating that a module is present for each channel, respectively. If a module is not present, a logic High is received, which is achieved by a pull-up resistor on the IXF1110 pad.

The status of each bit (one for each port) is found in bits 9:0 of the GBIC Status Register (refer to Table 86, “GBIC Status Register Ports 0-9 (Addr: 0x799)” on page 121). Any change in the state of these bits causes a logic Low level on the MOD_DEF_Int output if this operation is enabled.

3.4.4.2.2 TX_FAULT_9:0

These 10 pins are inputs to the IXF1110. These signals are pulled to a logic Low level by the GBIC module during normal operation, which indicates no fault condition exists. If a fault is present, a logic High is received via the use of a pull-up resistor on the IXF1110 pad.

The status of each bit (one for each port) can be found in bits 19:10 of the GBIC Status Register (see Table 86, “GBIC Status Register Ports 0-9 (Addr: 0x799)” on page 121). Any change in the state of these bits causes a logic Low level on the TX_FAULT_Int output if this operation is enabled.

3.4.4.2.3 RX_LOS_9:0

These 10 pins are inputs to the IXF1110. During normal operation, these signals are pulled to a logic Low level by the GBIC module, which indicates that no Loss-of-Signal exists. If a Loss-of-Signal occurs, a logic High is received on these inputs via the use of a pull-up resistor on the IXF1110 pad.

The status of each bit (one for each port) is found in GBIC Status Register bits 29:20 (see Table 86 on page 121). Any change in the state of these bits causes a logic Low level on the RX_LOS_Int output if this operation is enabled.

3.4.4.2.4 TX_DISABLE_9:0

These 10 pins are outputs from the IXF1110. During normal operation, these signals are pulled to a logic Low level by the IXF1110, indicating that the GBIC transmitter is enabled. If the GBIC module transmitter is disabled, these signals are switched to a logic High level. On the IXF1110, these outputs are open-drain types and pulled up by the 4.7k to 10k pull-up resistor at the GBIC module. Each of these signals is controlled via GBIC Control Register bits 9:0, respectively (see Table 87 on page 121).

3.4.4.2.5 MOD_DEF_Int

MOD_DEF_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the MOD_DEF_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the GBIC Status Register takes place (see Table 86 on page 121). The signal then returns to an inactive state.

Note: The MOD_DEF_9:0 inputs shown in Table 86, “GBIC Status Register Ports 0-9 (Addr: 0x799)” on page 121 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

3.4.4.2.6 Tx_FAULT_Int

TX_FAULT_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the TX_FAULT_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the GBIC Status Register takes place (see Table 86 on page 121). The signal then returns to an inactive state.

Note: The TX_FAULT_9:0 inputs shown in Table 86, "GBIC Status Register Ports 0-9 (Addr: 0x799)" on page 121 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

3.4.4.2.7 RX_LOS_Int

RX_LOS_Int is a single output, open-drain type signal, and is active Low. A change in state of any of the Rx_LOS_9:0 inputs causes this signal to switch Low and remain in this state until a Read of the GBIC Status register has taken place. The signal then returns to an inactive state.

Note: The RX_LOS_9:0 inputs shown in Table 86, "GBIC Status Register Ports 0-9 (Addr: 0x799)" on page 121 are synchronized with an internal system clock. This results in a delay from the time the signal is active to the register bit and/or interrupt being set.

Note: MOD_DEF_Int, TX_FAULT_Int, and RX_LOS_Int are open-drain type outputs. With the three signals on the device, the system can decide which GBIC Status Register bits to look at to identify the interrupt condition source port. However, this is achieved at the expense of two device pins.

In systems that cannot support multiple interrupt signals (applications that do not have extra hardware pins), these three outputs can be connected to a single pull-up resistor and used as a single interrupt pin.

3.4.5 I^2C Module Configuration Interface

The I^2C interface is supported on Type 4 SFF GBIC modules. Details of the operation are found in SFF-8053, revision 5.5, Annex D, Module Definition "4" GBIC (Serial Identification). This document details the contents of the registers and addresses accessible on a given GBIC module supporting this interface.

SFF-8053 identifies up to 512 8-bit registers that are accessible in each GBIC. The GBIC interface is Read Only and supports either sequential or random access to the 8-bit parameters. The maximum clock rate of the interface is 100 kHz. All address select pins on the internal E^2PROM are tied Low to give a device address equal to zero (00h).

The specific interface in the IXF1110 supports only a subset of the full I^2C interface, and only the features required to support the GBIC modules are implemented, leading to the following support features:

- Single I^2C_CLK pin connected to all GBIC modules, and implemented to save unnecessary pin use.
- Ten per-port I^2C_DATA pins (I^2C_DATA_9:0) are required due to the GBIC module requirement that all modules must be addressed as 00h.
- The interface is Read Only.
- Due to the single internal GBIC controller, only one GBIC module may be accessed at any one time. Each access contains a single register Read. Since these register accesses will most likely

be done during power-up or discovery of a new module, these restrictions should not affect normal operation.

3.4.5.1 General Description

In the IXF1110, the entire I^2C interface is controlled through a single I^2C Control and Data Register (see Table 88 on page 121). The general operation is described below.

The I^2C Control and Data Register is divided into the following sections:

- 8-bit DataRead from the GBIC
- ReadDataValid bit
- 8-bit DataAddressSelect
- 4-bit PortAddressSelect
- WriteCommand bit
- I^2C Enable bit

When reading data from a given port, the following steps must be followed (see the following note for clarity).

- Write to the I^2C Data and Control Register with port and register addresses
- Poll I^2C Data and Control Register for “ReadDataValid” status

Note: EXAMPLE: Read the data stored at Port 5 (PortAddressSelect), Register 00h (DataAddressSelect) which is the Identifier field used to determine the type of serial transceiver.

1. Program the I^2C Data and Control Register with the following information:
   a. DataRead = 00h
   b. ReadDataValid = 00h
   c. DataAddressSelect = 00h
   d. PortAddressSelect = 05h
   e. WriteCommand = 01h
   f. I^2CEnable = 01h

   This data is written into the I^2C Data and Control Register in a single cycle via the CPU interface.
2. When this register is written and the WriteCommand bit is at a Logic 1, the I^2C access state machine examines the PortAddressSelect and enables the I^2C_DATA_0:9 output for the selected port.
3. Next, the state machine uses the data in the DataAddressSelect field to build the data frame to be sent to the GBIC.
4. The I^2C DATA_READ_FSM internal state machine then takes over the task of transferring the actual data between the IXF1110 and the selected GBIC (refer to the details in Section 3.4.5.2, “I2C Protocol Specifics” on page 44).
5. The I^2C DATA_READ_FSM internal state machine places the received data into the DataRead field in the I^2C Data and Control Register. It also sets the ReadDataValid bit to a Logic 1 to signify that the Read data is valid.

6. The data is read through the CPU interface. The CPU must poll this register once a Write command has been issued to retrieve the data. An implementation-specific time is required to complete the detailed GBIC register access.

Note: Only one GBIC I^2C access sequence can be run at any given time. If a second Write is carried out to the I^2C Data and Control Register before a result is returned for the previous Write, the data for the first Write is lost. An internal state machine completes the GBIC register access for the first Write. It attempts to place the data in the DataRead field and checks to see if the WriteCommand bit is 00h. If it is not 00h, it throws the data away and signals the I^2C access state machine to begin a new cycle using the data from the second Write.

3.4.5.2 I^2C Protocol Specifics

This section describes the I^2C protocol behavior supported by the IXF1110, which is controlled by an internal state machine. Specific protocol states are defined below, with an additional description of the hardware pins used on the interface.

The Serial Clock Line (I^2C_CLK) is an output from the IXF1110. The serial data is synchronous with this clock and is driven off the rising edge by the IXF1110 and off the falling edge by the GBIC module. The IXF1110 has only one I^2C_CLK line that drives all of the GBIC modules. I^2C_CLK runs continuously when enabled (I^2C Enable = 01h0).

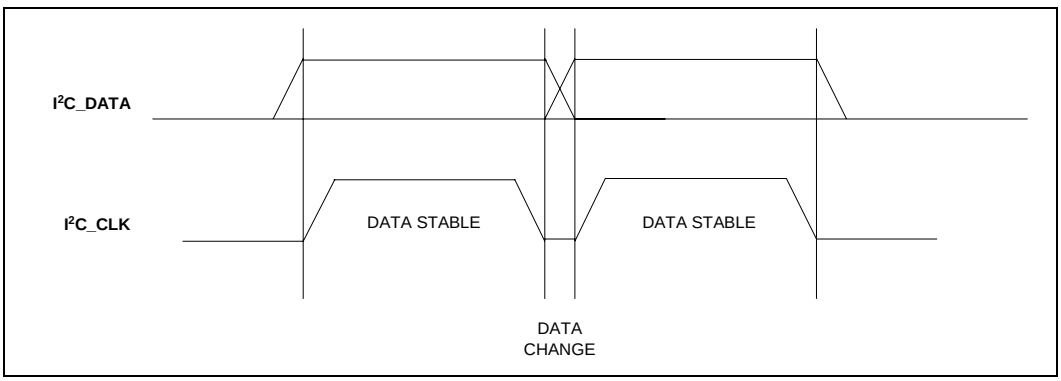
The Serial Data (I^2C_DATA_0:9) pins (one per port) are bi-directional for serial data transfer, and are open drain.

3.4.5.3 Port Protocol Operation

3.4.5.4 Clock and Data Transitions

The I^2C_DATA is normally pulled High with an extra device. Data on the I^2C_DATA pin changes only during the I^2C_CLK Low time periods (see Figure 12). Data changes during I^2C_CLK High periods indicate a start or stop condition.

Figure 12. Data Validity Timing Diagram



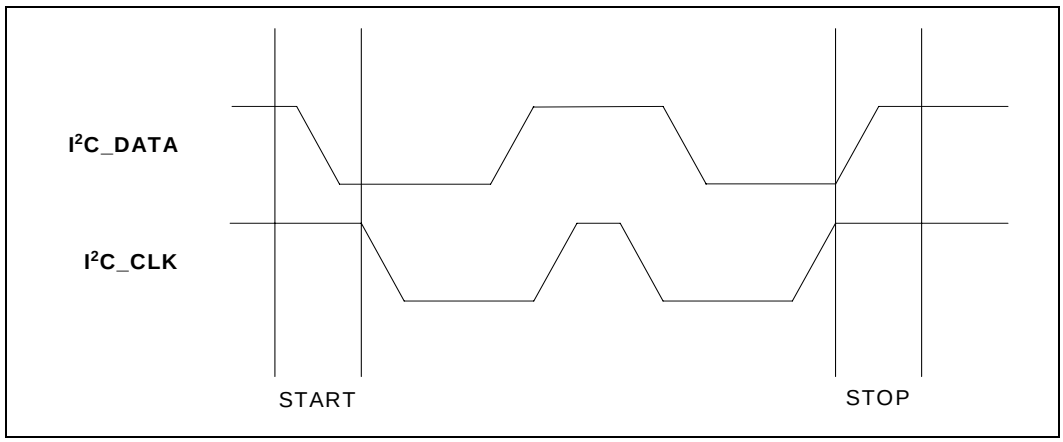
3.4.5.4.1 Start Condition

A High-to-Low transition of I^2C_DATA, with I^2C_CLK High, is a start condition that must precede any other command (see Figure 13).

3.4.5.4.2 Stop Condition

A Low-to-High transition of the I²C_DATA with I²C_CLK High is a stop condition. After a Read sequence, the stop command places the E²PROM in the GBIC in a standby power mode (see Figure 13).

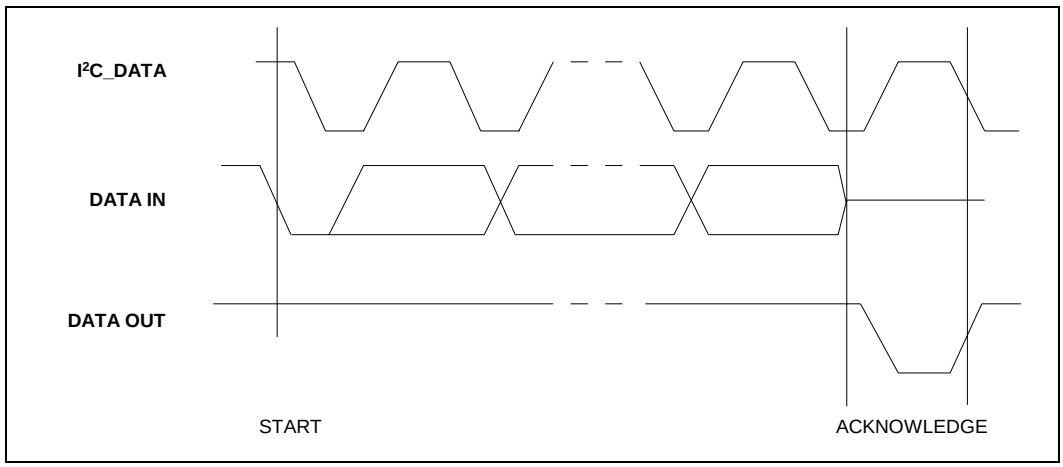
Figure 13. Start and Stop Definition Timing Diagram



3.4.5.4.3 Acknowledge

All addresses and data words are serially transmitted to and from the GBIC in 8-bit words. The GBIC E²PROM sends a zero to acknowledge that it has received each word, which happens during the ninth clock cycle (see Figure 14).

Figure 14. Acknowledge Timing Diagram



3.4.5.4.4 Memory Reset

After an interruption in protocol, power loss, or system reset, any two-wire GBIC can be reset by following three steps:

1. Clock up to 9 cycles
2. Wait for I²C_DATA High in each cycle while I²C_CLK is High

3. Initiate a start condition

Memory reset on this device is defined as follows: After completing steps 1 through 3, there is no clean finish to end the reset of the memory with a start condition, thus, always add a stop condition following the start. This ensures a clean protocol termination if there is no more data to transfer at the end of the reset cycle.

3.4.5.4.5 Device Addressing

All E^2PROMs in GBIC devices require an 8-bit device address word following a start condition to enable the chip to read or write. The device address word consists of a mandatory one, zero sequence for the four most significant bits. This is common to all devices. The next 3 bits are the A2, A1 and A0 device address bits that are tied to zero in a GBIC module. The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is High and a Write operation is initiated if this bit is Low.

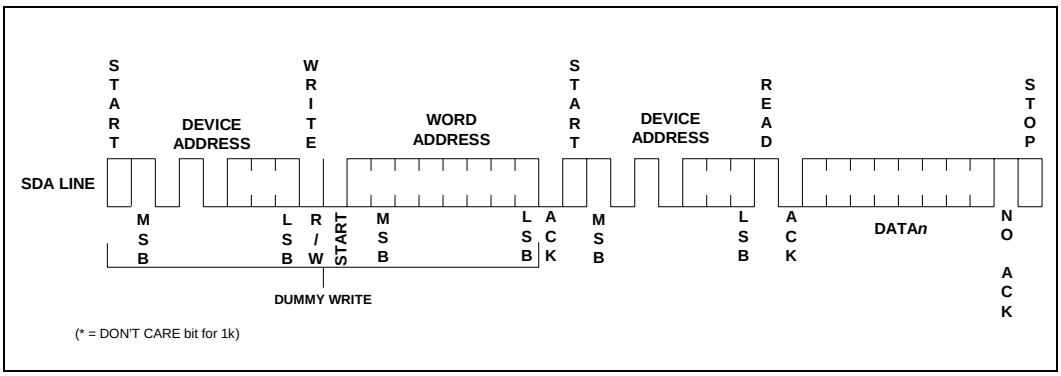
Upon comparison of the device address, the GBIC module outputs a zero. If a comparison is not made, the GBIC E^2PROM returns to a standby state.

3.4.5.4.6 Random Read Operation

A random Read requires a “dummy” Byte/Write sequence to load the data word address. The “dummy” Write is achieved by first sending a device address word with the Read/Write bit cleared to Low, which signals a Write operation. The GBIC acknowledges receipt of the device address word. The IXF1110 sends the data word address, which is again acknowledged by the GBIC. The IXF1110 then generates another start condition. This completes the “dummy” Write and sets the GBIC E^2PROM pointers to the desired location.

The IXF1110 initiates a current address Read by sending a device address with the Read/Write bit set High. The GBIC acknowledges the device address and serially clocks out the data word. The IXF1110 does not respond with a zero but generates a stop condition (see Figure 15).

Figure 15. Random Read



3.4.5.5 AC Timing Characteristics

Table 29, “I2C AC Timing Characteristics” on page 70, Figure 30, “I2C Bus Timing Diagram” on page 70, and Figure 31, “I2C Write Cycle Diagram” on page 70 provide the AC timing characteristics of the GBIC interface.

3.5 LED Interface

3.5.1 Introduction

The IXF1110 uses a serial interface consisting of three signals to provide LED data to some form of external driver. This interface provides the data for 30 separate direct drive LEDs and allows three LEDs per MAC port.

There are two modes of operation, each with its own separate LED decode mapping. Modes of operation and LEDs are detailed in “Modes of Operation”.

3.5.2 Modes of Operation

Mode selection is accomplished by using the LED_SEL_MODE bit. This bit is globally selected and controls the operation of all ports (see Table 65, “LED Control Register (Addr: 0x509)” on page 100).

There are two modes of operation:

Mode 0: (LED_SEL_MODE = 0 [Default]): This mode selects operations compatible with the SGS Thompson M5450 Led Display Driver Device. This device converts the serial data stream, output by the IXF1110, into 30 direct-drive LED outputs.

Mode 1: (LED_SEL_MODE = 1): This mode is used with standard TTL (74LS595) or HCMOS (74HC595) octal shift registers with latches, providing the most general and cost-effective implementation of the serial data stream conversion.

In addition to these physical modes of operation, there are two types of specific LED data decodes available. This option is a global selection and controls the operation of all ports (see Table 65, “LED Control Register (Addr: 0x509)” on page 100).

3.5.3 LED Interface Signal Description

The IXF1110 LED interface consists of three output signal pins that are 2.5V CMOS level pads. Table 10 provides LED signal names, pin numbers, and descriptions.

Table 10. LED Pin Descriptions

Pin Name	Pin #	Pin Description
LED_CLK	A20	LED_CLK: This signal is an output that provides a continuous clock synchronous to the serial data stream output on the LED_DATA pin. This clock has a maximum speed of 0.5 MHz. The behavior of this signal remains constant in all modes of operation.
LED_DATA	A19	LED_DATA: This signal provides the data, in various formats, as a serial bit stream. The data must be valid on the rising edge of the LED_CLK signal. In Mode 0, the data presented on this pin is TRUE (Logic 1 = High). In Mode 1, the data presented on this pin is INVERTED (Logic 1 = Low).
LED_LATCH	K18	LED_LATCH: This is an output pin and the signal is used only in Mode 1 as the Latch enable for the shift register chain. This signal is not used in Mode 0, and should be left unconnected.

3.5.4 Mode 0: Detailed Operation

Note: Please refer to the SGS Thompson M5450 datasheet for device-operation information.

The operation of the LED Interface in Mode 0 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 16 on page 48 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 16 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the M5450 device.The actual data shown in Figure 16 consists of a chain of 36 bits only, 30 of which are valid LED DATA. The 36-bit data chain is built up as follows:

Figure 16. Mode 0 Timing Diagram

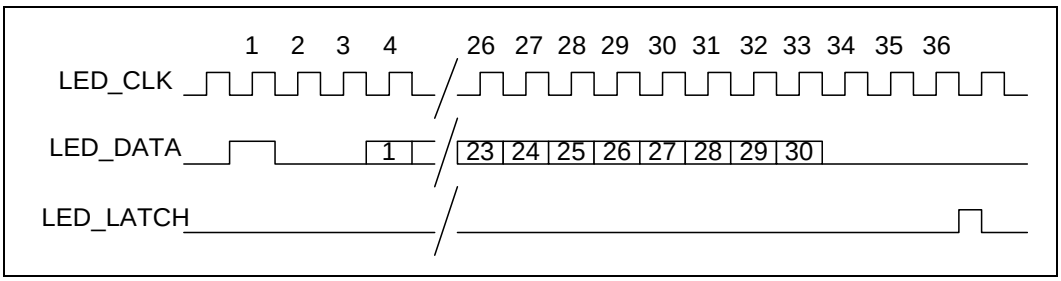


Table 11. Mode 0 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit is used to synchronize the M5450 device to expect 35 bits of data to follow.
2:3	PAD BITS	These bits are used only as fillers in the data stream to extend the length from the actual 30 bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.
4:33	LED DATA 1-30	These bits are the actual data transmitted to the M5450 device. The decode for each individual bit in each mode is defined in Table 10 on page 47. The data is TRUE. Logic 1(LED ON) = High
34:36	PAD BITS	These bits are used as fillers in the data stream to extend the length from the actual 30-bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.

When implemented on a board with the M5450 device, the LED DATA bit 1 appears on output bit 3 of the M5450 and the LED DATA bit 2 appears on output bit 4, etc. This means that output bits 1, 2, 3, 34, and 35 will never have valid data and should not be used.

3.5.5 Mode 1: Detailed Operation

Note: Please refer to manufacturers' 74LS/HC595 datasheet for information on device operation.

The operation of the LED Interface in Mode 1 is again based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. Figure 17 on page 49 shows the basic timing relationship and relative positioning in the data stream of each bit.

Figure 17 shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the Shift Register chain devices.

The LED_LATCH signal is required in Mode 1, and is used to latch the data shifted into the shift register chain into the output latches of the 74HC595 device. As seen in Figure 17, the LED_LATCH signal is active High during the Low period on the 36th LED_CLK cycle. This avoids any possibility of trying to latch data as it is shifting through the register.

When this operation mode is implemented on a board with a shift register chain containing three 74HC595 devices, the LED DATA bit 1 is output on Shift Register bit 1, and so on up the chain. Only Shift Register bits 31 and 32 do not contain valid data. The actual data shown in Figure 17 consists of a 36-bit chain, of which 30 bits are valid LED DATA. The 36-bit data chain is built up as follows:

Note: The LED_DATA signal is now inverted from the state in Mode 0.

Figure 17. Mode 1 Timing Diagram

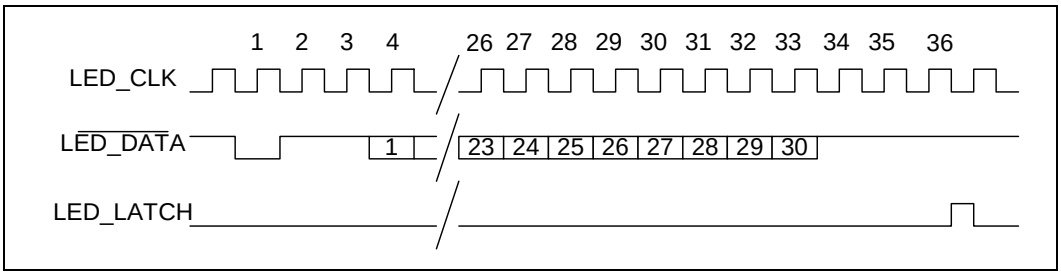


Table 12. Mode 1 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit has no meaning in Mode 1 operation and is shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
2:3	PAD BITS	These bits have no meaning in Mode 1 operation and are shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
4:33	LED DATA 1-30	These bits are the actual data to be transmitted to the 32-stage shift register chain. The decode for each bit in each mode is defined in Table 13 on page 50. The data is INVERTED. Logic 1 (LED ON) = Low.
34:36	PAD BITS	These bits have no meaning in Mode 1 operation and are latched into positions 31 and 32 in the shift register chain. These bits are not considered as valid data and should be ignored. They should always be a Logic 0 = High.

3.5.6 Power-On, Reset, and Initialization

The LED interface is disabled at power-on or reset. The system software controller must enable the LED interface. The internal state machines and output pins are held in reset until the full IXF1110 device configuration is completed. This is done by setting the LED_ENABLE bit to a logic 1 (see Table 65, "LED Control Register (Addr: 0x509)" on page 100). The power-on default for this bit is Logic 0.

3.5.7 LED Data Decodes

Table 13 shows the data decode of the data for the IXF1110.

Table 13. LED Data Decodes

LED_DATA#	MACPORT#	IXF1110 Designation
1	0	Rx LED - Amber
2		Rx LED - Green
3		Tx LED - Green
4	1	Rx LED - Amber
5		Rx LED - Green
6		Tx LED - Green
7	2	Rx LED - Amber
8		Rx LED - Green
9		Tx LED - Green
10	3	Rx LED - Amber
11		Rx LED - Green
12		Tx LED - Green
13	4	Rx LED - Amber
14		Rx LED - Green
15		Tx LED - Green
16	5	Rx LED - Amber
17		Rx LED - Green
18		Tx LED - Green
19	6	Rx LED - Amber
20		Rx LED - Green
21		Tx LED - Green
22	7	Rx LED - Amber
23		Rx LED - Green
24		Tx LED - Green
25	8	Rx LED - Amber
26		Rx LED - Green
27		Tx LED - Green

Table 13. LED Data Decodes (Continued)

LED_DATA#	MACPORT#	IXF1110 Designation
28	9	Rx LED - Amber
29		Rx LED - Green
30		Tx LED - Green

3.5.7.1 LED Signaling Behavior

Operation in each mode for the decoded LED data in Table 13 is detailed in Table 14.

3.5.7.1.1 IXF1110 LED Behavior

Table 14. IXF1110 LED Behavior

Type	Status	Description
RxLED Amber	Off	Port has no link synchronization or remote fault error
	On	Port has a link synchronization error or no optical signal
	Blinking	Port has remote fault
RxLED Green	Off	Port is not enabled
	On	Port has link and is enabled
	Blinking	Port is receiving data
TxLED Green	Off	Port is not transmitting data
	Blinking	Port is transmitting data

3.6 CPU Interface

3.6.1 General Description

The CPU Interface block provides access to registers and statistics in the IXF1110. The interface is asynchronous externally and operates within the 125 MHz clock domain internally. The interface provides access to the following registers:

- MAC Control
- MAC RX Statistics
- MAC TX Statistics
- Global Status and Configuration
- RX Block
- TX Block
- SPI4-2 Block
- SerDes Block
- GBIC Block

3.6.2 Functional Description

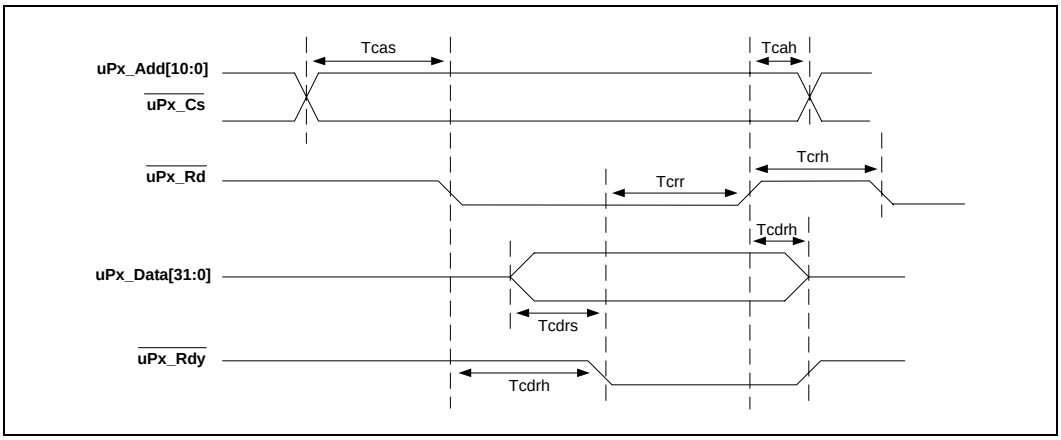
3.6.2.1 Read Access

Read access involves the following:

- Detect assertion of asynchronous Read control signal and latch address
- Generate internal Read strobe
- Drive valid data onto processor bus
- Assert asynchronous-ready signal for required length of time

Figure 18 provides the timing of the asynchronous interface for Read access.

Figure 18. Read Timing Diagram - Asynchronous Interface



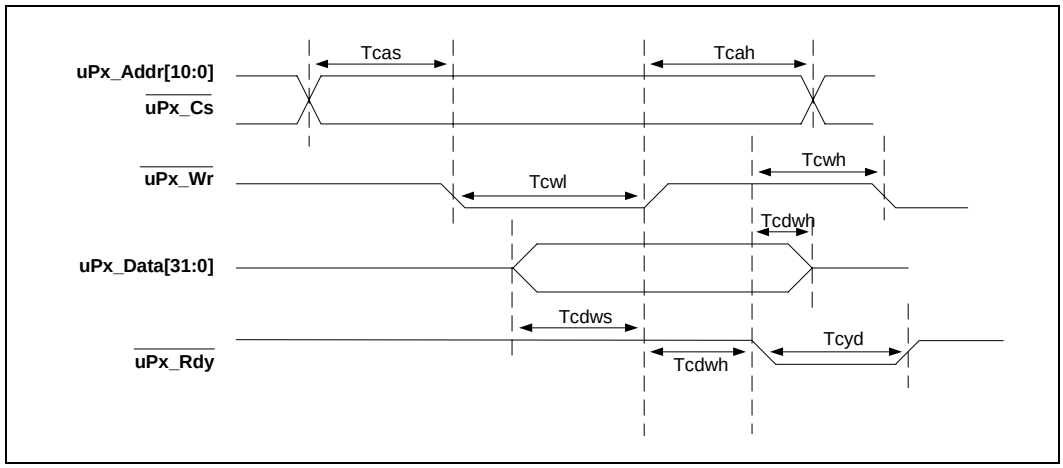
3.6.2.2 Write Access

The Write process involves the following:

- Detect assertion of Asynchronous Write control signal and latch address
- Detect de-assertion of Asynchronous Write control signal and latch data
- Generate internal Write strobe
- Assert Asynchronous Ready signal for required length of time

Figure 19 shows the timing of the asynchronous interface for Write access.

Figure 19. Write Timing Diagram - Asynchronous Interface



3.6.3 Endian

The Endian of the CPU interface may be changed to allow connection of various CPUs to the IXF1110. The Endian selection is determined by setting the Endian bit in the CPU Interface Register (see Table 64 on page 100).

3.7 Clocks

The IXF1110 device has system interface reference clocks, SPI4-2 data path input and output clocks, JTAG input clock, GBIC output clock and LED output clock. All of these clock sources have unique requirements. This section will detail these requirements.

3.7.1 System Interface Reference Clocks

There are two system interface clocks required by the IXF1110 devices.

The system interface clock, which supplies the clock to the majority of the internal circuitry, is the 125 MHz clock. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- +/- 50 ppm
- Maximum duty cycle distortion 40/60

The other system interface clock supplies the clock source for the SPI4-2 receive circuitry. The source of this clock must meet the following specifications.

- 2.5 V CMOS drive
- 1/8 frequency of the SPI4-2 data path frequency
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS.

3.7.2 SPI4-2 Receive and Transmit Data Path Clocks

The SPI4-2 data path clocks are compliant with the OIF 2000.88.4 Specification.

The IXF1110 has the following requirements on the transmit data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable (frequency and level) when reset is removed or when sourced, whichever happens last

The IXF1110 meets the following specifications on the receive data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable when sourced

3.7.3 JTAG Clock

The IXF1110 supports JTAG. The clock source must meet the 2.5 V CMOS specification. The maximum clock input frequency of 11 MHz with a maximum duty cycle distortion of 40/60.

3.7.4 GBIC Clock

The IXF1110 device supports a single output GBIC clock to support all 10 GBIC interfaces. The output meets the 2.5V CMOS specification. The maximum clock frequency as defined by the GBIC specification is 100kHz

3.7.5 LED Clock

The IXF1110 supports a serial LED data stream. This interface implements a 2.5 V CMOS output clock with a maximum frequency of 500 kHz.

4.0 Applications

4.1 TX and RX FIFO Operation

4.1.1 TX FIFO

The IXF1110 TX FIFOs are implemented with 4.5 KB for each channel. This provides enough space for at least one maximum size packet per port storage and ensures that no underrun conditions occur, assuming that the sending device can supply data at the required data rate.

The MAC threshold parameter, which is user programmable, determines when data is transmitted out of the MAC. This parameter is configurable for specific block sizes and the user must ensure that an underrun does not occur. The threshold must be set to a value that exceeds the programmed MaxBurst1 parameter. This method of operation eliminates the possibility of underrun, except when the controlling switch device fails.

4.1.2 RX FIFO

The IXF1110 RX FIFOs are provisioned so that each port has its own 17.0 KB memory space. This is enough memory to ensure that there is never an over-run on any channel while transferring normal Ethernet frame size data.

The FIFOs automatically generate Pause control frames to halt the link partner when the High watermark is reached and to restart the link partner when the data stored in the FIFO falls below the low watermark.

4.2 Reset and Initialization

When powering up the IXF1110, the hardware reset signal, $\overline{\text{Sys\_Res}}$, should be held active Low for a minimum of 100 ns after all of the power rails have fully stabilized to their nominal values and the input clocks have reached their nominal frequency (TDCLK = 400 MHz, CLK125 = 125 MHz, and CLK50 = 50 MHz).

Note: In systems where the $\overline{\text{Sys\_Res}}$ pin is driven from a single board-wide reset signal, the switch or network processor will only come out of reset at the same time as the IXF1110, or possibly later. This means that the TDCLK will not be stable when the $\overline{\text{Sys\_Res}}$ pin is released. In the IXF1110, a built-in feature reactivates the internal reset once TDCLK is applied. It is essential in this case to ensure that the switch or network processor does not output TDCLK until it is stable and has reached its nominal operating frequency.

The IXF1110 extends this hardware reset internally to ensure synchronization of all internal blocks within the system. The internal reset is extended for a minimum of 220 µs after all clocks are stable. Before attempting to access the internal register set via the CPU interface allow for a minimum of 500 µs from all clocks being stable.

At this point, the device is correctly initialized and ready to be used. Clocks start to appear at the relevant device ports and the SPI4-2 interface begins to source a training pattern on the receive side while waiting for a training pattern on the transmit side. The SPI4-2 interface syncs up with the connected switch or network processor per the SPI4-2 Specification.

The CPU accesses can begin to configure the device for any existing user preferences desired. By default all ports on the IXF1110 are enabled after power-up. The device is ready for use at this time if the default settings are to be used. Otherwise, access the required registers via the CPU interface and configure the control registers to the required settings.

5.0 Test Specifications

Table 15 through Table 29 on page 70 and Figure 20 on page 61 through Figure 31 on page 70 represent the target specifications of the following IXF1110 interfaces:

- CPU
- JTAG
- Transmit Pause Control
- GBIC
- Hardware Reset
- LED
- SerDes
- SPI4-2
- I^2C

These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 17 through Table 29 on page 70 apply over the recommended operating conditions specified in Table 16.

Table 15. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage		VDD	-0.3	2.4	Volts
		AVDD	-0.3	2.4	Volts
		VDD2	-0.3	3.0	Volts
		AVDD2	-0.3	3.0	Volts
Operating Temperature	Ambient	TOPA	-15	+85	°C
	Case	TOPC	–	+130	°C
Storage Temperature		TST	-65	-150	°C

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16. Operating Conditions

Parameter		Symbol	Min	Typ[1]	Max	Units
Recommended Supply Voltage		VDD, AVDD	1.71	1.80	1.89	Volts
		VDD2, AVDD2	2.375	2.50	2.625	Volts
Operating Current	1000BASE-SX	IDD and AIDD	–	2.31	–	Amps
		IDD2 and AIDD2	–	0.310	–	Amps
Recommended Operating Temperature	Ambient	TOPA	0	–	70	^{o}C
	Case with Heat Sink	TOPC-HS	0	–	119	^{o}C
	Case without Heat Sink	TOPC-NHS	0	–	118	^{o}C
Power Consumption	1000BASE-SX full-duplex TX and RX at 25 ^{o}C	P	–	4.9	–	Watts

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Table 17. LVTTL I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	VIL	–	–	0.70	V	VCC=MIN
Input High Voltage	VIH	1.7	–	–	V	VCC=MIN
Output Low Voltage	VOL	–	–	0.40	V	VCC=Min, IOL=3.9mA
Output High Voltage	VOH	2.0	–	–	V	VCC=MIN, IOH=-2.9mA
Output Leakage Current	IOZ	–	–	10	µA	VCC=MAX

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Table 18. LVDS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Voltage Range	VI	-0.20	–	VddMax+ 0.20	V	–
Differential Input Voltage	|VID|	100	–	–	mV	@400 MHz
Input Common-Mode Current	ICM	–	–	–	µA	LVDS Input VOS = 1.2 V
Threshold Hysteresis	TH	25	–	–	mV	–
Differential Input Impedance	RIN	85	–	115	Ω	Typical 100 Ω
Output Low Voltage	VOL	0.95	–	–	V	–
Output High Voltage	VOH		–	1.51	V	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Table 18. LVDS I/O Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Differential Output Voltage	|VOD|	330	–	446	mV	–
Delta Differential Output Voltage (Complementary States)	Δ|VOD|	–	–	25	mV	–
Offset (Common-Mode) Voltage	VOS	1.12	–	1.3	V	–
Output Leakage Current	IOZ	–	–	10	µA	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 19. LVPECL I/O Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	VIL	VCC-1.81	–	VCC-1.48	V	–
Input High Voltage	VIH	VCC-1.16	–	VCC-0.88	V	–
Output Low Voltage	VOL	VCC-1.81	–	VCC-1.62	V	–
Output High Voltage	VOH	VCC-1.025	–	VCC-0.88	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20. CPU Port Read Timing Diagram

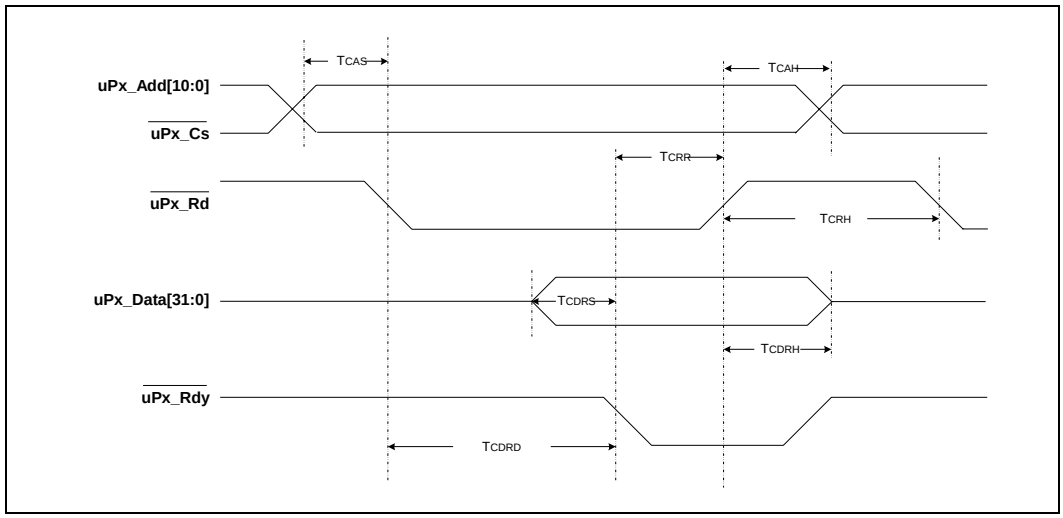


Figure 21. CPU Port Write Timing Diagram

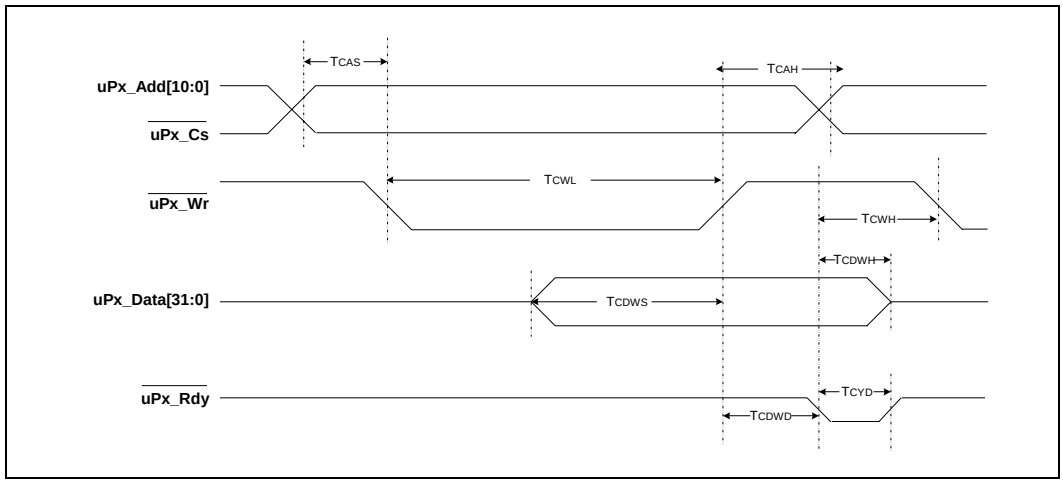


Table 20. CPU Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Test Conditions
uPx_Add[12:0], $\overline{\text{uPx\_Cs}}$ Setup Time	TCAS	10 ns	–	–	–
uPx_Add[12:0], $\overline{\text{uPx\_Cs}}$ Hold Time	TCAH	10 ns	–	–	–
$\overline{\text{uPx\_Rdy}}$ Assertion to $\overline{\text{uPx\_Rd}}$ Deassertion	TCRR	10 ns	–	–	–
$\overline{\text{uPx\_Rd}}$ High Width	TCRH	24 ns (3x cycle)	–	–	–
uPx_Data[31:0] to $\overline{\text{uPx\_Rdy}}$ Setup Time	TCDRS	10 ns	–	–	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 20. CPU Timing Parameters (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Test Conditions
uPx_Data[31:0] to uPx_Rd Hold Time	TCDRH	8 ns	–	32 ns	–
Read uPx_Data[31:0] Driving Delay	TCDRD	24 ns	–	120 ns	–
uPx_Wr Width	TCWL	40 ns	–	–	–
uPx_Rdy to uPx_Wr Hold Time	TCWH	16 ns	–	–	–
uPx_Data[31:0] to uPx_Wr Setup Time	TCDWS	10 ns	–	–	–
uPx_Rdy to uPx_Data[31:0] Hold Time	TCDWH	10 ns	–	–	–
uPx_Data[31:0] Latching Delay	TCDWD	8 ns	–	32 ns	–
uPx_Rdy Width in Write Cycle	TCYD	24 ns	–	40 ns	–
Read uPx_Rdy deassertion to uPx_Wr Assertion	TRTW	32 ns	–	–	–
Write uPx_Rdy deassertion to uPx_Rd Assertion	TWTR	32 ns	–	–	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 22. JTAG Timing Diagram

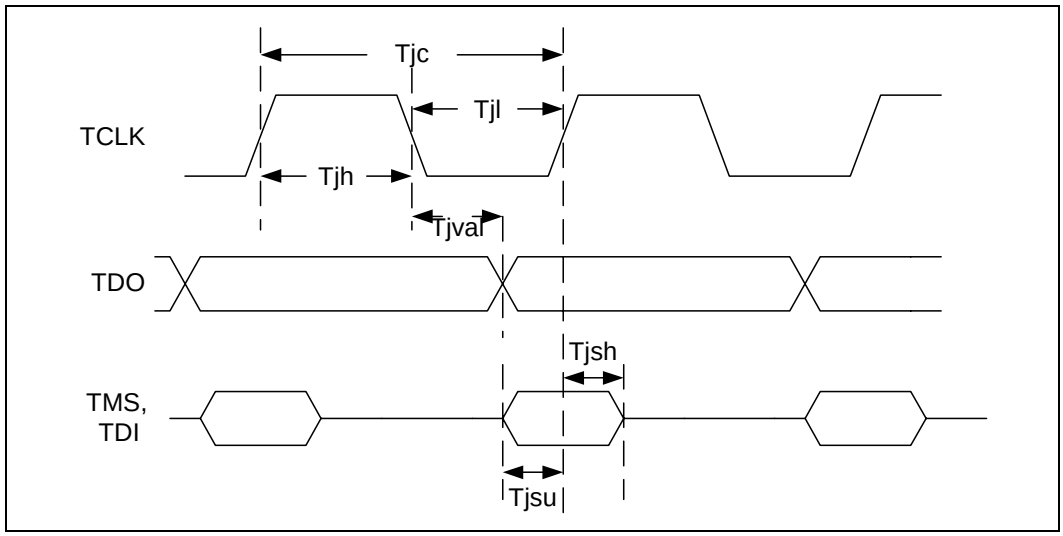


Table 21. JTAG Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TCLK Cycle Time	Tjc	90	–	–	ns	–
TCLK High Time	Tjh	0.4 x Tjc	–	0.6 x Tjc	ns	–
TCLK Low Time	Tjl	0.4 x Tjc	–	0.6 x Tjc	ns	–
TCLK Falling Edge to TDO Valid	Tjval	–	–	25	ns	–
TMS/TDI Setup to TCLK	Tjsu	20	–	–	ns	–
TMS/TDI Hold from TCLK	Tjsh	5	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 23. Transmit Pause Control Interface Diagram

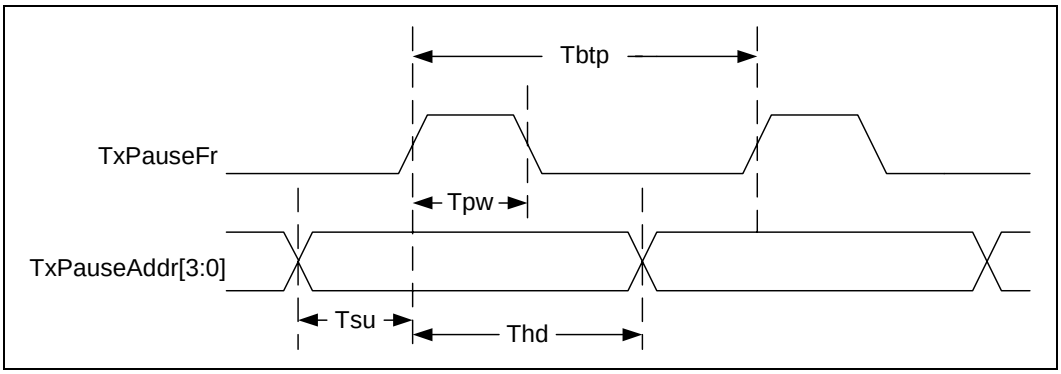


Table 22. Transmit Pause Control Interface Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TxPauseFr Width	Tpw	16	–	–	ns	–
TxPauseAddr[3:0] Setup to TxPauseFr	Tsu	16	–	–	ns	–
TxPauseAddr[3:0] Hold from TxPauseFr	Thd	32	–	–	ns	–
TxPauseFr Pulse to Pulse	Tbtp	48	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 24. GBIC Interrupt Timing

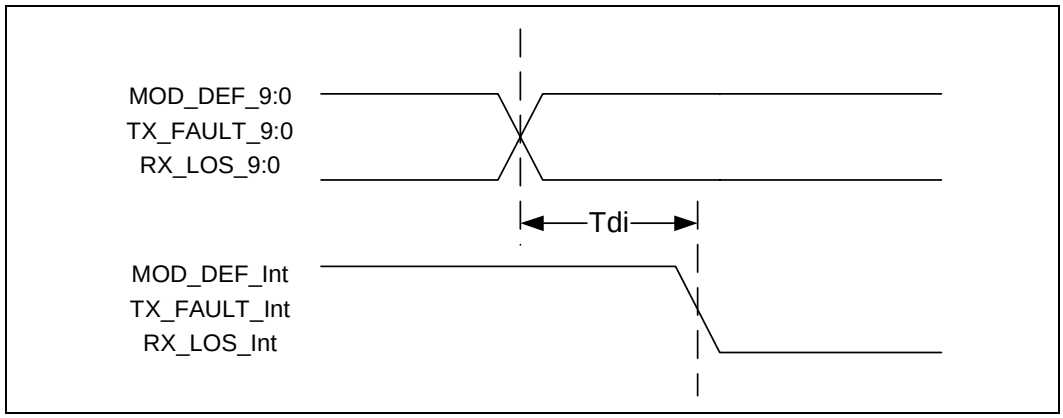


Table 23. GBIC Interrupt Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Change of state on MOD_DEF_9:0 or TX_FAULT_9:0 or RX_LOS_9:0 to assertion (active low) on MOD_DEF_Int or TX_FAULT_Int or RX_LOS_Int	Tdi	24	–	–	–	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 25. Hardware Reset Timing Diagram

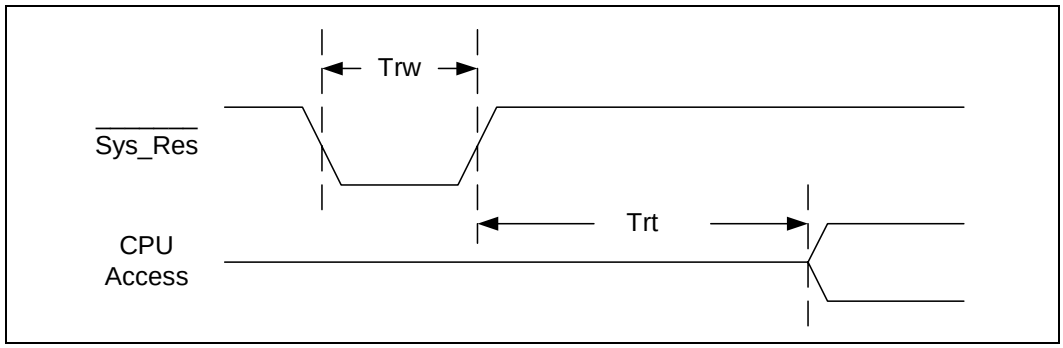


Table 24. Hardware Reset Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Reset Pulse Width	Trw	1	–	–	µs	–
Reset Recovery Time	Trt	200	–	–	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 26. LED Timing Diagram

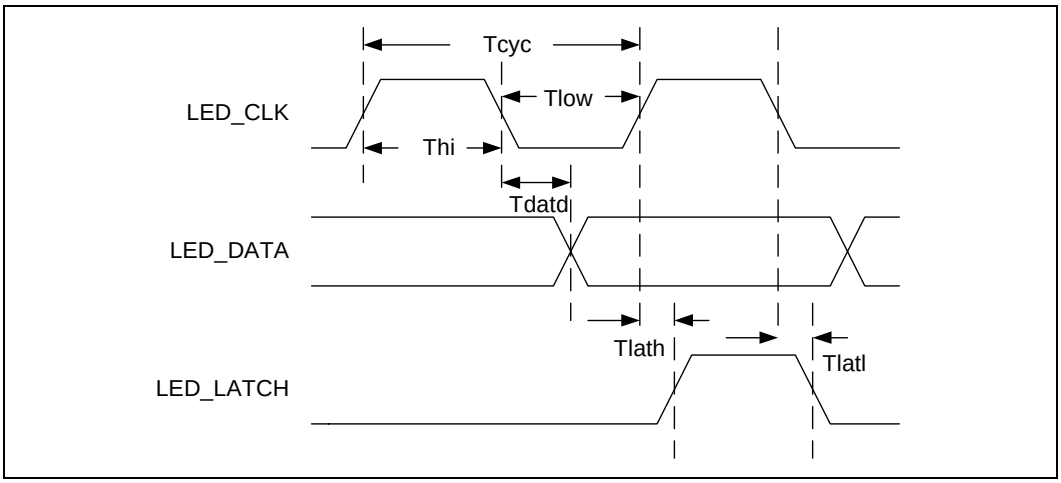


Table 25. LED Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
LED_CLK Cycle Time	Tcyc	2	–	–	µs	–
LED_CLK High Time	Thi	1	–	–	µs	50% duty cycle
LED_CLK Low Time	Tlow	1	–	–	µs	50% duty cycle
LED_CLK Falling Edge to LED_DATA Valid	Tdatd	–	–	–	ns	–
LED_CLK Rising Edge to LED_LATCH Rising Edge	Tlath	–	–	–	ns	–
LED_CLK Falling Edge to LED_LATCH Falling Edge	Tlatl	–	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 27. SerDes Timing Diagram

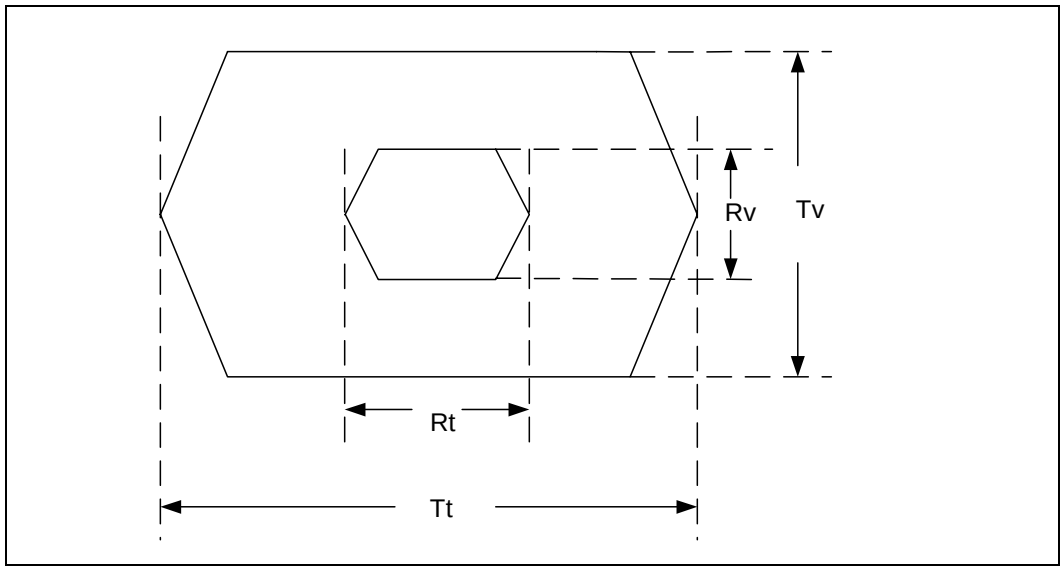


Table 26. SerDes Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit Eye Width	Tt	800	–	–	pS	–
Receive Eye Width	Rt	280	–	–	pS	–
Transmit Amplitude	Tv	1000	–	–	mV	–
Receive Amplitude	Rv	400	–	–	mV	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 28. SPI4-2 Transmit FIFO Status Bus Timing Diagram

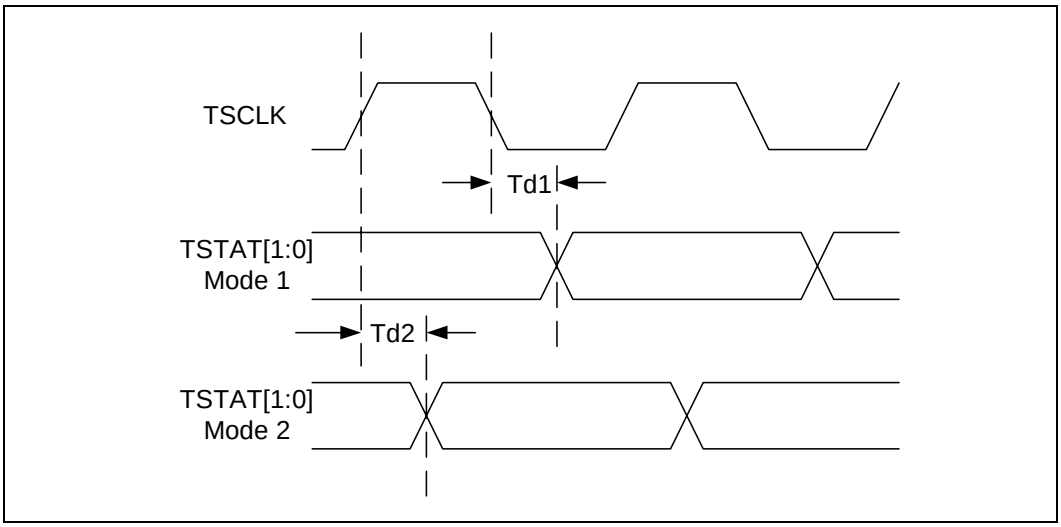


Table 27. SPI4-2 Transmit FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
TSCLK Falling Edge to TSTAT[1:0] Valid (Mode 1)	Td1	–	–	280	ps	–
TSCLK Rising Edge to TSTAT[1:0] Valid (Mode 2)	Td2	–	–	280	ps	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 29. SPI4-2 Receive FIFO Status Bus Timing Diagram

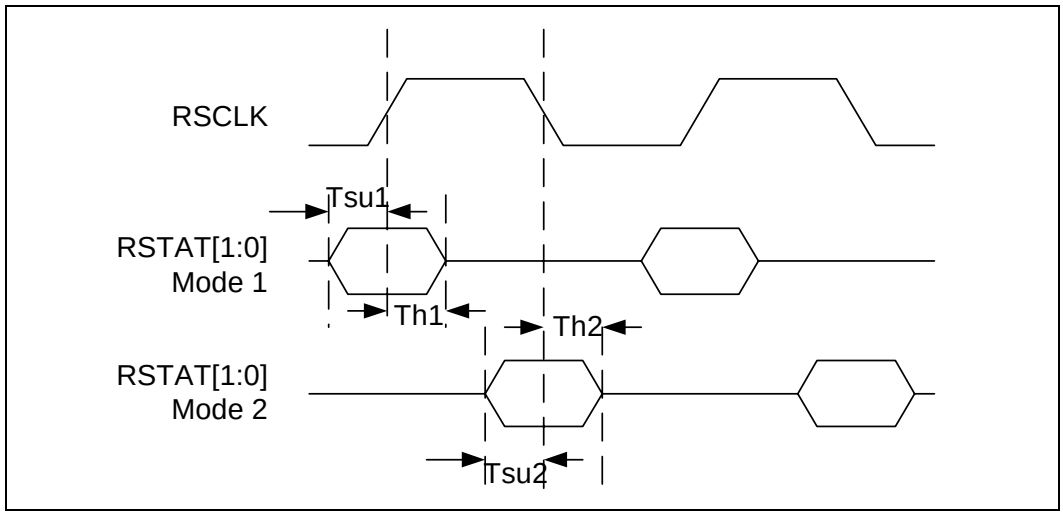


Table 28. SPI4-2 Receive FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
RSTAT[1:0] Setup to RSCLK Rising Edge (Mode 1)	Tsu1	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Rising Edge (Mode 1)	Th1	0.5	–	–	ns	–
RSTAT[1:0] Setup to RSCLK Falling Edge (Mode 2)	Tsu2	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Falling Edge (Mode 2)	Th2	0.5	–	–	ns	–

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.

Figure 30. I²C Bus Timing Diagram

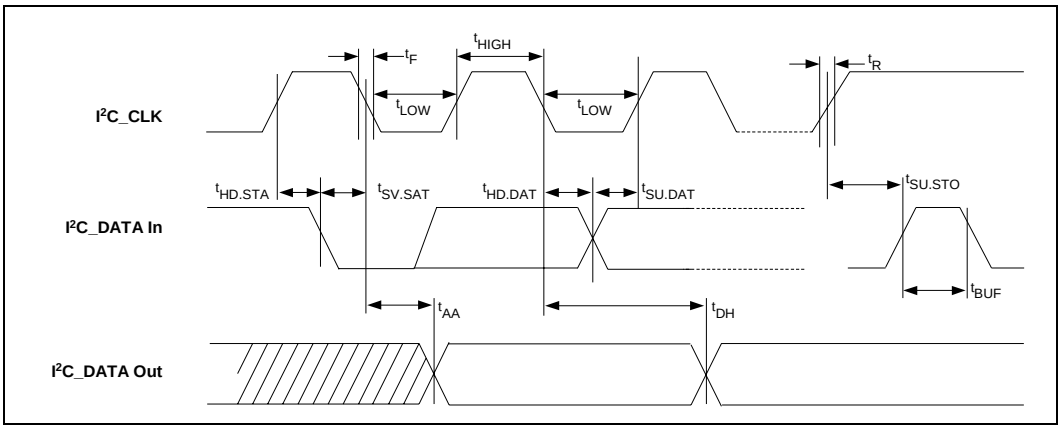


Figure 31. I²C Write Cycle Diagram

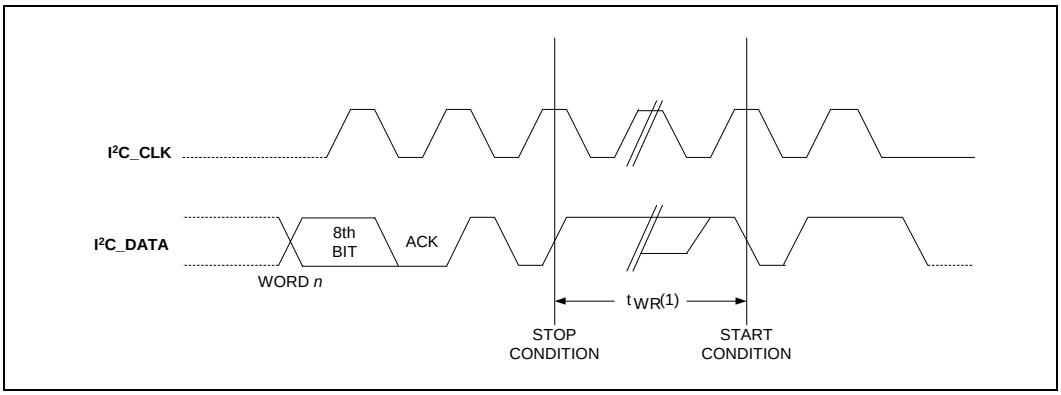


Table 29. I²C AC Timing Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Clock Frequency, SCL	f_{SCL}	–	–	100	kHz	–
Clock Pulse Width Low	t_{LOW}	4.7	–		µs	–
Clock Pulse Width High	t_{HIGH}	4.0	–		µs	–
Noise Suppression	t_I	–	–	100	ns	–
Clock Low to Data Valid Out	t_{AA}	0.1	–	4.5	µs	–
Time bus must be free before a new transmission starts	t_{BUF}	4.7	–	–	µs	–
Start Hold Time	$t_{HD.STA}$	4.0	–	–	µs	–
Start Setup Time	$t_{SU.STA}$	4.7	–	–	µs	–
Data In Hold Time	$t_{HD.DAT}$	0	–	–	µs	–
Data In Setup time	$t_{SU.DAT}$	200	–	–	ns	–
Inputs Rise Time	t_R	–	–	1.0	µs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 29. I²C AC Timing Characteristics (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Inputs Fall Time	t_F	–	–	300	ns	–
Stop Setup Time	$t_{SU.STO}$	4.7	–	–	µs	–
Data Out Hold Time	t_{DH}	100	–	–	ns	–
Write Cycle Time	t_{WR}	–	–	10	ms	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

6.0 Register Definitions

6.1 Introduction

This section provides information on the location and functionality of the control and status registers contained in the IXF1110.

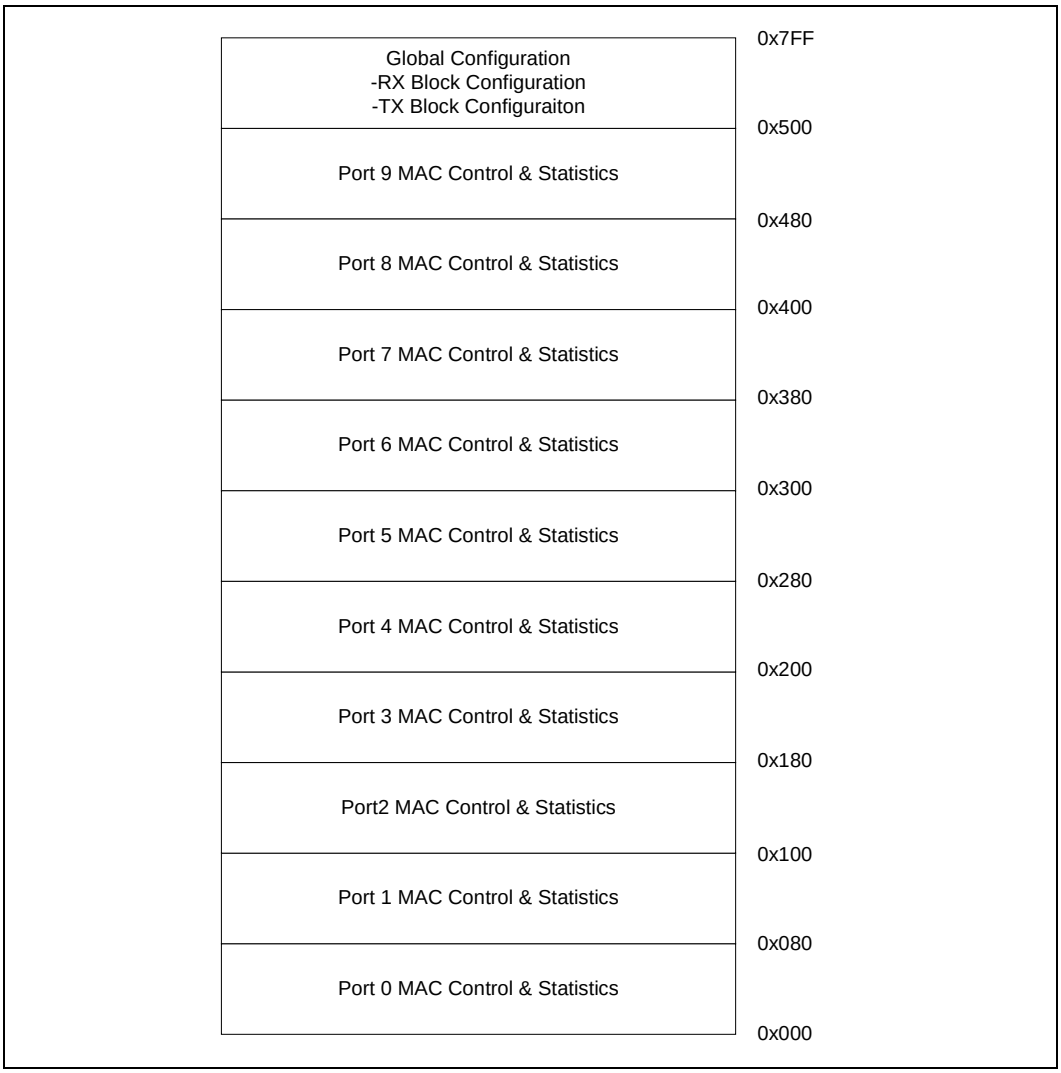
6.2 Document Structure

This document is structured to give a general overview of the register map and an in-depth description of each bit of a register in later sections.

6.3 Graphical Representation

Figure 32 represents an overview of the IXF1110 global control status registers that are used to configure or report on all ports.

Figure 32. Memory Overview Diagram

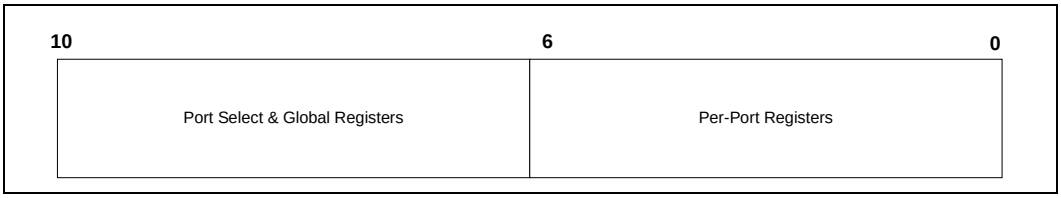


6.4 Per Port Registers

The following section covers all of the registers that are replicated in each of the 10 ports in the IXF1110. These registers perform an identical function in each port.

The address vector for the IXF1110 is 11 bits wide. This allows for 7 bits of port-specific access and a 4-bit vector to address each port and all global registers. The address format is shown in Figure 33.

Figure 33. Register Overview Diagram



6.5 Memory Map

Table 30 through Table 38 on page 82 provide the IXF1110 memory maps. A number of global control and status registers are used to configure or report on all ports, and some registers are replicated on a per-port basis.

Note: All registers in the IXF1110 are 32 bits.

Table 30. MAC Control Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
StationAddressLow	32	R/W	83	0x00
StationAddressHigh	32	R/W	83	0x01
Reserved	32	RO	–	0x02
FDFCType	32	R/W	83	0x03
Reserved	32	RO	–	0x04
Reserved	32	RO	–	0x05
Reserved	32	RO	–	0X06
FCTxTimerValue	32	R/W	83	0x07
FDFCAddressLow	32	R/W	84	0x08
FDFCAddressHigh	32	R/W	84	0x09
IPGReceiveTime1	32	R/W	84	0x0A
IPGReceiveTime2	32	R/W	84	0x0B
IPGTransmitTime	32	R/W	84	0x0C
Reserved	32	R/W	--	0x0D
PauseThreshold	32	R/W	85	0x0E
MaxFrameSize	32	R/W	85	0x0F
Reserved	32	RO	–	0x10
Reserved	32	RO	–	0x11
FCEnable	32	R/W	85	0x12
Reserved	32	RO	–	0x13
ShortRuntsThreshold	32	R/W	85	0x14
DiscardUnknownControlFrame	32	R/W	86	0x15
RxConfigWord	32	R/W	86	0x16
TxConfigWord	32	R/W	87	0x17
DiverseConfig	32	R/W	87	0x18
PacketFilterControl	32	R/W	88	0x19
PortMulticastAddressLow	32	R/W	89	0x1A
PortMulticastAddressHigh	32	R/W	89	0x1B

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 31. MAC RX Statistics Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RxOctetsTotalOK	32	RR	90	0x20
RxOctetsBAD	32	RR	90	0x21
RxUCPckts	32	RR	90	0x22
RxMCPkts	32	RR	90	0x23
RxBCPkts	32	RR	90	0x24
RxPkts64Octets	32	RR	90	0x25
RxPkts65to127Octets	32	RR	90	0x26
RxPkts128to255Octets	32	RR	90	0x27
RxPkts256to511Octets	32	RR	90	0x28
RxPkts512to1023Octets	32	RR	90	0x29
RxPkts1024to1518Octets	32	RR	90	0x2A
RxPkts1519toMaxOctets	32	RR	90	0x2B
FCSErrors	32	RR	90	0x2C
Tagged	32	RR	90	0x2D
RxDataError	32	RR	90	0x2E
AlignErrors	32	RR	90	0x2F
LongErrors	32	RR	90	0x30
JabberErrors	32	RR	90	0x31
PauseMacControlReceivedCounter	32	RR	90	0x32
UnknownMacControlFrameCounter	32	RR	90	0x33
VeryLongErrors	32	RR	90	0x34
RuntErrors	32	RR	90	0x35
ShortErrors	32	RR	90	0x36
CarrierExtendError	32	RR	90	0x37
SequenceErrors	32	RR	90	0x38
SymbolErrors	32	RR	90	0x39

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 32. MAC TX Statistics Register Map

Register	Bit Size	Mode[1]	Ref Page	Offset
MAX TX Statistics Registers (Port Index + Offset)				
OctetsTransmittedOK	32	RR	93	0x40
OctetsTransmittedBad	32	RR	93	0x41
TxUCPkts	32	RR	93	0x42
TxMCPkts	32	RR	93	0x43
TxBCPkts	32	RR	93	0x44
TxPkts64Octets	32	RR	93	0x45
TxPkts65to127Octets	32	RR	93	0x46
TxPkts128to255Octets	32	RR	93	0x47
TxPkts256to511Octets	32	RR	93	0x48
TxPkts512to1023Octets	32	RR	93	0x49
TxPkts1024to1518Octets	32	RR	93	0x4A
TxPkts1519toMaxOctets	32	RR	93	0x4B
DeferredTx	32	RR	93	0x4C
TxTotalCollisions	32	RR	93	0x4D
TxSingleCollisions	32	RR	93	0x4E
TxMultipleCollisions	32	RR	93	0x4F
TxLateCollisions	32	RR	93	0x50
ExcessiveCollisionErrors	32	RR	93	0x51
ExcessiveDeferralErrors	32	RR	93	0x52
TxExcessiveLengthDrop	32	RR	93	0x53
TxUnderrun	32	RR	93	0x54
Tagged	32	RR	93	0x55
CRCError	32	RR	93	0x56
TxPauseFrames	32	RR	93	0x57
FlowControlCollisionsSend	32	RR	93	0x58

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 33. Global Status and Configuration Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
Port Enable	32	R/W	97	0x500
Link LED Enable	32	R/W	98	0x502
Reserved	32	RO	–	0x503
Reserved	32	RO	–	0x504
MAC Soft Reset	32	R/W	99	0x505
Reserved	32	RO	–	0x506
Reserved	32	RO	–	0x507
CPU Interface	32	R/W	100	0x508
LED Control	32	R/W	100	0x509
LED Flash Rate	32	R/W	100	0x50A
LED Fault Disable	32	R/W	100	0x50B
Reserved	32	RO	–	0x50C
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 34. RX Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
RX FIFO High Watermark Port 0	32	R/W	102	0x580
RX FIFO High Watermark Port 1	32	R/W	102	0x581
RX FIFO High Watermark Port 2	32	R/W	102	0x582
RX FIFO High Watermark Port 3	32	R/W	102	0x583
RX FIFO High Watermark Port 4	32	R/W	102	0x584
RX FIFO High Watermark Port 5	32	R/W	102	0x585
RX FIFO High Watermark Port 6	32	R/W	102	0x586
RX FIFO High Watermark Port 7	32	R/W	102	0x587
RX FIFO High Watermark Port 8	32	R/W	102	0x588
RX FIFO High Watermark Port 9	32	R/W	102	0x589
RX FIFO Low Watermark Port 0	32	R/W	103	0x58A
RX FIFO Low Watermark Port 1	32	R/W	103	0x58B
RX FIFO Low Watermark Port 2	32	R/W	103	0x58C
RX FIFO Low Watermark Port 3	32	R/W	103	0x58D
RX FIFO Low Watermark Port 4	32	R/W	103	0x58E
RX FIFO Low Watermark Port 5	32	R/W	103	0x58F
RX FIFO Low Watermark Port 6	32	R/W	103	0x590
RX FIFO Low Watermark Port 7	32	R/W	103	0x591
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 34. RX Block Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Address
RX FIFO Low Watermark Port 8	32	R/W	103	0x592
RX FIFO Low Watermark Port 9	32	R/W	103	0x593
Number of Frames Removed on Port 0	32	RR	104	0x594
Number of Frames Removed on Port 1	32	RR	104	0x595
Number of Frames Removed on Port 2	32	RR	104	0x596
Number of Frames Removed on Port 3	32	RR	104	0x597
Number of Frames Removed on Port 4	32	RR	104	0x598
Number of Frames Removed on Port 5	32	RR	104	0x599
Number of Frames Removed on Port 6	32	RR	104	0x59A
Number of Frames Removed on Port7	32	RR	104	0x59B
Number of Frames Removed on Port8	32	RR	104	0x59C
Number of Frames Removed on Port 9	32	RR	104	0x59D
Reserved	32	RO	–	0x59E
RX FIFO Errored Frames Drop Enable	32	R/W	105	0x59F
RX FIFO Overflow Event	32	RR	107	0x5A0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 35. TX Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO High Watermark Port 0	32	R/W	108	0x600
TX FIFO High Watermark Port 1	32	R/W	108	0x601
TX FIFO High Watermark Port 2	32	R/W	108	0x602
TX FIFO High Watermark Port 3	32	R/W	108	0x603
TX FIFO High Watermark Port 4	32	R/W	108	0x604
TX FIFO High Watermark Port 5	32	R/W	108	0x605
TX FIFO High Watermark Port 6	32	R/W	108	0x606
TX FIFO High Watermark Port 7	32	R/W	108	0x607
TX FIFO High Watermark Port 8	32	R/W	108	0x608
TX FIFO High Watermark Port 9	32	R/W	108	0x609
TX FIFO Low Watermark Port 0	32	R/W	108	0x60A
TX FIFO Low Watermark Port 1	32	R/W	109	0x60B
TX FIFO Low Watermark Port 2	32	R/W	109	0x60C
TX FIFO Low Watermark Port 3	32	R/W	109	0x60D
TX FIFO Low Watermark Port 4	32	R/W	109	0x60E
TX FIFO Low Watermark Port 5	32	R/W	109	0x60F
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 35. TX Block Register Map (Continued)

Register	Bit Size	Mode[1]	Ref Page	Address
TX FIFO Low Watermark Port 6	32	R/W	109	0x610
TX FIFO Low Watermark Port 7	32	R/W	109	0x611
TX FIFO Low Watermark Port 8	32	R/W	109	0x612
TX FIFO Low Watermark Port 9	32	R/W	109	0x613
MAC Transfer Threshold Port 0	32	R/W	111	0x614
MAC Transfer Threshold Port 1	32	R/W	111	0x615
MAC Transfer Threshold Port 2	32	R/W	111	0x616
MAC Transfer Threshold Port 3	32	R/W	111	0x617
MAC Transfer Threshold Port 4	32	R/W	111	0x618
MAC Transfer Threshold Port 5	32	R/W	111	0x619
MAC Transfer Threshold Port 6	32	R/W	111	0x61A
MAC Transfer Threshold Port 7	32	R/W	111	0x61B
MAC Transfer Threshold Port 8	32	R/W	111	0x61C
MAC Transfer Threshold Port 9	32	R/W	111	0x61D
TX FIFO Overflow Event	32	RR	114	0x61E
Reserved	32	RO	–	0x61F
Reserved	32	RO	–	0x620
Info Out of Sequence	32	RR	115	0x621
Number of Frames Removed on Port 0	32	RR	116	0x622
Number of Frames Removed on Port 1	32	RR	116	0x623
Number of Frames Removed on Port 2	32	RR	116	0x624
Number of Frames Removed on Port 3	32	RR	116	0x625
Number of Frames Removed on Port 4	32	RR	116	0x626
Number of Frames Removed on Port 5	32	RR	116	0x627
Number of Frames Removed on Port 6	32	RR	116	0x628
Number of Frames Removed on Port 7	32	RR	116	0x629
Number of Frames Removed on Port 8	32	RR	116	0x62A
Number of Frames Removed on Port 9	32	RR	116	0x62B

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 36. SPI4-2 Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
SPI4-2 Rx Burst Size Register	32	R/W	117	0x700
SPI4-2 Rx Training Register	32	R/W	117	0x701
SPI4-2 Calendar Register	32	R/W	118	0x702
SPI4-2 Tx Synchronization Register	32	R/W	118	0x703
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 37. SerDes Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
Tx and Rx AC/DC Coupling Selection	32	R/W	119	0x780
Reserved	32	RO	–	0x781
Reserved	32	RO	–	0x782
Reserved	32	RO	–	0x783
Reserved	32	RO	–	0x784
Reserved	32	RO	–	0x785
Reserved	32	RO	–	0x786
Tx and Rx Power-Down Ports 0-9	32	R/W	119	0x787
Reserved	32	RO	–	0x788
Reserved	32	RO	–	0x789
Reserved	32	RO	–	0x78A
Reserved	32	RO	–	0x78B
Reserved	32	RO	–	0x78C
Reserved	32	RO	–	0x78D
Reserved	32	RO	–	0x78E
Reserved	32	RO	–	0x78F
Reserved	32	RO	–	0x790
Reserved	32	RO	–	0x791
Reserved	32	RO	–	0x792
Rx Signal Detect Level Ports 0-9	32	RO	120	0x793
Reserved	32	RO	–	0x794
Reserved	32	RO	–	0x795
Reserved	32	RO	–	0x796
Reserved	32	RO	–	0x797
Reserved	32	RO	–	0x798

Table 38. GBIC Block Register Map

Register	Bit Size	Mode[1]	Ref Page	Address
GBIC Status Register Ports 0-9	32	RO	121	0x799
GBIC Control Register Ports 0-9	32	R/W	121	0x79A
I^2C Control and Data Register Ports 0-9	32	R/W	121	0x79B

6.5.1 MAC Control Registers

Table 39 through Table 58 on page 89 provide details on the control and status registers associated with each MAC port. The register address is '**Port_index + 0x****', where the port index is set at any value from 0x0 through 0x5. All registers are 32 bits.

Table 39. Station Address Register Low (Addr: Port_Index + 0x00)

Bit	Name	Description	Type[1]	Default
31:0	StationAddress Low	Source MAC address bits 31-0. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 40. Station Address Register High (Addr: Port_Index + 0x01)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	StationAddress High	Source MAC address bits 47-32. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 41. FDFC Type Register (Addr: Port_Index + 0x03)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFCType	Contains the value of the type field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0x8808
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 42. FC TX Timer Value Register (Addr: Port_Index + 0x07)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FCTxTimer Value	The pause length sent to the receiving station in 512 bit times	R/W	0x005E
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 43. FDFC Address Low Register (Addr: Port_Index + 0x08)

Bit	Name	Description	Type[1]	Default
31:0	FDFC AddressLow	Contains the value of the lowest 32 bits of the destination address field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0xC2000001
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 44. FDFC Address High Register (Addr: Port_Index + 0x09)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFC AddressHigh	Contains the value of the highest 16 bits of the destination address filed transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds it high watermark.	R/W	0x0180
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 45. IPG Receive Time 1 Register (Addr: Port_Index + 0x0A)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPGReceive Time1	First part of the IPG time for non back-to-back transmissions	R/W	0x0008
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 46. IPG Receive Time 2 Register (Addr: Port_Index + 0x0B)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPGReceive Time2	Second part of the IPG time for non back-to-back transmissions	R/W	0x0007
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 47. IPG Transmit Time Register (Addr: Port_Index + 0x0C)

Bit	Name	Description	Type[1]	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPGTransmit Time	IPG time for back-to-back transmissions	R/W	0x0008
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 48. Pause Threshold Register (Addr: Port_Index + 0x0E)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Pause Threshold	When a pause frame is sent, an internal timer checks when a new pause frame must be scheduled for transmission to keep the link partner in pause mode. The pause threshold value is the minimum time to send before the earlier pause frame is aged out.	R/W	0x002F
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 49. Max Frame Size Register (Addr: Port_Index + 0x0F)

Bit	Name	Description	Type[1]	Default
31:14	Reserved	Reserved	RO	0x0000
13:0	MaxFrameSize	The maximum frame size the MAC can receive or transmit without activating any error counters, and without truncation. The maximum frame size is internally adjusted by +4 if VLAN is tagged.	R/W	0x05EE
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 50. FC Enable Register (Addr: Port_Index + 0x12)

Bit	Name	Description	Type[1]	Default
Register Description: Indicates flow control settings of the IXF1110.				
31:2	Reserved	Reserved	RO	0x00000001
1	TXFDFC	1 = Enable TX FD Flow Control 0 = Disables	R/W	1
0	RXFDFC	1 = Enable RX FD Flow Control 0 = Disables	R/W	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 51. Short Runts Threshold Register (Addr: Port_Index + 0x14)

Bit	Name	Description	Type[1]	Default
31:5	Reserved	Reserved	RO	0x0000000
4:0	ShortRunts Threshold	Holds the value in bytes, which applies to the threshold in determining between runts and short.	R/W	01000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 52. Discard Unknown Control Frame Register (Addr: Port_Index + 0x15)

Bit	Name	Description	Type[1]	Default
31:1	Reserved	Reserved	RO	0x00000000
0	DiscardUnknown ControlFrame	0 = Keep unknown control frames 1 = Discard unknown control frames.	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 53. RX Config Word Register (Addr: Port_Index + 0x16)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in the IXF1110 only for auto-negotiation. The contents of this register are the “config_word” received from the link partner, as described in IEEE 802.3z, Subclause 37.3.6.1.3.				0x00000000
31:22	Reserved	Reserved	RO	0
21	An_complete	Auto-negotiation complete. This bit remains cleared from the time auto-negotiation is reset until auto-negotiation reaches the “LINK_OK” state. It remains set until auto-negotiation is disabled or restarted. (This bit is only valid if auto-negotiation is enabled.)	RO	0
20	Rx Sync	0 = Loss of synchronization 1 = Bit synchronization (bit remains Low until register is read)	RR	0
19	RxConfig	0 = Receiving idle/data stream 1 = Receiving /C/ ordered sets	RO	
18	ConfigChanged	0 = RxConfigWord has changed since last read 1 = RxConfigWord has not changed since last read (This bit remains High until register is read)	RR	0
17	InvalidWord	0 = Have not received an invalid symbol 1 = Have received an invalid symbol (This bit remains High until register is read)	RR	0
16	CarrierSense	0 = Device is not receiving idle characters (carrier sense is true). 1 = Device is receiving idle characters (carrier sense is false).	RO	0
15	NextPage	Next Page request	RO	0
14	Reserved	Reserved	RO	0
13:12	RemoteFault[1:0]	Remote fault definitions	RO	00
11:9	Reserved	Reserved	RO	00
8	AsymPause	Asym Pause (ability to send pause frames)	RO	1
7	SymPause	Syn Pause (ability to send and receive pause frames)	RO	1
6	HalfDuplex	Half-duplex	RO	1
5	FullDuplex	Full-duplex	RO	1
4:0	Reserved	Reserved	RO	00000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 54. TX Config Word Register (Addr: Port_Index + 0x17)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in the IXF1110 for auto-negotiation only. The contents of this register are sent as the config_word.				0x000001A0
31:16	Reserved	Reserved	RO	0x0000
15	NextPage	Next Page request	R/W	0
14	Reserved	Reserved	RO	0
13:12[2]	RemoteFault[1:0]	Remote fault definitions	R/W	00
11:9	Reserved	Reserved	RO	000
8	AsymPause	Ability to send pause frames	R/W	1
7	SymPause	Ability to send and receive pause frames	R/W	1
6	HalfDuplex	Half-duplex	R/W	0
5	FullDuplex	Full-duplex	R/W	1
4:0	Reserved	Reserved	RO	00000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. There is no way to automatically update the state of the Remote Fault bits for transmission. The state of these bits must be set by the system controller via the uP interface prior to enabling auto-negotiation.

Table 55. Diverse Config Register (Addr: Port_Index + 0x18)

Bit	Name	Description	Type[1]	Default
Register Description: This register contains various configuration bits for general use				0x0000110D
31:16	Reserved	Reserved	RO	0x0000
15	force_fsm_abort_enable	Force_fsm_abort_enable	R/W	0
14	AlignPhaseOp	Align phase opposite	R/W	0
13	i_los	Invert loss of synchronization	R/W	0
12	rbc_running_125	rbc running 125	R/W	1
11	clk_Switch_defer	Clock switch defer	R/W	0
10	burst_mode_en	Burst mode enable	R/W	0
9	late_col_retransmit	Late collision retransmit	R/W	0
8	Underrun_no_retransmit	Underrun no Retransmit	R/W	1
7	pad_enable	Enable padding of undersized packets	R/W	0
6	crc_add	Enable automatic CRC appending	R/W	0
5	autoneg_enable	Enable auto-negotiation	R/W	0
4	los_invert	Loss of sync invert	R/W	0
3	phy_duplex	PHY duplex	R/W	1
2	force_duplex	Force Duplex	R/W	1
1	send_config	Send Config	R/W	0
0	set_link_up	Set Link-Up	R/W	1

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 56. Packet Filter Control Register (Addr: Port_Index + 0x19)

Bit	Name	Description	Type[1]	Default
Register Description: This register allows for specific packet types to be marked for filtering, and is used in conjunction with the RX FIFO Errored Frames Drop Enable Register				0x00000000
31:6	Reserved	Reserved		0x000000
5	CRCErrorPass[2]	This bit enables a Global filter on frames with a CRC Error. When CRCErrorPASS = 0, all frames with a CRC Error are marked as bad. **Note:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 71 on page 105). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When CRCErrorPASS = 1, frames with a CRC Error are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
4	PauseFramePass[2]	This bit enables a Global filter on Pause frames. When PauseFramePass = 0, all Pause frames are marked as bad. **Note:** When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 71 on page 105). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When PauseFramePass = 1, all Pause frames are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
3	VLANDropEn[2]	This bit enables a Global filter on VLAN frames. When VLANDropEn = 0, all VLAN frames are passed to the SPI4-2 Interface. When VLANDropEn = 1, all VLAN frames are dropped.	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 10000 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.

Table 56. Packet Filter Control Register (Addr: Port_Index + 0x19) (Continued)

Bit	Name	Description	Type[1]	Default
2	B/CastDropEn[2]	This bit enables a Global filter on Broadcast frames. When B/CastDropEn = 0, all broadcast frames are passed to the SPI4-2 Interface. When B/CastDropEn = 1, all broadcast frames are dropped.	R/W	0
1	M/CastMatchEn[2]	This bit enables a filter on multicast frames. If this bit = 0, all multicast frames are good and are passed to the SPI4-2 Interface. If this bit = 1, only multicast frames with a destination address that matches the PortMulticastAddress is forwarded. All other multicast frames are dropped.	R/W	0
0	U/CastMatchEn[2]	This bit enables a filter on unicast frames. If this bit = 0, all unicast frames are good and are passed to the SPI4-2 interface. If this bit = 1, only unicast frames with a destination address that matches the Station Address is forwarded. All other unicast frames are dropped.	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 10000 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.

Table 57. Port Multicast Address Low Register (Addr: Port_Index + 0x1A)

Bit	Name	Description	Type[1]	Default
31:0	Port Multicast Address Low	This address is used to compare against multicast frames at the receiving side if multicast filtering is enabled. This register contains bits 31:0 of the address.	R/W	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 58. Port Multicast Address High Register (Addr: Port_Index + 0x1B)

Bit	Name	Description	Type[1]	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Port Multicast Address High	This address is used to compare against multicast frames at the receiving side if Multicast filtering is enabled. This register contains bits 47:32 of the address.	R/W	0x0000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.2 MAC RX Statistics Register Overview

The MAC RX Statistics Registers contain the MAC receiver statistic counters and are cleared when read. The software polls these registers and accumulates values to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 59 covers the RX statistics for the 10 MAC ports. The address is identical to the port number.

Table 59. RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)

Name	Description	Address	Type[1]	Default
RxOctetsTotalOK	Counts the bytes received in all legal frames, including all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x20	RR	0x00000000
RxOctetsBAD[2]	Counts the bytes received in all bad frames of a size greater than or equal to 64 bytes. A bad frame is defined as a properly framed packet containing a CRC, alignment error, or code violation. The 64-byte value is measured from the destination address, up to and including CRC. The initial preamble and SFD are not included in this value. **Note:** This register does not increment the Bad Octet count on undersized receive packets.	Port_Index + 0x21	RR	0x00000000
RxUCPkts	The total number of unicast packets received (excluding bad packets) **Note:** This count includes non-pause control and VLAN packets, which are also counted in other counters. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x22	RR	0x00000000
RxMCPkts	The total number of multicast packets received (excluding bad packets **Note:** This count includes pause control packets, which are also counted in the PauseMacControl-ReceivedCounter. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x23	RR	0x00000000
RxBCPkts	The total number of Broadcast packets received (excluding bad packets)	Port_Index + 0x24	RR	0x00000000
RxPkts64Octets	The total number of packets received (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x25	RR	0x00000000
RxPkts65to127 Octets	The total number of packets received (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x26	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 85.

Table 59. RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39) (Continued)

Name	Description	Address	Type[1]	Default
RxPkts128to255 Octets	The total number of packets received (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field	Port_Index + 0x27	RR	0x00000000
RxPkts256to511 Octets	The total number of packets received (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x28	RR	0x00000000
RxPkts512to1023 Octets	The total number of packets received (including bad packets) that were [512-1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x29	RR	0x00000000
RxPkts1024to1518 Octets	The total number of packets received (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x2A	RR	0x00000000
RxPkts1519toMax Octets	The total number of packets received (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max, including the tag	Port_Index + 0x2B	RR	0x00000000
FCSErrors	Number of frames received with legal size, but with wrong CRC field (also called FCS field) Note: Legal size is 64 bytes through the value stored in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 85.	Port_Index + 0x2C	RR	0x00000000
Tagged	Number of frames (including bad packets) with VLAN tag (Type field = 0x8100)	Port_Index + 0x2D	RR	0x00000000
RxDataError	Number of frames received with legal length, containing a code violation (signaled with RX_ERR on RGMII) **Note:** The IXF1110 does not support an RGMII interface, thus this counter is not applicable to the IXF1110.	Port_Index + 0x2E	RR	0x00000000
AlignErrors	Frames with a legal frame size, but containing less than 8 additional bits. The CRC of the frame is wrong when the additional bits are stripped. If the CRC is OK, the frame is not counted, but treated as an OK frame.	Port_Index + 0x2F	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 85.

Table 59. RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39) (Continued)

Name	Description	Address	Type[1]	Default
LongErrors[2]	Frames bigger than the maximum allowed, with both OK CRC and the integral number of octets Default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x30	RR	0x00000000
JabberErrors	Frames bigger than the maximum allowed, with either a bad CRC or a non-integral number of octets. The default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x31	RR	0x00000000
PauseMacControl ReceivedCounter	Number of Pause MAC control frames received	Port_Index + 0x32	RR	0x00000000
UnknownMac ControlFrame Counter	Number of MAC control frames received with an op code different from 0001 (Pause)	Port_Index + 0x33	RR	0x00000000
VeryLongErrors[2]	Frames bigger than the larger of 2*MaxFrameSize and 50000 bits	Port_Index + 0x34	RR	0x00000000
RuntErrors	The total number of packets received that are less than 64 octets in length, but longer than or equal to 96 bit times. **Note:** The “ShortRuntsThreshold” Register controls the byte count used to determine the difference between Runts and Shorts, and therefore controls which counter is incremented for a given frame size. This counter is only updated after receipt of two good frames.	Port_Index + 0x35	RR	0x00000000
Short Errors	The total number of packets received that are less than 96 bit times, which corresponds to a 4-byte frame with a well formed preamble and SFD. This counter indicates fragment sizes illegal in all modes, and is only fully updated after reception of a good frame following a fragment.	Port_Index + 0x36	RR	0x00000000
Carrier Extend Error	Gigabit half-duplex event only Note: N/A - half-duplex only	Port_Index + 0x37	RR	0x00000000
SequenceErrors	Records the number of sequencing errors that occur	Port_Index + 0x38	RR	0x00000000
SymbolErrors	Records the number of symbol errors encountered by the PHY	Port_Index + 0x39	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2^14-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2^14-1. MaxFrameSize is determined by the settings in the “Max Frame Size Register (Addr: Port_Index + 0x0F)” on page 85.

6.5.3 TX Statistics Register Overview

The MAC TX Statistics Registers contain all the MAC transmit statistic counters and are cleared when read. The software must poll these registers to accumulate values and ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 60 covers all 10 MAC ports TX statistics; the address is identical to the port number.

Table 60. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
OctetsTransmittedOK	Counts the bytes transmitted in all legal frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. Any initial collided transmission attempts before a successful frame transmission do not add to this counter.	Port_Index + 0x40	RR	0x00000000
OctetsTransmittedBad	Counts the bytes transmitted in all bad frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted Late collision counted: The count is close to the actual number of bytes transmitted before the frame is discarded Excessive collision counted: The count is close to the actual number of bytes transmitted before the frame is discarded TX underrun counted: The count is expected to match the number of bytes actually transmitted before the frame is discarded TX CRC error counted: All bytes not sent with success are counted by this counter Any initial collided transmission attempts before a successful frame transmission do not add to this counter	Port_Index + 0x41	RR	0x00000000
TxUCPkts	The total number of unicast packets transmitted (excluding bad packets)	Port_Index + 0x42	RR	0x00000000
TxMCPkts	The total number of multicast packets transmitted (excluding bad packets) **Note:** This count includes pause control packets which are also counted in the TxPauseFrames Counter. Thus, these types of packets are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x43	RR	0x00000000
TxBCPkts	The total number of broadcast packets transmitted (excluding bad packets)	Port_Index + 0x44	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 60. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
TxPkts64Octets	The total number of packets transmitted (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x45	RR	0x00000000
Txpkts65to127Octets	The total number of packets transmitted (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x46	RR	0x00000000
Txpkts128to255Octets	The total number of packets transmitted (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128 - 255 bytes, including tag field	Port_Index + 0x47	RR	0x00000000
Txpkts256to511Octets	The total number of packets transmitted (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x48	RR	0x00000000
Txpkts512to1023Octets	The total number of packets transmitted (including bad packets) that were [512 - 1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x49	RR	0x00000000
Txpkts1024to1518Octets	The total number of packets transmitted (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x4A	RR	0x00000000
Txpkts1519toMaxOctets	The total number of packets transmitted (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1526-max, including the tag	Port_Index + 0x4B	RR	0x00000000
DeferredTx (C)	Number of times the initial transmission attempt of a frame is postponed due to another frame already being transmitted on the Ethernet network. **Note**: N/A - half-duplex only	Port_Index + 0x4C	RR	0x00000000
TxTotal Collisions	Sum of all collision events **Note**: N/A - half-duplex only	Port_Index + 0x4D	RR	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 60. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
TxSingleCollisions	A count of successfully transmitted frames on a particular interface where the transmission is inhibited by exactly one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the MultipleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4E	RR	0x00000000
TxMultipleCollisions	A count of successfully transmitted frames on a particular interface for which transmission is inhibited by more than one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the SingleCollisionFrames object. **Note**: N/A - half-duplex only	Port_Index + 0x4F	RR	0x00000000
TxLateCollisions	The number of times a collision is detected on a particular interface later than 512 bit-times into the transmission of a packet. Such frame are terminated and discarded. **Note**: N/A - half-duplex only	Port_Index + 0x50	RR	0x00000000
ExcessiveCollisionErrors	A count of frames, which collides 16 times and is then discarded by the MAC. Not effecting xMultipleCollisions Note: N/A - half-duplex only	Port_Index + 0x51	RR	0x00000000
ExcessiveDeferralErrors	Number of times frame transmission is postponed more than 2*MaxFrameSize due to another frame already being transmitted on the Ethernet network. This causes the MAC to discard the frame. **Note**: N/A - half-duplex only	Port_Index + 0x52	RR	0x00000000
TxExcessiveLengthDrop	Frame transmissions aborted by the MAC because the frame is longer than maximum frame size. These frames are truncated by the MAC when the maximum frame size violation is detected by the MAC.	Port_Index + 0x53	RR	0x00000000
TxUnderrun	Internal TX error which causes the MAC to end the transmission before the end of the frame because the MAC did not get the needed data in time for transmission. The frames are lost and a fragment or a CRC error is transmitted.	Port_Index + 0x54	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 60. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type[1]	Default
Tagged	Number of OK frames with VLAN tag. (Type field = 0x8100).	Port_Index + 0x55	RR	0x00000000
CRCError	Number of frames transmitted with a legal size, but with the wrong CRC field (also called FCS field)	Port_Index + 0x56	RR	0x00000000
TxPauseFrames	Number of pause MAC frames transmitted	Port_Index + 0x57	RR	0x00000000
FlowControlCollisionsSend	Collisions generated on purpose on incoming frames, to avoid reception of traffic, while the port is in half-duplex and has flow control enabled, and do not have sufficient memory to receive more frames. Note: Due to the internal counting technique, a last frame might have to be transmitted after last flow control collision send to get the correct statistic. **Note**: N/A - half-duplex only	Port_Index + 0x58	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.4 Global Status and Configuration Register Overview

Table 61 through Table 67 on page 100 provide an overview of the Global Control and Status Registers.

Table 61. Port Enable Register (Addr: 0x500)

Bit	Name	Description	Type[1]	Default
Register Description: A control register for each port in the IXF1110. Port ID = bit position in the register. To make a port active, the bit must be set High (for example, port 4 active implies register value = 0001.0000). Setting the bit to 0 de-asserts the reset. The default state for this register is for all 10 ports to be active.				0x000003FF
31:10	Reserved	Reserved	RO	0x00000
9	Port 9 Enable	Port 9 0 = Disable 1 = Enable	R/W	1
8	Port 8 Enable	Port 8 0 = Disable 1 = Enable	R/W	1
7	Port 7 Enable	Port 7 0 = Disable 1 = Enable	R/W	1
6	Port 6 Enable	Port 6 0 = Disable 1 = Enable	R/W	1
5	Port 5 Enable	Port 5 0 = Disable 1 = Enable	R/W	1
4	Port 4 Enable	Port 4 0 = Disable 1 = Enable	R/W	1
3	Port 3 Enable	Port 3 0 = Disable 1 = Enable	R/W	1
2	Port 2 Enable	Port 2 0 = Disable 1 = Enable	R/W	1
1	Port 1 Enable	Port 1 0 = Disable 1 = Enable	R/W	1
0	Port 0 Enable	Port 0 0 = Disable 1 = Enable	R/W	1

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. If a port is disabled mid-packet on the receive side in SerDes mode, the RX Stats will not update for that packet due to power-down of SerDes when the port is disabled.

Table 62. Link LED Enable Register (Addr: 0x502)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port bit should be set upon detection of link to enable proper operation of the link LEDs.				0x00000000
31:10	Reserved	Reserved	RO	0x00000
9	Link LED Enable Port 9	Port 9 link 0 = No link 1 = Link	R/W	0
8	Link LED Enable Port 8	Port 8 link 0 = No link 1 = Link	R/W	0
7	Link LED Enable Port 7	Port 7 link 0 = No link 1 = Link	R/W	0
6	Link LED Enable Port 6	Port 6 link 0 = No link 1 = Link	R/W	0
5	Link LED Enable Port 5	Port 5 link 0 = No link 1 = Link	R/W	0
4	Link LED Enable Port 4	Port 4 link 0 = No link 1 = Link	R/W	0
3	Link LED Enable Port 3	Port 3 link 0 = No link 1 = Link	R/W	0
2	Link LED Enable Port 2	Port 2 link 0 = No link 1 = Link	R/W	0
1	Link LED Enable Port 1	Port 1 link 0 = No link 1 = Link	R/W	0
0	Link LED Enable Port 0	Port 0 link 0 = No link 1 = Link	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 63. MAC Soft Reset Register (Addr: 0x505)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port software activated reset of the MAC core.				0x00000000
31:10	Reserved	Reserved	RO	0x00000
9	MAC Soft Reset Port 9	Port 9 0 = Disable 1 = Enable	R/W	0
8	MAC Soft Reset Port 8	Port 8 0 = Disable 1 = Enable	R/W	0
7	MAC Soft Reset Port 7	Port 7 0 = Disable 1 = Enable	R/W	0
6	MAC Soft Reset Port 6	Port 6 0 = Disable 1 = Enable	R/W	0
5	MAC Soft Reset Port 5	Port 5 0 = Disable 1 = Enable	R/W	0
4	MAC Soft Reset Port 4	Port 4 0 = Disable 1 = Enable	R/W	0
3	MAC Soft Reset Port 3	Port 3 0 = Disable 1 = Enable	R/W	0
2	MAC Soft Reset Port 2	Port 2 0 = Disable 1 = Enable	R/W	0
1	MAC Soft Reset Port 1	Port 1 0 = Disable 1 = Enable	R/W	0
0	MAC Soft Reset Port 0	Port 0 0 = Disable 1 = Enable	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 64. CPU Interface Register (Addr: 0x508)

Bit	Name	Description	Type[1]	Default
Register Description: CPU interface Endian select. This register allows the user to select the Endian of the CPU interface to allow various different CPUs to be connected to the IXF1110.				0x00000000
31:1	Reserved	Reserved	RO	0x00000000
0	Endian	0 = Little Endian 1 = Big Endian	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 65. LED Control Register (Addr: 0x509)

Bit	Name	Description	Type[1]	Default
Register Description: Globally selects and enables the LED mode				0x00000000
1	LED Enable	0 = Disable LEDs 1 = Enable LEDs	R/W	0
0	LED Control	0 = Enable LED Mode 0 for use with SGS Thomson M5450 LED driver (Default) 1 = LED Mode 1 for use with Standard Octal Shift Register	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 66. LED Flash Rate Register (Addr: 0x50A)

Bit	Name	Description	Type[1]	Default
31:2	Reserved	Reserved	RO	0x00000000
1:0	LED Flash Rate	00 = 100 ms flash rate 01 = 250 ms flash rate 10 = 500 ms flash rate 11 = Reserved	R/W	00
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 67. LED Fault Disable Register (Addr: 0x50B)

Bit	Name	Description	Type[1]	Default
Register Description: Per-port fault disable: Disables the LED flashing for local or remote faults				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	LED Fault Disable Port 9	Port 9 0 = Fault enabled 1 = Fault disabled	R/W	0
8	LED Fault Disable Port 8	Port 8 0 = Fault enabled 1 = Fault disabled	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 67. LED Fault Disable Register (Addr: 0x50B) (Continued)

Bit	Name	Description	Type[1]	Default
7	LED Fault Disable Port 7	Port 7 0 = Fault enabled 1 = Fault disabled	R/W	0
6	LED Fault Disable Port 6	Port 6 0 = Fault enabled 1 = Fault disabled	R/W	0
5	LED Fault Disable Port 5	Port 5 0 = Fault enabled 1 = Fault disabled	R/W	0
4	LED Fault Disable Port 4	Port 4 0 = Fault enabled 1 = Fault disabled	R/W	0
3	LED Fault Disable Port 3	Port 3 0 = Fault enabled 1 = Fault disabled	R/W	0
2	LED Fault Disable Port 2	Port 2 0 = Fault enabled 1 = Fault disabled	R/W	0
1	LED Fault Disable Port 1	Port 1 0 = Fault enabled 1 = Fault disabled	R/W	0
0	LED Fault Disable Port 0	Port 0 0 = Fault enabled 1 = Fault disabled	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.5 Global RX Block Register Overview

Table 68 through Table 72 on page 107 provide an overview of the RX Block Registers, which include the RX FIFO High and Low watermarks.

Table 68. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 0	High watermark for RX FIFO port 0. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x580	R/W	0x00000740
RX FIFO High Watermark Port 1	High watermark for RX FIFO port 1. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x581	R/W	0x00000740
RX FIFO High Watermark Port 2	High watermark for RX FIFO port 2. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x582	R/W	0x00000740
RX FIFO High Watermark Port 3	High watermark for RX FIFO port 3. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x583	R/W	0x00000740
RX FIFO High Watermark Port 4	High watermark for RX FIFO port 4. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x584	R/W	0x00000740
RX FIFO High Watermark Port 5	High watermark for RX FIFO port 5. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x585	R/W	0x00000740
RX FIFO High Watermark Port 6	High watermark for RX FIFO port 6. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x586	R/W	0x00000740

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 68. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589) (Continued)

Name[2]	Description	Address	Type[1]	Default
RX FIFO High Watermark Port 7	High watermark for RX FIFO port 7. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x587	R/W	0x00000740
RX FIFO High Watermark Port 8	High watermark for RX FIFO port 8. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC	0x588	R/W	0x00000740
RX FIFO High Watermark Port 9	High watermark for RX FIFO port 9. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x589	R/W	0x00000740

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 69. RX FIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 0	Low watermark for RX FIFO port 0. The default value is 1840 bytes. When the port is in flow control, and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58A	R/W	0x00000730
RX FIFO Low Watermark Port 1	Low watermark for RX FIFO port 1. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58B	R/W	0x00000730
RX FIFO Low Watermark Port 2	Low watermark for RX FIFO port 2. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58C	R/W	0x00000730
RX FIFO Low Watermark Port 3	Low watermark for RX FIFO port 3. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58D	R/W	0x00000730
RX FIFO Low Watermark Port 4	Low watermark for RX FIFO port 4. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58E	R/W	0x00000730

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 69. RX FIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593) (Continued)

Name[2]	Description	Address	Type[1]	Default
RX FIFO Low Watermark Port 5	Low watermark for RX FIFO port 5. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58F	R/W	0x00000730
RX FIFO Low Watermark Port 6	Low watermark for RX FIFO port 6. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x590	R/W	0x00000730
RX FIFO Low Watermark Port 7	Low watermark for RX FIFO port 7. The default value is 1840 bytes.When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x591	R/W	0x00000730
RX FIFO Low Watermark Port 8	Low watermark for RX FIFO port 8. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x592	R/W	0x00000730
RX FIFO Low Watermark Port 9	Low watermark for RX FIFO port 9. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x593	R/W	0x00000730

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:15 - Reserved and RO.
   Bits 14:0 - Described above.

Table 70. Number of Frames Removed on Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name[2]	Description	Address	Type[1]	Default
Number of Frames Removed on Port 0	If the RX FIFO on port 0 becomes full, the number of frames lost/removed on this port is shown in this register.	0x594	RR	0x00000000
Number of Frames Removed on Port 1	If the RX FIFO on port 1 becomes full, the number of frames lost/removed on this port is shown in this register.	0x595	RR	0x00000000
Number of Frames Removed on Port 2	If the RX FIFO on port 2 becomes full, the number of frames lost/removed on this port is shown in this register.	0x596	RR	0x00000000
Number of Frames Removed on Port 3	If the RX FIFO on port 3 becomes full, the number of frames lost/removed on this port is shown in this register.	0x597	RR	0x00000000
Number of Frames Removed on Port 4	If the RX FIFO on port 4 becomes full, the number of frames lost/removed on this port is shown in this register.	0x598	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and RO.
   Bits 21:0 - Described above.

Table 70. Number of Frames Removed on Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name[2]	Description	Address	Type[1]	Default
Number of Frames Removed on Port 5	If the RX FIFO on port 5 becomes full, the number of frames lost/removed on this port is shown in this register.	0x599	RR	0x00000000
Number of Frames Removed on Port 6	If the RX FIFO on port 6 becomes full, the number of frames lost/removed on this port is shown in this register.	0x59A	RR	0x00000000
Number of Frames Removed on Port 7	If the RX FIFO on port 7 becomes full, the number of frames lost/removed on this port is shown in this register.	0x59B	RR	0x00000000
Number of Frames Removed on Port 8	If the RX FIFO on port 8 becomes full, the number of frames lost/removed on this port is shown in this register.	0x59C	RR	0x00000000
Number of Frames Removed on Port 9	If the RX FIFO on port 9 becomes full, the number of frames lost/removed on this port is shown in this register.	0x59D	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write.
2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:22 - Reserved and RO.
   Bits 21:0 - Described above.

Table 71. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)

Bit	Name	Description	Type[1]	Default
Register Description: This register is used in conjunction with the MAC filter bits to select whether errored or filtered frames are to be dropped.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 9: 0 = Do not drop frames 1 = Drop frames	R/W	0
8	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 8: 0 = Do not drop frames 1 = Drop frames	R/W	0
7	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 7: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 71. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F) (Continued)

Bit	Name	Description	Type[1]	Default
6	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 6: 0 = Do not drop frames 1 = Drop frames	R/W	0
5	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 5: 0 = Do not drop frames 1 = Drop frames	R/W	0
4	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 4: 0 = Do not drop frames 1 = Drop frames	R/W	0
3	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 3: 0 = Do not drop frames 1 = Drop frames	R/W	0
2	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 2: 0 = Do not drop frames 1 = Drop frames	R/W	0
1	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 1: 0 = Do not drop frames 1 = Drop frames	R/W	0
0	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the MAC Filter bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 0: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 72. RX FIFO Overflow Event Register (Addr: 0x5A0)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides a status if a FIFO-full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	RX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	RX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
6	RX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	RX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	RX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	RX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	RX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	RX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	RX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1. R = Read Only Clear on Read; W = Write only; R/W = Read/Write				

6.5.6 TX Block Register Overview

Table 73 through Table 78 on page 116 provide an overview of the TX Block Registers, which include the TX FIFO High and Low watermark.

Table 73. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 0	High watermark for TX FIFO port 0. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x600	R/W	0x00000630
TX FIFO High Watermark Port 1	High watermark for TX FIFO port 1. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x601	R/W	0x00000630
TX FIFO High Watermark Port 2	High watermark for TX FIFO port 2. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x602	R/W	0x00000630
TX FIFO High Watermark Port 3	High watermark for TX FIFO port 3. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x603	R/W	0x00000630
TX FIFO High Watermark Port 4	High watermark for TX FIFO port 4. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x604	R/W	0x00000630
TX FIFO High Watermark Port 5	High watermark for TX FIFO port 5. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x605	R/W	0x00000630
TX FIFO High Watermark Port 6	High watermark for TX FIFO port 6. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x606	R/W	0x00000630

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 73. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609) (Continued)

Name[2]	Description	Address	Type[1]	Default
TX FIFO High Watermark Port 7	High watermark for TX FIFO port 7. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x607	R/W	0x00000630
TX FIFO High Watermark Port 8	High watermark for TX FIFO port 8. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x608	R/W	0x00000630
TX FIFO High Watermark Port 9	High watermark for TX FIFO port 9. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates “SATISFIED.” This implies further up in the system that no more data must be sent to this port.	0x609	R/W	0x00000630

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 74. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 0	Low watermark for TX FIFO port 0. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60A	R/W	0x000001D0
TX FIFO Low Watermark Port 1	Low watermark for TX FIFO port 1. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60B	R/W	0x000001D0
TX FIFO Low Watermark Port 2	Low watermark for TX FIFO port 2. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60C	R/W	0x000001D0
TX FIFO Low Watermark Port 3	Low watermark for TX FIFO port 3. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60D	R/W	0x000001D0

1. R = Read Only Clear on Read; W = Write only; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 74. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613) (Continued)

Name[2]	Description	Address	Type[1]	Default
TX FIFO Low Watermark Port 4	Low watermark for TX FIFO port 4. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60E	R/W	0x000001D0
TX FIFO Low Watermark Port 5	Low watermark for TX FIFO port 5. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60F	R/W	0x000001D0
TX FIFO Low Watermark Port 6	Low watermark for TX FIFO port 6. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x610	R/W	0x000001D0
TX FIFO Low Watermark Port 7	Low watermark for TX FIFO port 7. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x611	R/W	0x000001D0
TX FIFO Low Watermark Port 8	Low watermark for TX FIFO port 8. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x612	R/W	0x000001D0
TX FIFO Low Watermark Port 9	Low watermark for TX FIFO port 9. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates “STARVING”. This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x613	R/W	0x000001D0

1. R = Read Only Clear on Read; W = Write only; R/W = Read/Write
2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.

Table 75. MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D)

Name[2]	Description[3]	Address	Type[1]	Default
MAC Transfer Threshold Port 0	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x614	R/W	0x00000040
MAC Transfer Threshold Port 1	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x615	R/W	0x00000040
MAC Transfer Threshold Port 2	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x616	R/W	0x00000040
MAC Transfer Threshold Port 3	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x617	R/W	0x00000040

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 75. MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name[2]	Description[3]	Address	Type[1]	Default
MAC Transfer Threshold Port 4	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x618	R/W	0x00000040
MAC Transfer Threshold Port 5	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x619	R/W	0x00000040
MAC Transfer Threshold Port 6	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61A	R/W	0x00000040
MAC Transfer Threshold Port 7	Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61B	R/W	0x00000040

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 75. MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name[2]	Description[3]	Address	Type[1]	Default
MAC Transfer Threshold Port 8	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61C	R/W	0x00000040
MAC Transfer Threshold Port 9	Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps. If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed. Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.	0x61D	R/W	0x00000040

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9):
   Bits 31:13 - Reserved and RO.
   Bits 12:0 - Described above.
3. For proper operation of the IXF1110, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.

Table 76. TX FIFO Overflow Event Register (Addr: 0x61E)

Bit	Name	Description	Type[1]	Default
Register Description: This register provides status that a FIFO- full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	TX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	TX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	TX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
6	TX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	TX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	TX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	TX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	TX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	TX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	TX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 77. Info Out-of-Sequence Register (Addr: 0x621)

Bit	Name	Description	Type[1]	Default
Register Description: This register signals when out-of-sequence data is detected in the TX FIFO. Events such as SOP followed by another SOP cause this bit to be set and remain so until read. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	Info Out-of-Sequence Port 9	Port 9 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
8	Info Out-of-Sequence Port 8	Port 8 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
7	Info Out-of-Sequence Port 7	Port 7 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
6	Info Out-of-Sequence Port 6	Port 6 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
5	Info Out-of-Sequence Port 5	Port 5 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
4	Info Out-of-Sequence Port 4	Port 4 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
3	Info Out-of-Sequence Port 3	Port 3 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
2	Info Out-of-Sequence Port 2	Port 2 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1	Info Out-of-Sequence Port 1	Port 1 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
0	Info Out-of-Sequence Port 0	Port 0 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 78. Number of Frames Removed Ports 0-9 (Addr: 0x622 - 0x62B)

Name	Description	Address	Type[1]	Default
Number of Frames Removed on Port 0	When TX FIFO on port 0 becomes full or reset, the number of frames lost/removed on this port is shown in this register.	0x622	RR	0x00000000
Number of Frames Removed on Port 1	In the case of TX FIFO on port 1 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x623	RR	0x00000000
Number of Frames Removed on Port 2	In the case of TX FIFO on port 2 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x624	RR	0x00000000
Number of Frames Removed on Port 3	In the case of TX FIFO on port 3 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x625	RR	0x00000000
Number of Frames Removed on Port 4	In the case of TX FIFO on port 4 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x626	RR	0x00000000
Number of Frames Removed on Port 5	In the case of TX FIFO on port 5 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x627	RR	0x00000000
Number of Frames Removed on Port 6	In the case of TX FIFO on port 6 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x628	RR	0x00000000
Number of Frames Removed on Port 7	In the case of TX FIFO on port 7 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x629	RR	0x00000000
Number of Frames Removed on Port 8	In the case of TX FIFO on port 8 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x62A	RR	0x00000000
Number of Frames Removed on Port 9	In the case of TX FIFO on port 9 becoming full or reset then the number of frames lost/ removed on this port will be shown in this register.	0x62B	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.7 SPI4-2 Block Register Overview

Table 79 through Table 82 on page 118 provide an overview of the SPI4-2 Block Registers.

Table 79. SPI4-2 RX Burst Size Register (Addr: 0x700)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for burst size.				0x00060002
31	no_idles	Additional Idles are inserted between payloads when set. During default operation, only a single control word is used to signal the end of one frame and the start of another. When this bit is set to 1, idles are inserted between the packets and have individual control words for EOP and SOP.	R/W	0x0
30:25	Reserved	Reserved	RO	0x00
24:16	MaxBurst1	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1110, can accept when the FIFO Status channel indicates STARVING	R/W	0x006
15:9	Reserved	Reserved	RO	0x00
8:0	MaxBurst2	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1110, can accept when the FIFO Status channel indicates HUNGRY	R/W	0x002

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 80. SPI4-2 RX Training Register (Addr: 0x701)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 RX interface start-up parameters for training sequences				0x00000000
31:24	Reserved	Reserved	RO	0x00
23:16	REP_T	Number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles	R/W	0x00
15:0	DATA_MAX_T[2]	Maximum interval (in number of cycles) between scheduling of training sequences on receive data path interface An all zero value disables training sequences.	R/W	0x0000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. The value of DATA_MAX_T is the Most Significant 16 bits of a 24-bit counter value. The Least Significant 8 bits are always 0x00. This allows for a much larger DAT_MAX_T time-out period and provides a more than adequate granularity of selection.

Table 81. SPI4-2 RX Calendar Register (Addr: 0x702)

Bit	Name	Description	Type[1]	Default Value
Register Description: SPI4-2 RX interface start-up parameters for FIFO status calendar operation.				0x00010300
31:30	RX Train Test Modes	00 = Normal mode. 01 = Do not enter training based on a repeating “11” pattern on RSTAT[1:0] 1x = Train continuously	R/W	0x0
29	RSCLK_invert	When this bit = 0, the FIFO status is captured on the rising edge of the RSCLK as per the SPI4-2 specification. When this bit = 1, the FIFO status is captured on the falling edge of RSCLK	R/W	0
28	TSCLK_invert	When this bit = 0, the FIFO status is launched on the rising edge of the TSCLK as per the SPI4-2 specification. When this bit = 0, the FIFO status is launched on the falling edge of TSCLK	R/W	0
27:21	Reserved	Reserved	RO	0x000
20	DIP2_Error	Set based on an incorrect RX DIP2 result. This bit is cleared upon a read	RR	0x0
19:16	DIP-2_Thr	Defines how many consecutive correct DIP-2s are required to disable sending of training sequences.	R/W	0x1
15:12	Reserved	Reserved	RO	0x0
11:8	Loss_of_Sync	Number of consecutive calendar framing cycles required to invoke sending of training sequences.	R/W	0x3
7:4	Reserved	Reserved	RO	0x0
3:0	CAL_M	Number of times FIFO status for ports 0 through 9 repeat between framing and DIP-2 cycles	R/W	0x0
1. R0 = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 82. SPI4-2 TX Synchronization Register (Addr: 0x703)

Bit	Name	Description	Type[1]	Default
Register Description: SPI4-2 synchronization DIP-4 counters.				0x00000045
31:8	Reserved	Reserved	RO	0x0000000
7:4	DIP4_UnLock[2]	Number of consecutive incorrect DIP4 results that cause TSTAT[1:0] being driven to “11”	R/W	0x4
3:0	DIP4_Lock	Number of consecutive correct DIP4 results to achieve synchronization and end training	R/W	0x5
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. When Periodic Training is enabled, the actual count of DIP4 errors required to lose synchronization is 1 less than the programmed value in this register. Therefore, this value should always be programmed to be 1 more than the desired value and should never be programmed to either 0 or 1.				

6.5.8 SerDes Register Overview

Table 83 through Table 85 on page 120 define the contents of the SerDes Register Block at base location 0x780 which contain the control and status for the ten SerDes interfaces on the IXF1110.

Table 83. TX and RX AC/DC Coupling Selection Register (Addr: 0x780)

Bit	Name	Description	Type[1]	Default
Register Description: Allows selection of AC or DC coupling on the output of each SerDes port (TX and RX are independent)				0x00000000
31:20	Reserved	Reserved	RO	0x000
19	RxACDC9	Selects line coupling mode, AC = 0, DC = 1	R/W	0
18	TxACDC9	Selects line coupling mode, AC = 0, DC = 1	R/W	0
17	RxACDC8	Selects line coupling mode, AC = 0, DC = 1	R/W	0
16	TxACDC8	Selects line coupling mode, AC = 0, DC = 1	R/W	0
15	RxACDC7	Selects line coupling mode, AC = 0, DC = 1	R/W	0
14	TxACDC7	Selects line coupling mode, AC = 0, DC = 1	R/W	0
13	RxACDC6	Selects line coupling mode, AC = 0, DC = 1	R/W	0
12	TxACDC6	Selects line coupling mode, AC = 0, DC = 1	R/W	0
11	RxACDC5	Selects line coupling mode, AC = 0, DC = 1	R/W	0
10	TxACDC5	Selects line coupling mode, AC = 0, DC = 1	R/W	0
9	RxACDC4	Selects line coupling mode, AC = 0, DC = 1	R/W	0
8	TxACDC4	Selects line coupling mode, AC = 0, DC = 1	R/W	0
7	RxACDC3	Selects line coupling mode, AC = 0, DC = 1	R/W	0
6	TxACDC3	Selects line coupling mode, AC = 0, DC = 1	R/W	0
5	RxACDC2	Selects line coupling mode, AC = 0, DC = 1	R/W	0
4	TxACDC2	Selects line coupling mode, AC = 0, DC = 1	R/W	0
3	RxACDC1	Selects line coupling mode, AC = 0, DC = 1	R/W	0
2	TxACDC1	Selects line coupling mode, AC = 0, DC = 1	R/W	0
1	RxACDC0	Selects line coupling mode, AC = 0, DC = 1	R/W	0
0	TxACDC0	Selects line coupling mode, AC = 0, DC = 1	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 84. Tx and Rx Power-Down Ports 0-9 Register (Addr: 0x787)

Bit	Name	Description	Type[1]	Default
Register Description: Tx and Rx power-down bits to allow per-port power-down of unused ports				0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 84. Tx and Rx Power-Down Ports 0-9 Register (Addr: 0x787)

Bit	Name	Description	Type[1]	Default
31:20	Reserved	Reserved	RO	0x000
19:10	TPWRDWN[9:0]	Tx power-down for Ports 9-0 (1 = Power-down)	R/W	0000000000
9:0	RPWRDWN[9:0]	Rx Power-Down power-down for Ports 9-0 (1 = Power-down)	R/W	0000000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 85. Rx Signal Detect Level Ports 0-9 Register (Addr: 0x793)

Bit	Name	Description	Type[1]	Default
Register Description: This register shows the status of the Rx input in relation to the level of the signal being received from the line, and is mainly used for debug and test purposes.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	RX Signal Detect Port 9	Signal Detect for Port 9 0 = Noise 1 = Signal	RO	0
8	RX Signal Detect Port 8	Signal Detect for Port 8 0 = Noise 1 = Signal	RO	0
7	RX Signal Detect Port 7	Signal Detect for Port 7 0 = Noise 1 = Signal	RO	0
6	RX Signal Detect Port 6	Signal Detect for Port 6 0 = Noise 1 = Signal	RO	0
5	RX Signal Detect Port 5	Signal Detect for Port 5 0 = Noise 1 = Signal	RO	0
4	RX Signal Detect Port 4	Signal Detect for Port 4 0 = Noise 1 = Signal	RO	0
3	RX Signal Detect Port 3	Signal Detect for Port 3 0 = Noise 1 = Signal	RO	0
2	RX Signal Detect Port 2	Signal Detect for Port 2 0 = Noise 1 = Signal	RO	0
1	RX Signal Detect Port 1	Signal Detect for Port 1 0 = Noise 1 = Signal	RO	0
0	RX Signal Detect Port 0	Signal Detect for Port 0 0 = Noise 1 = Signal	RO	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.9 GBIC Block Register Overview

Table 86 through Table 88 on page 121 provide an overview of the GBIC Block Registers. These registers provide a means to control and monitor the interface to the GBIC modules.

Table 86. GBIC Status Register Ports 0-9 (Addr: 0x799)

Bit	Name	Description	Type[1]	Default
31:30	Reserved	Reserved	RO	00
29:20	RX_LOS_9:0	RX_LOS inputs for Ports 0-9	RO	0000000000
19:10	TX_FAULT_9:0	TX_FAULT inputs for Ports 0-9	RO	0000000000
9:0	MOD_DEF_9:0	MOD_DEF inputs for Ports 0-9	RO	0000000000
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 87. GBIC Control Register Ports 0-9 Register (Addr: 0x79A)

Bit	Name	Description	Type[1]	Default
31:13	Reserved	Reserved	RO	0000000000 000000000
12	RX_LOS_En	Enable for RX_LOS_Int operation (Enabled = 1)	R/W	0
11	TX_FAULT_En	Enable for TX_FAULT_Int operation (Enabled = 1)	R/W	0
10	MOD_DEF_En	Enable for MOD_DEF_Int operation (Enabled = 1)	R/W	0
9:0	TX_DISABLE_9:0	TX_DISABLE outputs for Ports 0-9	R/W	0000000000
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 88. I^2C Control and Data Register Ports 9-0 Register (Addr: 0x79B)

Bit	Name	Description	Type[1]	Default
31:27	Reserved	Reserved	RO	00000
26	no_ack-err	This bit is set to 1 when a write and subsequent read from a GBIC has failed. This signal should be used to validate the data being read. Data is only valid if this bit is equal to zero.	RO	0
25	I^2CEnable	Enables device wide I^2C Accesses (Enabled = 1)	R/W	0
24	WriteCommand	This bit is set when a new access is requested. WriteCommand active = 1	R/W	0
23:20	PortAddress Select3:0	Address of the IXF1110 port to be accessed	R/W	0000
19:9	DataAddress Select10:0	Address of the GBIC data to be accessed	R/W	00000000000
8	ReadDataValid	ReadDataValid is set to a 1 when valid data is available in the DataRead7:0 field (Cleared on Read)	RR	0
7:0	DataRead7:0	DataRead from the GBIC modules	RO	00000000
1. RO = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

7.0 Package Overview

CBGA packages are suited for applications requiring high I/O counts and high electrical performance. They are recommended for high-power applications, having high noise immunity requirements.

7.1 Features

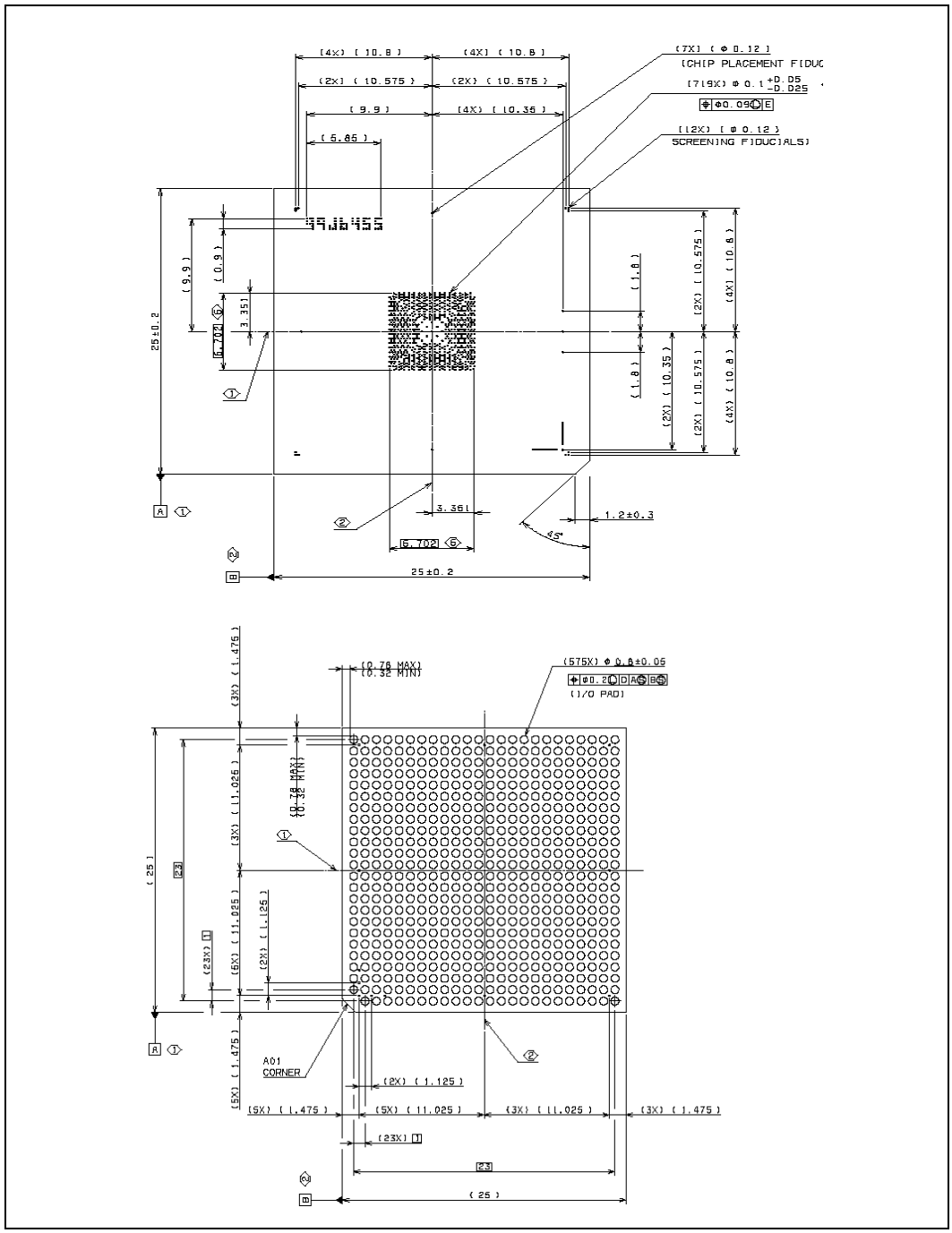
- Flip chip die attach; surface mount second-level interconnect
- High electrical performance
- High I/O counts
- Area array I/O options
- Multiple power zone offering supports core and four additional voltages
- JEDEC-compliant package

7.2 Package Specifics for the IXF1110

The IXF1110 uses the following packaging (see Figure 34, “IXF1110 552-Ceramic Ball Grid Array (CBGA) Package Specification” on page 123):

- 552-ball CBGA
- Ball pitch of 1.0 mm
- Overall package dimensions of 25 mm x 25 mm

Figure 34. IXF1110 552-Ceramic Ball Grid Array (CBGA) Package Specification



8.0 Product Ordering Information

Table 89. Product Information

Number	Revision	Qualification	MM Number	Ship Media
HFIXF1110CC.A1 QE000	A1	Q	848358	Tray

Figure 35. Ordering Information - Sample