

AGR18060E

60 W, 1805 MHz—1880 MHz, LDMOS RF Power Transistor

Introduction

The AGR18060E is a 60 W, 26 V N-channel laterally diffused metal oxide semiconductor (LDMOS) RF power field effect transistor (FET) suitable for enhanced data for global evolution (EDGE), global system for mobile communication (GSM), and single-carrier or multicarrier class AB power amplifier applications. It is packaged in an industry-standard package and is capable of delivering a minimum output power of 60 W, which makes it ideally suited for today's wireless base station RF power amplifier applications.



AGR18060EU (unflanged) AGR18060EF (flanged)

Figure 1. Available Packages

Features

- Typical EDGE performance:
 - 1880 MHz, 26 V, $I_{DQ} = 500$ mA
 - Output power (P_{OUT}): 20 W.
 - Power gain: 15 dB.
 - Efficiency: 34%.
 - Modulation spectrum:
 - @ ± 400 kHz = -62 dBc.
 - @ ± 600 kHz = -73 dBc.
 - Error vector magnitude (EVM) = 2%.
- Typical performance over entire GSM band:
 - P1dB: 60 W typ.
 - Power gain: @ P1dB = 14 dB.
 - Efficiency @ P1dB = 52% typical.
 - Return loss: -10 dB.
- High-reliability, gold-metalization process.
- Low hot carrier injection (HCI) induced bias drift over 20 years.
- Internally matched.
- High gain, efficiency, and linearity.
- Integrated ESD protection.
- Device can withstand 10:1 voltage standing wave ratio (VSWR) at 26 Vdc, 1805 MHz, 60 W continuous wave (CW) output power.
- Large signal impedance parameters available.

Table 1. Thermal Characteristics

| Parameter | Sym | Value | Unit |
|---------------------------------------|-----------------|-------|----------------------|
| Thermal Resistance, Junction to Case: | | | |
| AGR18060EU | $R_{\theta JC}$ | 1.00 | $^{\circ}\text{C/W}$ |
| AGR18060EF | $R_{\theta JC}$ | 1.00 | $^{\circ}\text{C/W}$ |

Table 2. Absolute Maximum Ratings*

| Parameter | Sym | Value | Unit |
|---|-----------|----------|-----------------------------|
| Drain-source Voltage | V_{DSS} | 65 | Vdc |
| Gate-source Voltage | V_{GS} | -0.5, 15 | Vdc |
| Total Dissipation at $T_c = 25^{\circ}\text{C}$: | | | |
| AGR18060EU | P_D | 175 | W |
| AGR18060EF | P_D | 175 | W |
| Derate Above 25°C : | | | |
| AGR18060EU | — | 1.00 | $\text{W}/^{\circ}\text{C}$ |
| AGR18060EF | — | 1.00 | $\text{W}/^{\circ}\text{C}$ |
| Operating Junction Temperature | T_J | 200 | $^{\circ}\text{C}$ |
| Storage Temperature Range | T_{STG} | -65, 150 | $^{\circ}\text{C}$ |

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

| AGR18060E | Minimum (V) | Class |
|-----------|-------------|-------|
| HBM | 500 | 1B |
| MM | 50 | A |
| CDM | 1500 | 4 |

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: $T_c = 30\text{ }^\circ\text{C}$.

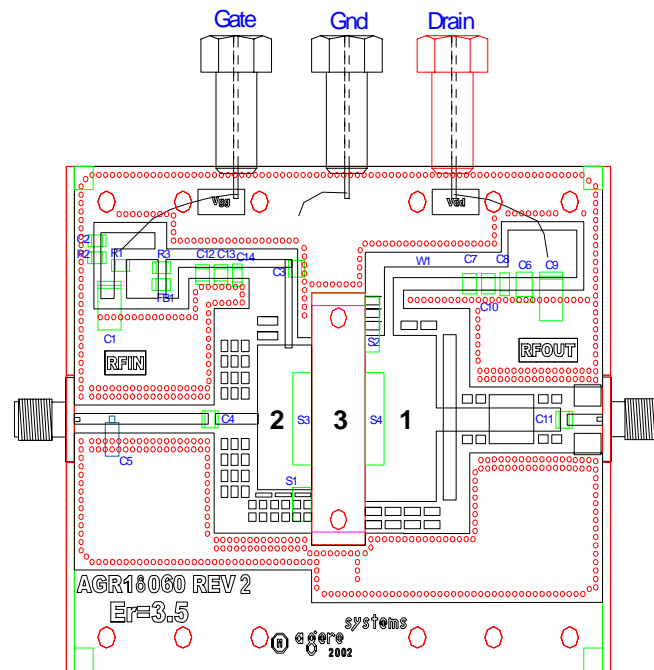
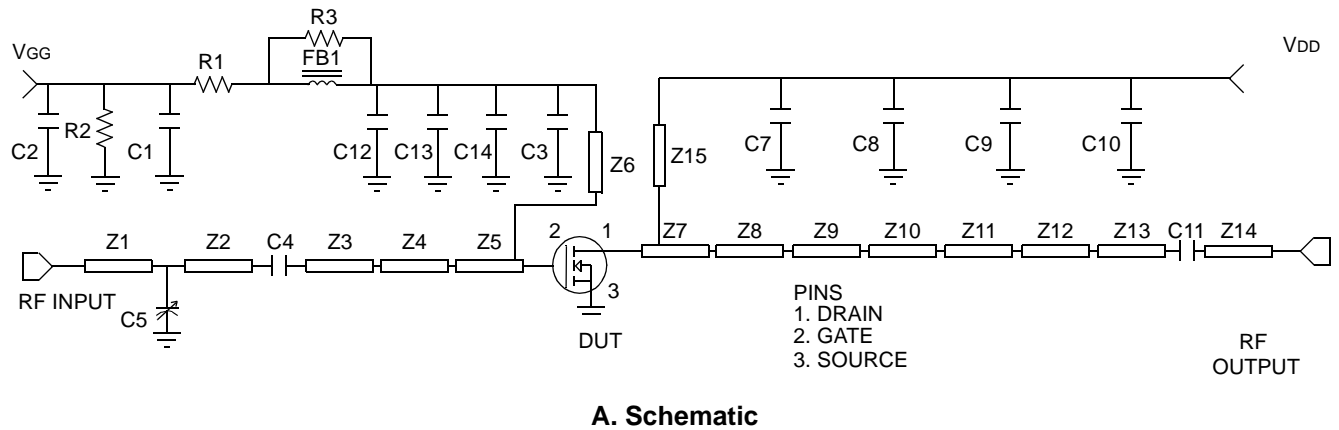
Table 4. dc Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|---------------|-----|------|-----|-----------------|
| Off Characteristics | | | | | |
| Drain-source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 90\text{ }\mu\text{A}$) | $V_{(BR)DSS}$ | 65 | — | — | Vdc |
| Gate-source Leakage Current ($V_{GS} = 5\text{ V}$, $V_{DS} = 0\text{ V}$) | I_{GSS} | — | — | 1.8 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26\text{ V}$, $V_{GS} = 0\text{ V}$) | I_{DSS} | — | — | 5.5 | μAdc |
| On Characteristics | | | | | |
| Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 0.45\text{ A}$) | G_{FS} | — | 4.0 | — | S |
| Gate Threshold Voltage ($V_{DS} = 10\text{ V}$, $I_D = 180\text{ }\mu\text{A}$) | $V_{GS(th)}$ | — | — | 4.8 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 26\text{ V}$, $I_D = 500\text{ mA}$) | $V_{GS(Q)}$ | — | 3.6 | — | Vdc |
| Drain-source On-voltage ($V_{GS} = 10\text{ V}$, $I_D = 0.45\text{ A}$) | $V_{DS(on)}$ | — | 0.08 | — | Vdc |

Table 5. RF Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------|---------------------------------|-----|-----|------|
| Dynamic Characteristics | | | | | |
| Transfer Capacitance ($V_{DS} = 26\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$) (Part is internally matched both on input and output.) | C_{RSS} | — | 1.3 | — | pF |
| Functional Tests (in Agere Systems Supplied Test Fixture) | | | | | |
| Two-Tone Common-source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{OUT} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1805\text{ MHz}$ and 1880 MHz , tone spacing = 100 kHz) | G_{PS} | — | 15 | — | dB |
| Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{OUT} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1805\text{ MHz}$ and 1880 MHz , tone spacing = 100 kHz) | η | — | 41 | — | % |
| Third-order Intermodulation Distortion* ($V_{DD} = 26\text{ Vdc}$, $P_{OUT} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1805\text{ MHz}$ and 1880 MHz , tone spacing = 100 kHz) | $IM3$ | — | -26 | — | dBc |
| Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{OUT} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1805\text{ MHz}$ and 1880 MHz , tone spacing = 100 kHz) | IRL | — | -10 | — | dB |
| Output Power at 1 dB Gain Compression ($V_{DD} = 26\text{ V}$, $P_{OUT} = 60\text{ W CW}$, $f = 1880\text{ MHz}$, $I_{DQ} = 500\text{ mA}$) | $P1dB$ | — | 60 | — | W |
| Ruggedness ($V_{DD} = 26\text{ V}$, $P_{OUT} = 60\text{ W CW}$, $I_{DQ} = 500\text{ mA}$, $f = 1880\text{ MHz}$, $VSWR = 10:1$ [all phase angles]) | Ψ | No degradation in output power. | | | |

Test Circuit Illustrations for AGR18060E

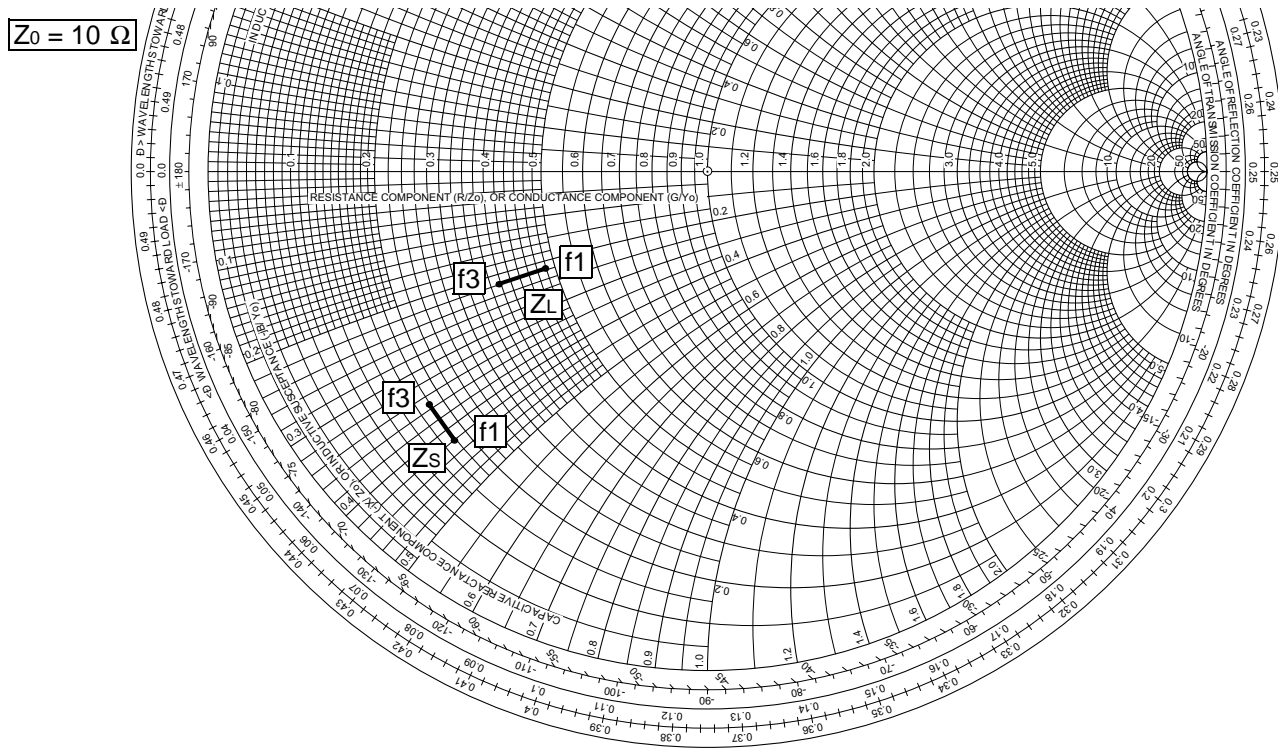


Parts List:

- Microstrip line: Z1 0.065 in. x 0.283 in.; Z2 0.065 in. x 0.700 in.; Z3 0.065 in. x 0.308 in.; Z4 0.856 in. x 0.262 in.; Z5 1.045 in. x 0.140 in.; Z6 0.051 in. x 0.470 in.; Z7 1.220 in. x 0.104 in.; Z8 0.998 in. x 0.422 in.; Z9 0.132 in. x 0.050 in.; Z10 0.984 in. x 0.093 in.; Z11 0.132 in. x 0.244 in.; Z12 0.289 in. x 0.332 in.; Z13 0.132 in. x 0.200 in.; Z14 0.065 in. x 0.250 in.
- ATC® B case chip capacitors: C3, C4: 10 pF, 100B100JCA500X; C11 8.2 pF 100B8R2JCA500X; C7 1000 pF, 100B102JCA500X.
- Kemet® B case chip capacitors: C9, C12: 0.10 μF, CDR33BX104AKWS.
- Johanson Giga-Trim® variable capacitors: C5, C17: 0.4 pF—2.5 pF.
- Vitramon® 1206: C2, C8: 22000 pF.
- Murata® 0805: C13 0.01 μF, GRM40X7R103K100AL.
- 0603: C14 220 pF.
- Fair-Rite® ferrite bead: FB1, #2743019447.
- Sprague® tantalum, SMT: C1, C10: 22 μF, 35 V.
- Fixed film chip resistors: R1 510 Ω, 1/4 W, 0.08 x 0.13; R2 560 kΩ, 1/4 W, 0.08 x 0.13; R3 4.7 Ω, 1/4 W, 0.08 x 0.13.
- PCB etched circuit boards.
- Taconic® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, $\epsilon_r = 3.5$.

Figure 2. AGR18060E Test Circuit Schematic

Typical Performance Characteristics



| MHz (f) | Zs Ω (Complex Source Impedance) | ZL Ω (Complex Optimum Load Impedance) |
|-------------|---|---|
| 1805 (f1) | 1.76 - j4.18 | 4.65 - j2.50 |
| 1842.5 (f2) | 1.78 - j3.78 | 4.23 - j2.44 |
| 1880 (f3) | 1.78 - j3.65 | 3.84 - j2.40 |

Note: ZL was chosen based on trade-offs between gain, output power, drain efficiency, and intermodulation distortion.

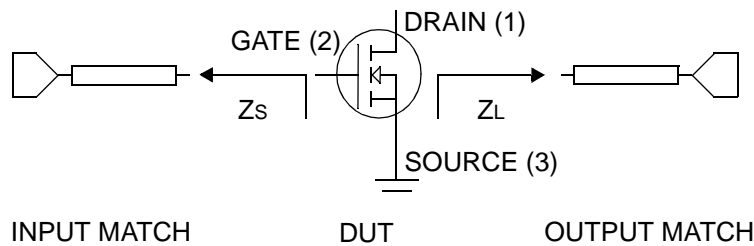
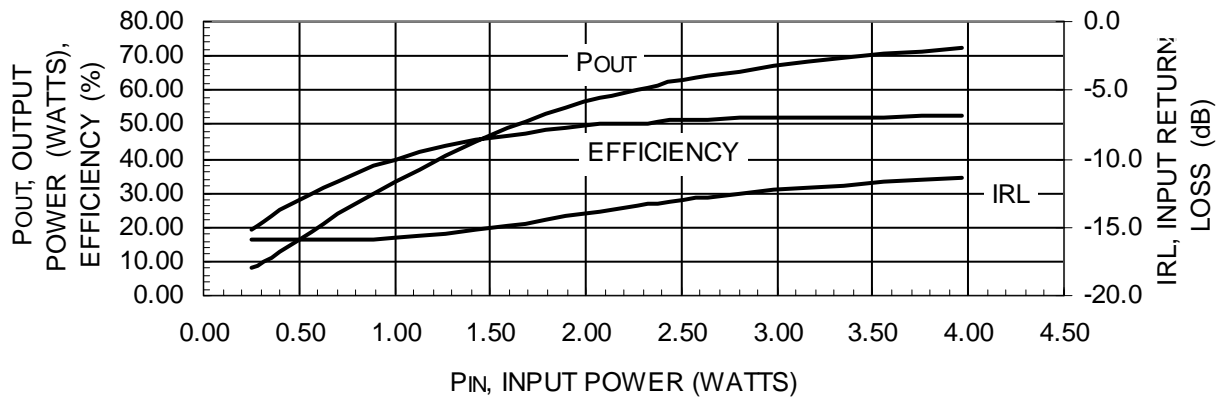


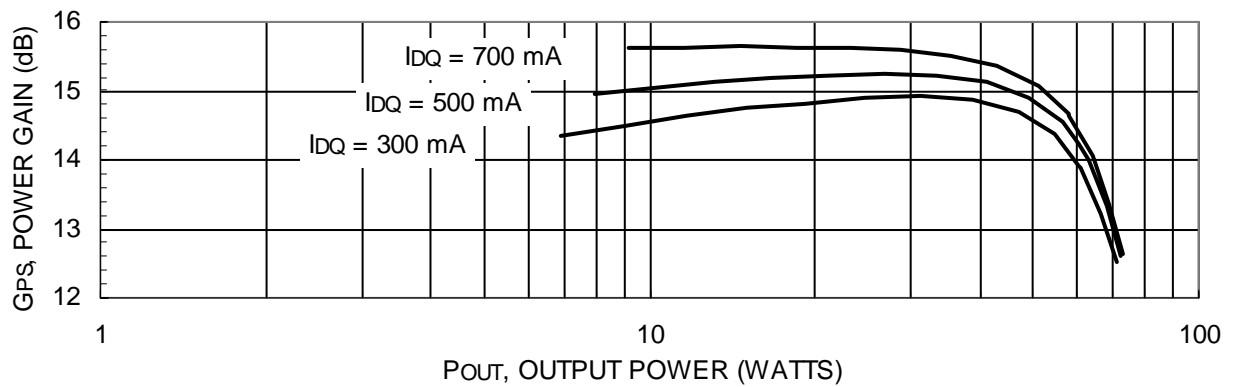
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



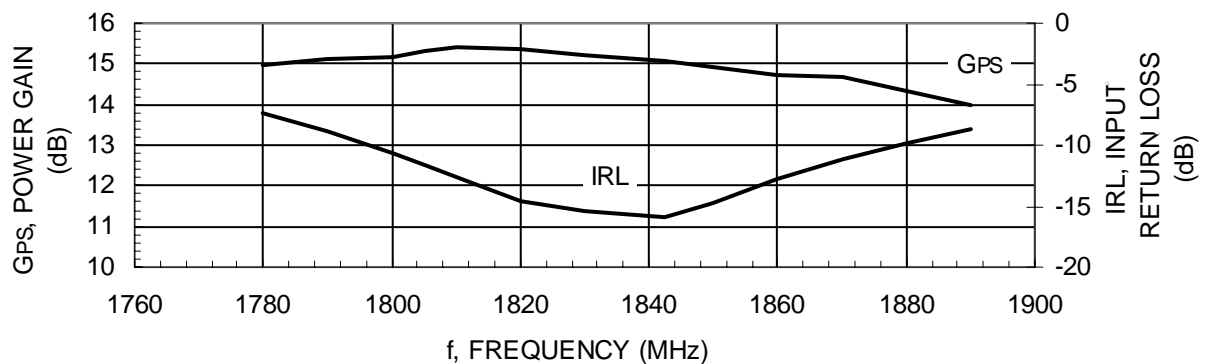
TEST CONDITIONS:
VDD = 26 V, IDQ = 500 mA, FREQUENCY = 1842.5 MHz, CW MEASUREMENT.

Figure 4. Output Power and Efficiency vs. Input Power



TEST CONDITIONS:
VDD = 26 V, FREQUENCY = 1842.5 MHz, CW MEASUREMENT.

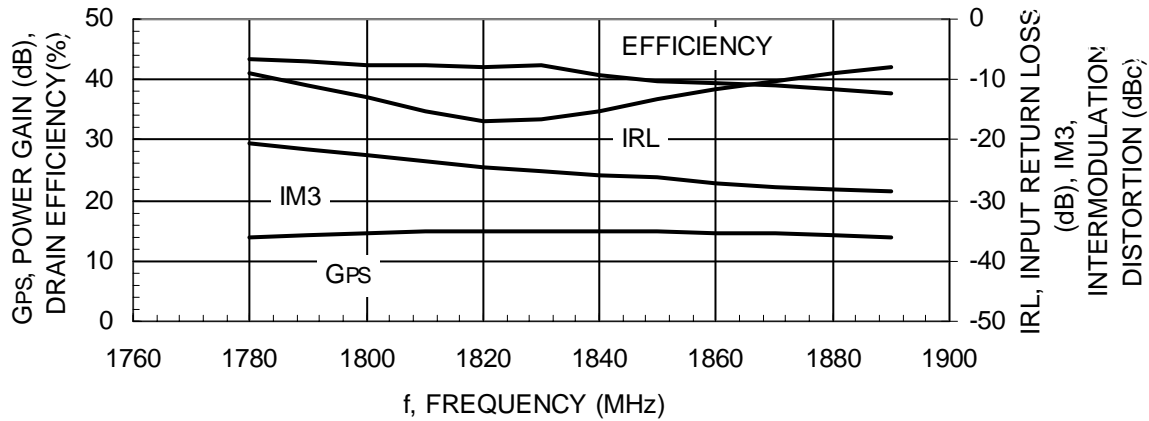
Figure 5. Power Gain vs. Output Power



TEST CONDITIONS:
VDD = 26 V, IDQ = 500 mA, PIN = 25 dBm, CW MEASUREMENT.

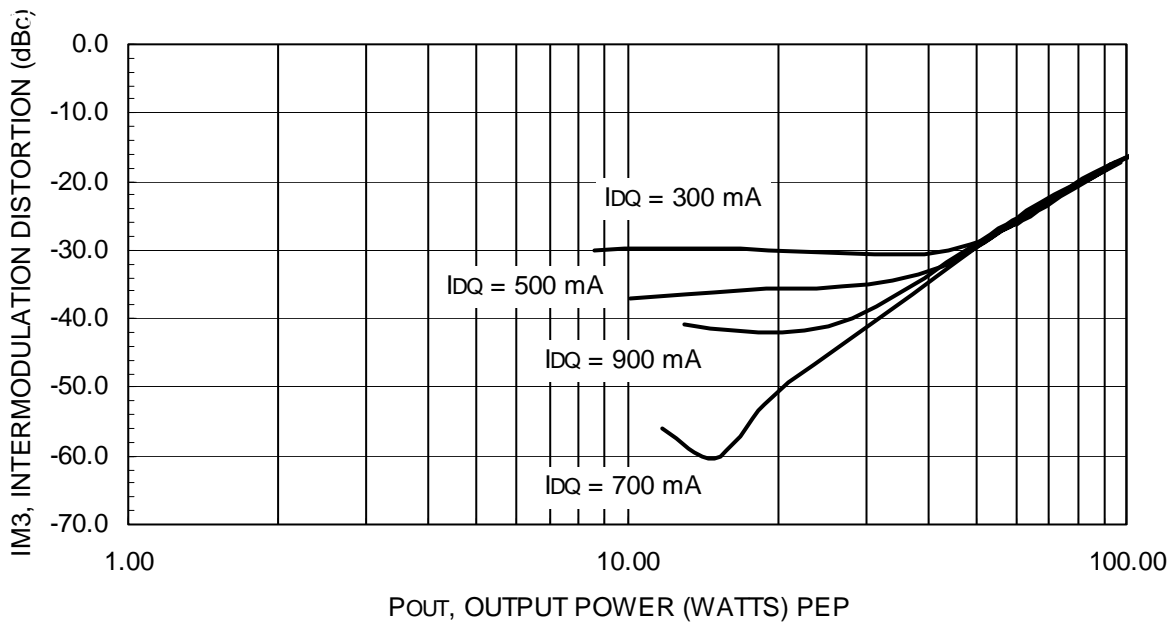
Figure 6. Gain and IRL vs. Signal Frequency

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 500 mA, P_{OUT} = 60 W (PEP), TWO-TONE MEASUREMENT, 100 kHz SPACING.

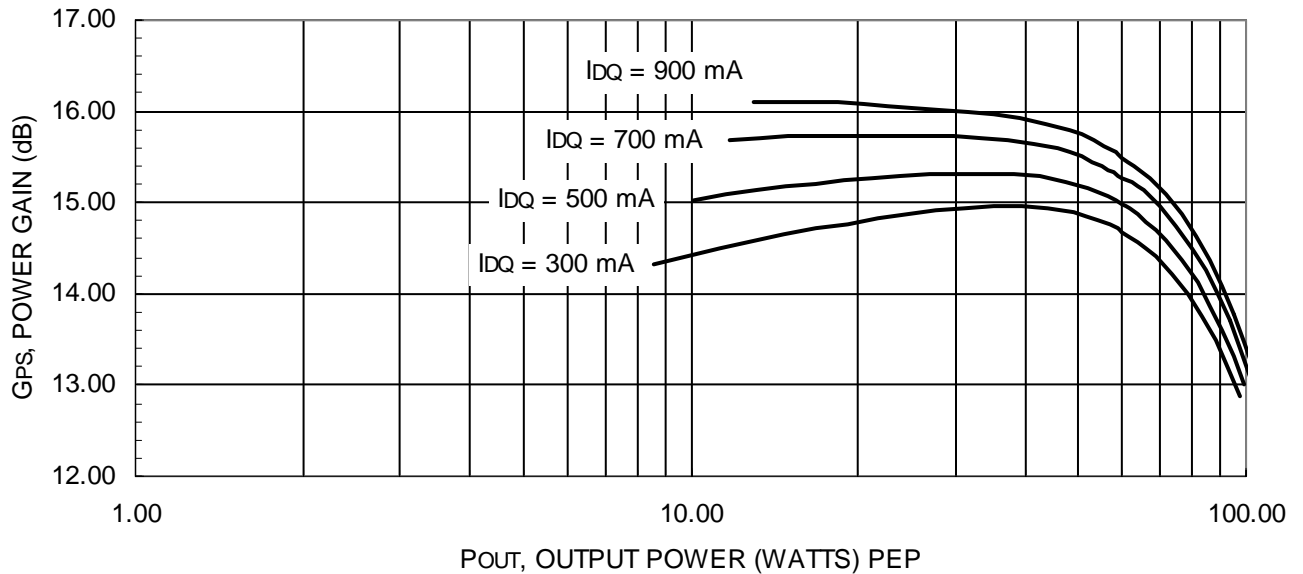
Figure 7. Gain, Efficiency, IRL, vs. Signal Frequency



TEST CONDITIONS:
V_{DD} = 26 V, FREQUENCY = 1842.5 MHz, TWO-TONE MEASUREMENT, 100 kHz SPACING.

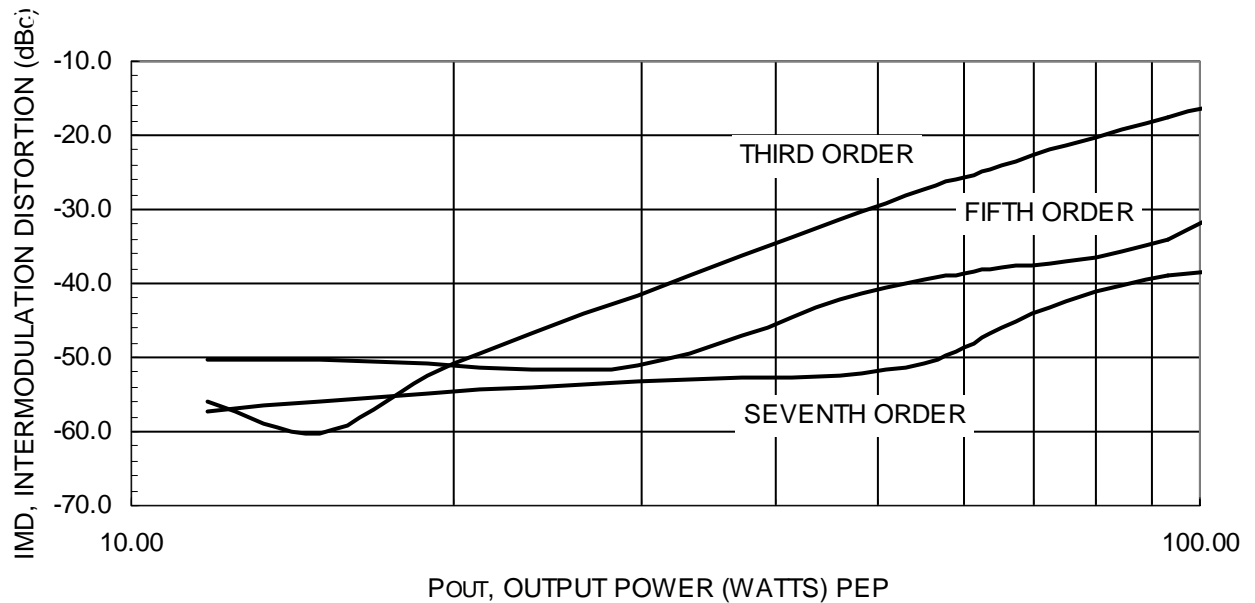
Figure 8. Intermodulation Distortion vs. Output Power

Typical Performance Characteristics (continued)



TEST CONDITIONS:
 V_{DD} = 26 V, FREQUENCY = 1842.5 MHz, TWO-TONE MEASUREMENT, 100 kHz SPACING.

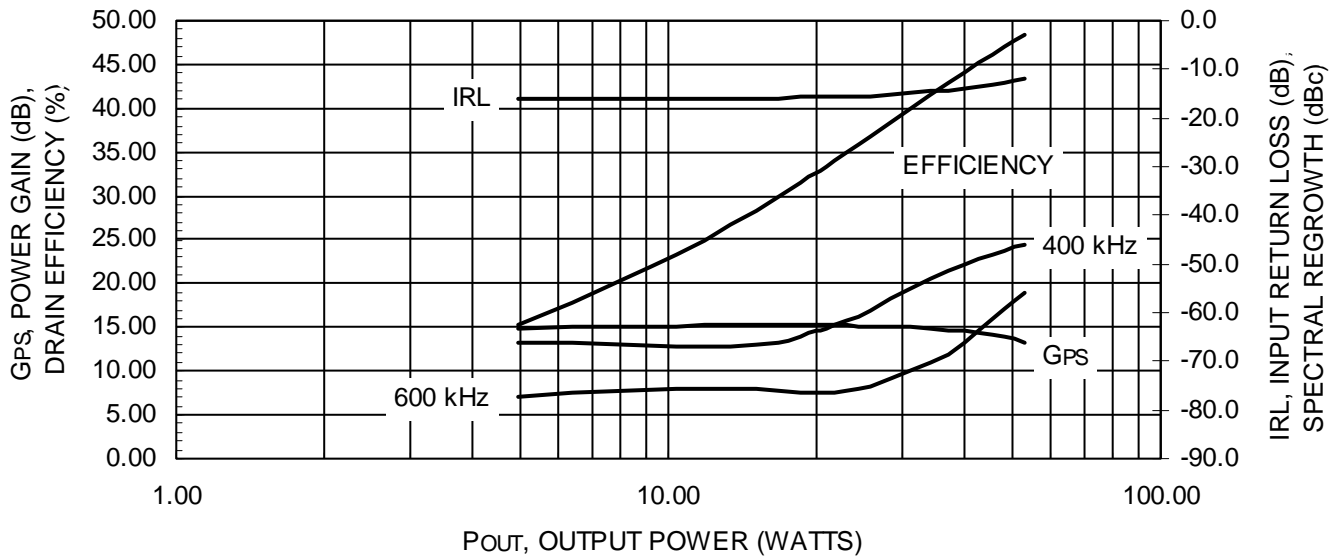
Figure 9. Power Gain vs. Output Power



TEST CONDITIONS:
 V_{DD} = 26 V, FREQUENCY = 1842.5 MHz, I_{DQ} = 700 mA, TWO TONES, 100 kHz SPACING.

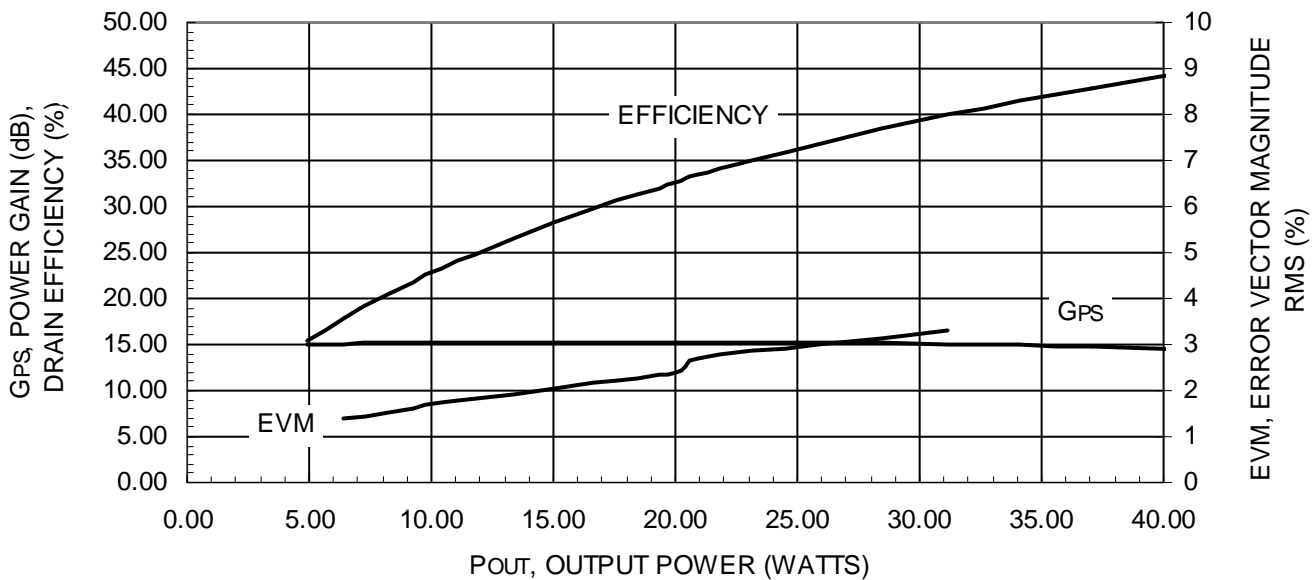
Figure 10. Intermodulation Products vs. Output Power

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 500 mA, FREQUENCY = 1842.5 MHz, EDGE MODULATION.

Figure 11. Power Gain, IRL, IMD, and Efficiency vs. Supply Voltage



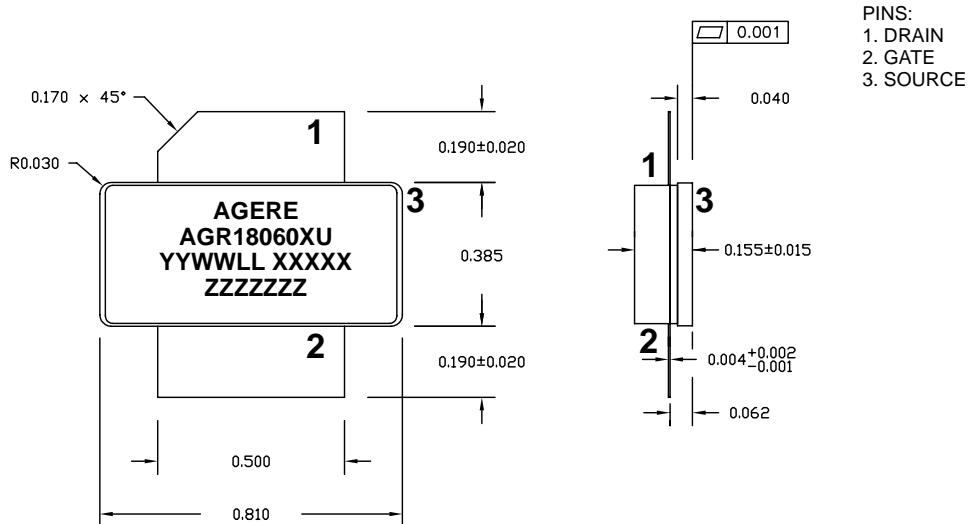
TEST CONDITIONS:
V_{DD} = 26 V, I_{DQ} = 500 mA, FREQUENCY = 1842.5 MHz, EDGE MODULATION.

Figure 12. Gain, Efficiency, IRL, and Spectral Regrowth vs. Output Power

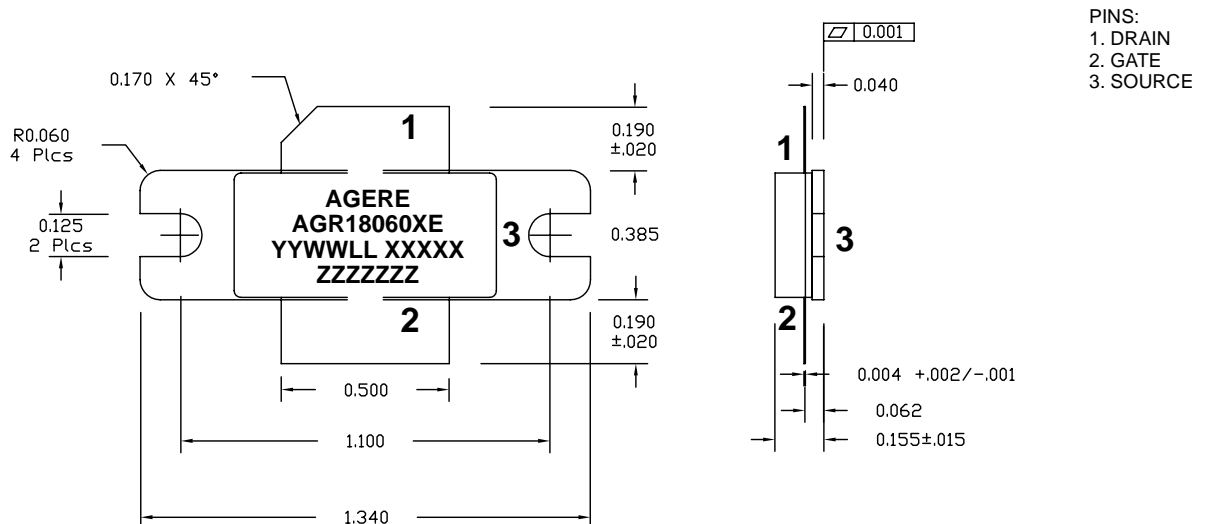
Package Dimensions

All dimensions are in inches. Tolerances are ± 0.005 in. unless specified.

AGR18060EU



AGR18060EF



Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; T = Thailand).
XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.

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