

MOS INTEGRATED CIRCUIT

μ PD42S4805A, 424805A

4 M-BIT DYNAMIC RAM

512 K-WORD BY 8-BIT, HYPER PAGE MODE

Description

The μ PD42S4805A, 424805A are 524 288 words by 8 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of page mode and is useful for the read operation.

The μ PD42S4805A, 424805A are packed in 28-pin plastic TSOP(III) and 28-pin plastic SOJ.

Features

- Hyper page mode
- 524 288 words by 8 bits organization
- Single +5.0 V \pm 10 % power supply

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μ PD42S4805A-50, 424805A-50	50 ns	84 ns	20 ns
μ PD42S4805A-60, 424805A-60	60 ns	104 ns	25 ns
μ PD42S4805A-70, 424805A-70	70 ns	124 ns	30 ns

- μ PD42S4805A can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

Part number	Refresh cycle	Refresh
μ PD42S4805A	1 024 cycles / 128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μ PD424805A	1 024 cycles / 16 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh	
μPD42S4805AG5-60	50 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh	
μPD42S4805AG5-60	60 ns			
μPD42S4805AG5-70	70 ns			
μPD42S4805AG5-50-7KD	50 ns	28-pin Plastic TSOP (II) (400 mil) Reverse bent		
μPD42S4805AG5-60-7KD	60 ns			
μPD42S4805AG5-70-7KD	70 ns			
μPD42S4805ALE-50	50 ns	28-pin Plastic SOJ (400 mil)		
μPD42S4805ALE-60	60 ns			
μPD42S4805ALE-70	70 ns			
μPD424805AG5-50	50 ns	28-pin Plastic TSOP (II) (400 mil)		$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD424805AG5-60	60 ns			
μPD424805AG5-70	70 ns			
μPD424805AG5-50-7KD	50 ns	28-pin Plastic TSOP (II) (400 mil) Reverse bent		
μPD424805AG5-60-7KD	60 ns			
μPD424805AG5-70-7KD	70 ns			
μPD424805ALE-50	50 ns	28-pin Plastic SOJ (400 mil)		
μPD424805ALE-60	60 ns			
μPD424805ALE-70	70 ns			

Quality Grade

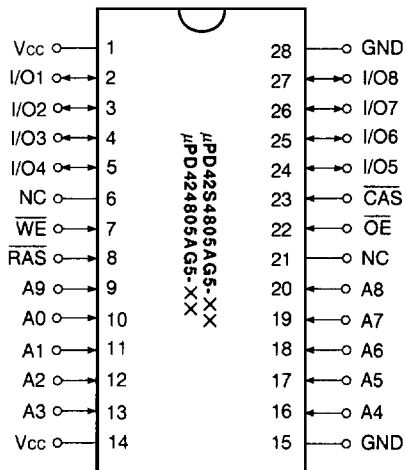
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)

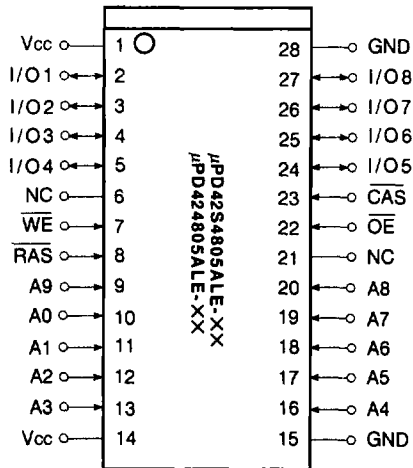
28-pin Plastic TSOP(II)

(400 mil)



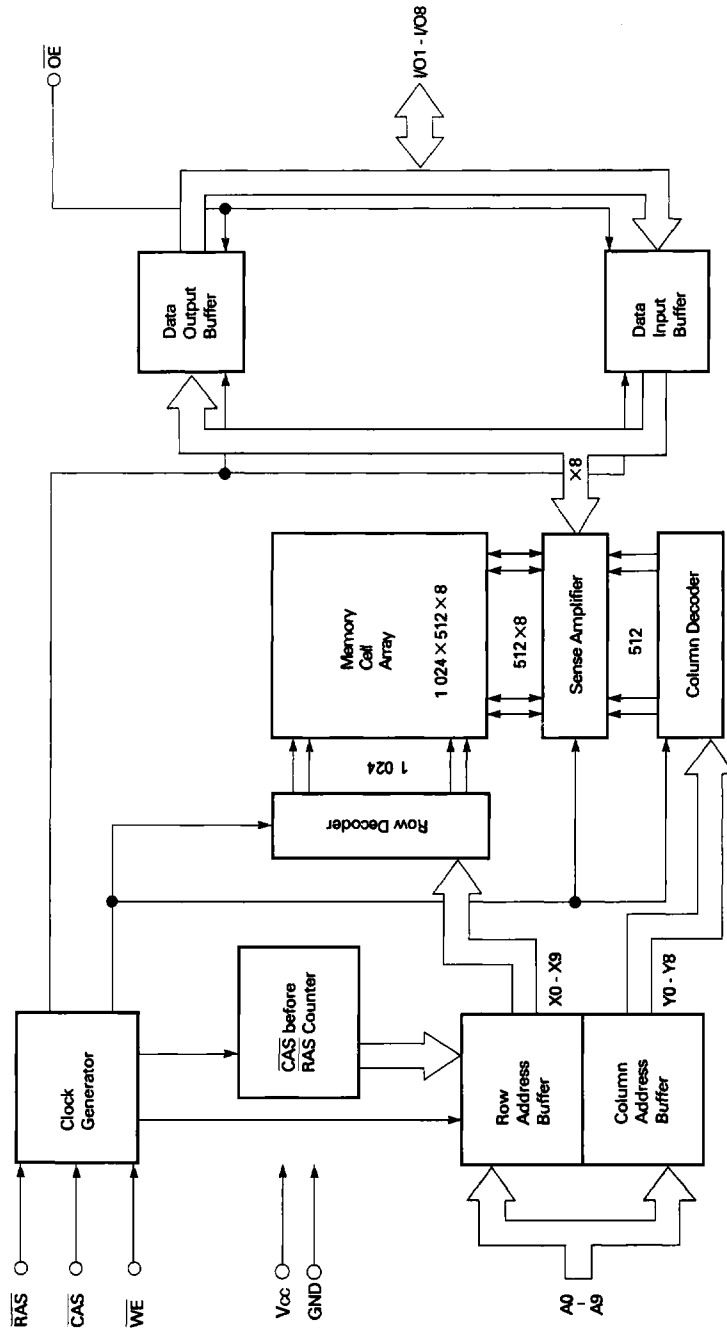
- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

28-pin Plastic SOJ
(400 mil)



- A0 to A9 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S4805A, 424805A have input pins $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 to A9 and input/output pins I/O1 to I/O8.

Pin Name	Input/Output	Function
$\overline{\text{RAS}}$ (Row address strobe)	Input	$\overline{\text{RAS}}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • CAS before RAS refresh
$\overline{\text{CAS}}$ (Column address strobe)		$\overline{\text{CAS}}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)		Address bus. Input total 19-bit of address signal, upper 10-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 524 288-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{\text{RAS}}$. Then, switch the address bus to column address and activate $\overline{\text{CAS}}$. Each address is taken into the device when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
$\overline{\text{WE}}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
$\overline{\text{OE}}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{OE}}$. If $\overline{\text{WE}}$ is activated during read operation, $\overline{\text{OE}}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

In the hyper page mode, the output data is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

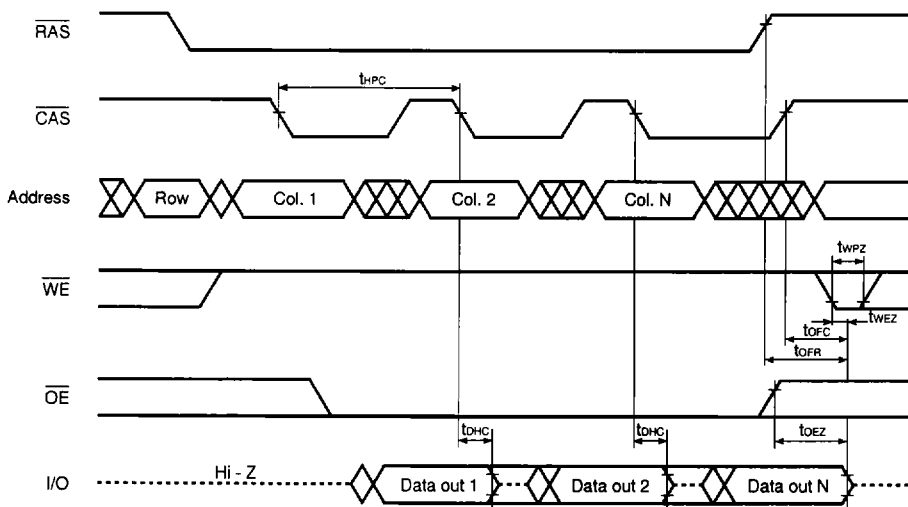
2. The $\overline{\text{CAS}}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

In the hyper page mode, due to the data extend function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{\text{CAS}}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{\text{RAS}}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

Hyper Page Mode Read Cycle



To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on the state of each signal.

(1) $\overline{\text{RAS}}$, $\overline{\text{CAS}}$: inactive (at the end of read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OFR} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

(2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$: active, $\overline{\text{OE}}$: active ... t_{WZ} , t_{WPC} are effective.

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: inactive ... t_{OZ} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		-1.0 to +7.0	V
Supply Voltage	V_{CC}		-1.0 to +7.0	V
Output Current	I_o		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		$V_{CC} + 1.0$	V
Low Level Input Voltage	V_{IL}		-1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance ($T_a = 25\text{ °C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{i1}	Address			5	pF
	C_{i2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$			7	pF
Data Input/Output Capacitance	$C_{i/o}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

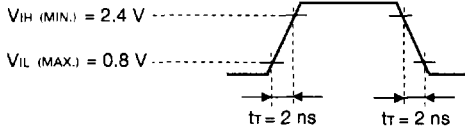
Parameter		Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
Operating current		I _{CC1}	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		80	mA	1, 2, 3
				$t_{RAC} = 60 \text{ ns}$		70		
				$t_{RAC} = 70 \text{ ns}$		60		
Standby current	μPD42S4805A	I _{CC2}	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}, I_o = 0 \text{ mA}$ $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}, I_o = 0 \text{ mA}$ $\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}, I_o = 0 \text{ mA}$ $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}, I_o = 0 \text{ mA}$			2	mA	
						0.15		
	μPD424805A					2		
						1		
RAS only refresh current		I _{CC3}	\overline{RAS} Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}, I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		80	mA	1, 2, 3, 4
				$t_{RAC} = 60 \text{ ns}$		70		
				$t_{RAC} = 70 \text{ ns}$		60		
Operating current (Hyper page mode)		I _{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}, \overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}, I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		80	mA	1, 2, 5
				$t_{RAC} = 60 \text{ ns}$		70		
				$t_{RAC} = 70 \text{ ns}$		60		
CAS before RAS refresh current		I _{CC5}	\overline{RAS} Cycling $t_{RC} = t_{RC(MIN.)}$ $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		80	mA	1, 2
				$t_{RAC} = 60 \text{ ns}$		70		
				$t_{RAC} = 70 \text{ ns}$		60		
CAS before RAS long refresh current (1 024 Cycles / 128 ms, only for the μPD42S4805A)		I _{CC6}	CAS before RAS refresh : 1 024 Cycles / 128 ms $\overline{RAS}, \overline{CAS}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX.)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ Standby : $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{WE}, \overline{OE} : V_{IH}$ $I_o = 0 \text{ mA}$	$t_{RAS} \leq 200 \text{ ns}$		200	μA	1, 2
				$t_{RAS} \leq 1 \mu\text{s}$		300		
Self refresh current (CAS before RAS self refresh, only for the μPD42S4805A)		I _{CC7}	$\overline{RAS}, \overline{CAS}$: $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX.)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			150	μA	2
Input leakage current		I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10		+10	μA	
Output leakage current		I _{O(L)}	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10		+10	μA	
High level output voltage		V _{OH}	$I_o = -5.0 \text{ mA}$	2.4			V	
Low level output voltage		V _{OL}	$I_o = +4.2 \text{ mA}$			0.4	V	

- Notes**
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).
 - Specified values are obtained with outputs unloaded.
 - I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
 - I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 - I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

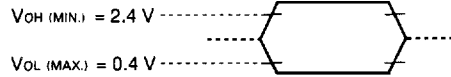
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write Cycle Time	t _{RC}	84	-	104	-	124	-	ns		
RAS Precharge Time	t _{RP}	30	-	40	-	50	-	ns		
CAS Precharge Time	t _{CPN}	7	-	10	-	10	-	ns		
RAS Pulse Width	t _{RAS}	50	10 000	60	10 000	70	10 000	ns		
CAS Pulse Width	t _{CAS}	7	10 000	10	10 000	12	10 000	ns		
RAS Hold Time	t _{RSH}	7	-	10	-	12	-	ns		
CAS Hold Time	t _{CASH}	35	-	40	-	50	-	ns		
RAS to CAS Delay Time	t _{RCD}	11	37	14	45	14	52	ns	1	
RAS to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	1	
CAS to RAS Precharge Time	t _{CRP}	5	-	5	-	5	-	ns	2	
Row Address Setup Time	t _{ASR}	0	-	0	-	0	-	ns		
Row Address Hold Time	t _{RAH}	7	-	10	-	10	-	ns		
Column Address Setup Time	t _{ASC}	0	-	0	-	0	-	ns		
Column Address Hold Time	t _{CAH}	7	-	10	-	12	-	ns		
OE Lead Time Referenced to RAS	t _{OES}	0	-	0	-	0	-	ns		
CAS to Data Setup Time	t _{CLZ}	0	-	0	-	0	-	ns		
OE to Data Setup Time	t _{OLZ}	0	-	0	-	0	-	ns		
OE to Data Delay Time	t _{OED}	10	-	13	-	15	-	ns		
Transition Time (Rise and Fall)	t _T	1	50	1	50	1	50	ns		
Refresh Time	μPD42S4805A	t _{REF}	-	128	-	128	-	128	ms	3
	μPD424805A		-	16	-	16	-	16	ms	

Notes 1. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from RAS
$\overline{\text{trAD}} \leq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\overline{\text{trAC}} (\text{MAX.})$	$\overline{\text{trAC}} (\text{MAX.})$
$\overline{\text{trAD}} > \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\overline{\text{tAA}} (\text{MAX.})$	$\overline{\text{trAD}} + \overline{\text{tAA}} (\text{MAX.})$
$\overline{\text{trCD}} > \overline{\text{trCD}} (\text{MAX.})$	$\overline{\text{tCAC}} (\text{MAX.})$	$\overline{\text{trCD}} + \overline{\text{tCAC}} (\text{MAX.})$

$\overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time($\overline{\text{trAC}}$, $\overline{\text{tAA}}$ or $\overline{\text{tCAC}}$) is to be used for finding out when output data will be available. Therefore, the input conditions $\overline{\text{trAD}} \geq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \geq \overline{\text{trCD}} (\text{MAX.})$ will not cause any operation problems.

2. $\overline{\text{tCRP}} (\text{MIN.})$ requirement is applied to RAS, CAS cycles.
3. This specification is applied only to the μPD42S4805A.

Read Cycle

Parameter	Symbol	trAC = 50 ns		trAC = 60 ns		trAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from RAS	trAC	-	50	-	60	-	70	ns	1
Access Time from CAS	tCAC	-	13	-	15	-	18	ns	1
Access Time from Column Address	tAA	-	25	-	30	-	35	ns	1
Access Time from OE	tOEA	-	13	-	15	-	18	ns	
Column Address Lead Time Referenced to RAS	trAL	25	-	30	-	35	-	ns	
Read Command Setup Time	trCS	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to RAS	trRH	0	-	0	-	0	-	ns	2
Read Command Hold Time Referenced to CAS	trCH	0	-	0	-	0	-	ns	2
Output Buffer Turn-off Delay Time from OE	tOEZ	0	10	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from RAS
$\overline{\text{trAD}} \leq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\overline{\text{trAC}} (\text{MAX.})$	$\overline{\text{trAC}} (\text{MAX.})$
$\overline{\text{trAD}} > \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \leq \overline{\text{trCD}} (\text{MAX.})$	$\overline{\text{tAA}} (\text{MAX.})$	$\overline{\text{trAD}} + \overline{\text{tAA}} (\text{MAX.})$
$\overline{\text{trCD}} > \overline{\text{trCD}} (\text{MAX.})$	$\overline{\text{tCAC}} (\text{MAX.})$	$\overline{\text{trCD}} + \overline{\text{tCAC}} (\text{MAX.})$

$\overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} (\text{MAX.})$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time($\overline{\text{trAC}}$, $\overline{\text{tAA}}$ or $\overline{\text{tCAC}}$) is to be used for finding out when output data will be available. Therefore, the input conditions $\overline{\text{trAD}} \geq \overline{\text{trAD}} (\text{MAX.})$ and $\overline{\text{trCD}} \geq \overline{\text{trCD}} (\text{MAX.})$ will not cause any operation problems.

2. Either $\overline{\text{trCH}} (\text{MIN.})$ or $\overline{\text{trRH}} (\text{MIN.})$ should be met in read cycles.
3. $\overline{\text{tOEZ}} (\text{MAX.})$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$	twch	7	-	10	-	10	-	ns	1
$\overline{\text{WE}}$ Pulse Width	twp	7	-	10	-	10	-	ns	1
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	trwl	7	-	10	-	12	-	ns	
$\overline{\text{WE}}$ Lead Time Referenced to $\overline{\text{CAS}}$	tcwl	7	-	10	-	12	-	ns	
$\overline{\text{WE}}$ Setup Time	twcs	0	-	0	-	0	-	ns	2
$\overline{\text{OE}}$ Hold Time	toeh	0	-	0	-	0	-	ns	
Data-in Setup Time	t _{ds}	0	-	0	-	0	-	ns	3
Data-in Hold Time	t _{dh}	7	-	10	-	10	-	ns	3

- Notes**
1. t_{wp(MIN.)} is applied to late write cycles or read modify write cycles. In early write cycles, t_{wch(MIN.)} should be met.
 2. If t_{wcs} ≥ t_{wcs(MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{ds(MIN.)} and t_{dh(MIN.)} are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{\text{WE}}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	trwc	107	-	133	-	157	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	trwd	64	-	77	-	89	-	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tcwd	27	-	32	-	37	-	ns	1
Column Address to $\overline{\text{WE}}$ Delay Time	tawd	39	-	47	-	54	-	ns	1

- Note**
1. If t_{wcs} ≥ t_{wcs(MIN.)}, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{trwd} ≥ t_{trwd(MIN.)}, t_{tcwd} ≥ t_{tcwd(MIN.)}, t_{tawd} ≥ t_{tawd(MIN.)}, and t_{tcpwd} ≥ t_{tcpwd(MIN.)}, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	20	-	25	-	30	-	ns	
RAS Pulse Width	t _{RASP}	50	125 000	60	125 000	70	125 000	ns	
CAS Pulse Width	t _{HCAS}	7	10 000	10	10 000	12	10 000	ns	
CAS Precharge Time	t _{CP}	7	-	10	-	10	-	ns	
Access Time from CAS Precharge	t _{ACP}	-	27	-	35	-	40	ns	
CAS Precharge to WE Delay Time	t _{CPWD}	41	-	52	-	59	-	ns	1
RAS Hold Time from CAS Precharge	t _{RHCP}	27	-	35	-	40	-	ns	
Read Modify Write Cycle Time	t _{HPRWC}	52	-	66	-	75	-	ns	
Data Output Hold Time	t _{DHC}	5	-	5	-	5	-	ns	
Output Buffer Turn-off Delay from WE	t _{WEZ}	0	10	0	13	0	15	ns	2,3
WE Pulse Width	t _{WPZ}	7	-	10	-	10	-	ns	3
Output Buffer Turn-off Delay from RAS	t _{OFR}	0	10	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from CAS	t _{OFZ}	0	10	0	13	0	15	ns	2,3

Notes 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWd} \geq t_{RWd(MIN.)}$, $t_{CWd} \geq t_{CWd(MIN.)}$, $t_{AWd} \geq t_{AWd(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

3. To make I/Os to Hi-Z in read cycle, it is necessary to control RAS, CAS, WE, OE as follows. The effective specification depends on state of each signal.

(1) RAS, CAS : inactive (at the end of read cycle)

WE : inactive, OE : active

t_{OFZ} is effective when RAS is inactivated before CAS is inactivated.

t_{OFR} is effective when CAS is inactivated before RAS is inactivated.

(2) Both RAS and CAS are active or either RAS or CAS is active (in read cycle)

WE : active, OE : active ... t_{WEZ}, t_{WPZ} are effective.

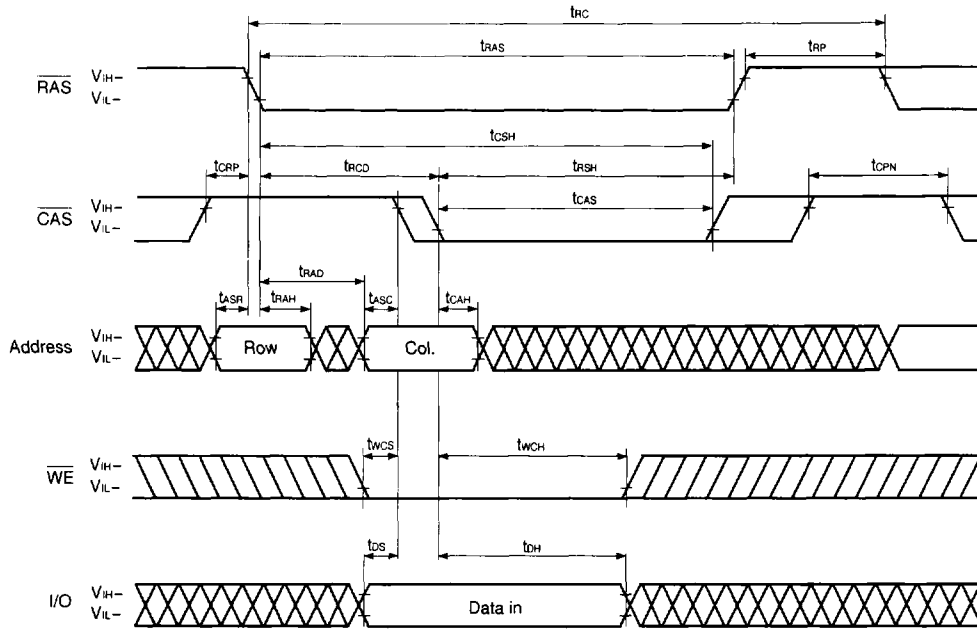
WE : inactive, OE : inactive ... t_{OEZ} is effective.

Refresh Cycle

Parameter	Symbol	t _{RAC} = 50 ns		t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	5	-	5	-	5	-	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	-	10	-	10	-	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	-	5	-	5	-	ns	
RAS Pulse Width (CAS before RAS Self Refresh)	t _{RASS}	100	-	100	-	100	-	μs	1
RAS Precharge Time (CAS before RAS Self Refresh)	t _{RPS}	90	-	110	-	130	-	ns	1
CAS Hold Time (CAS before RAS Self Refresh)	t _{CHS}	-50	-	-50	-	-50	-	ns	1
WE Hold Time (Hidden Refresh Cycle)	t _{WHR}	15	-	15	-	15	-	ns	

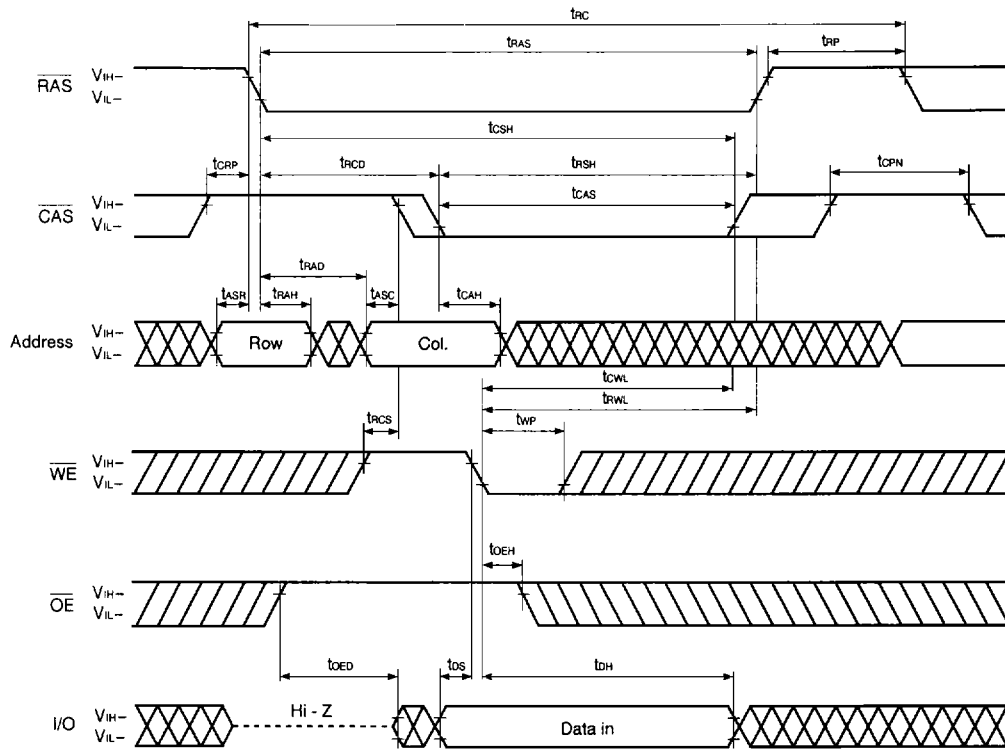
Note 1. This specification is applied only to the μPD42S4805A.

Early Write Cycle

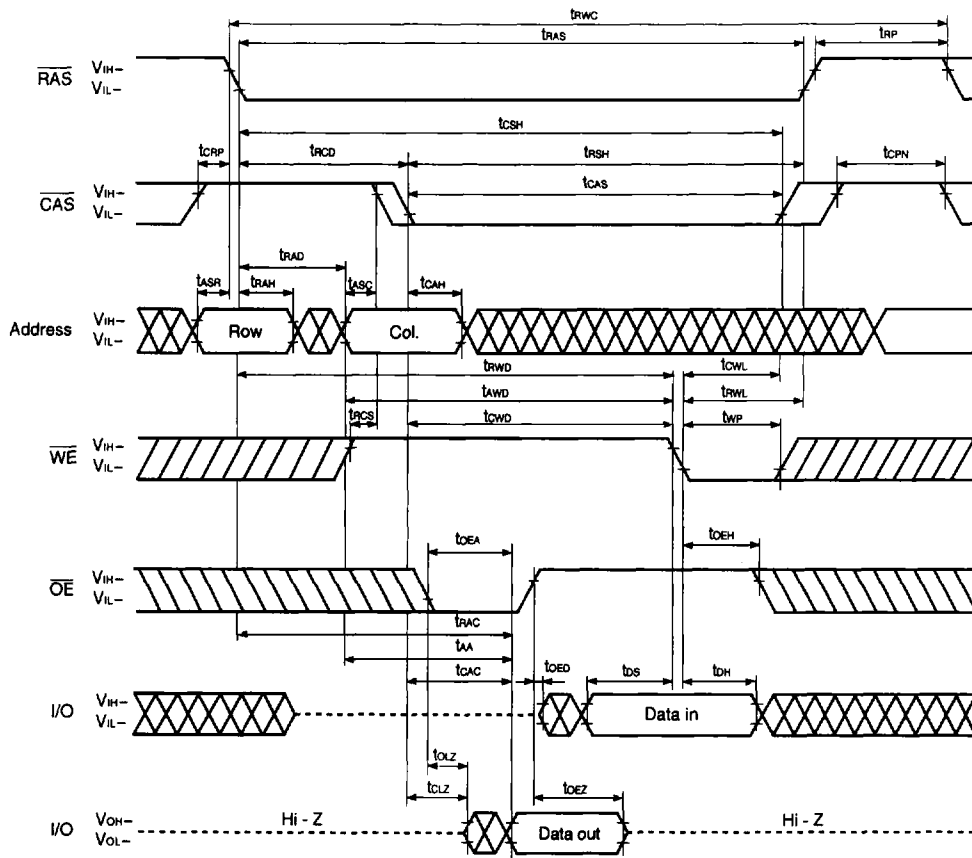


Remark \overline{OE} : Don't care

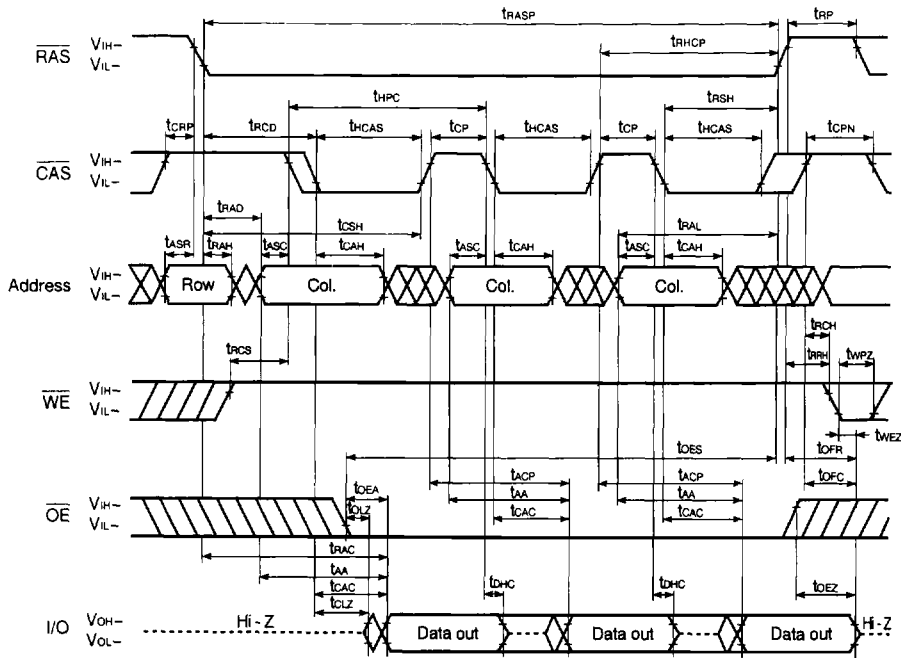
Late Write Cycle



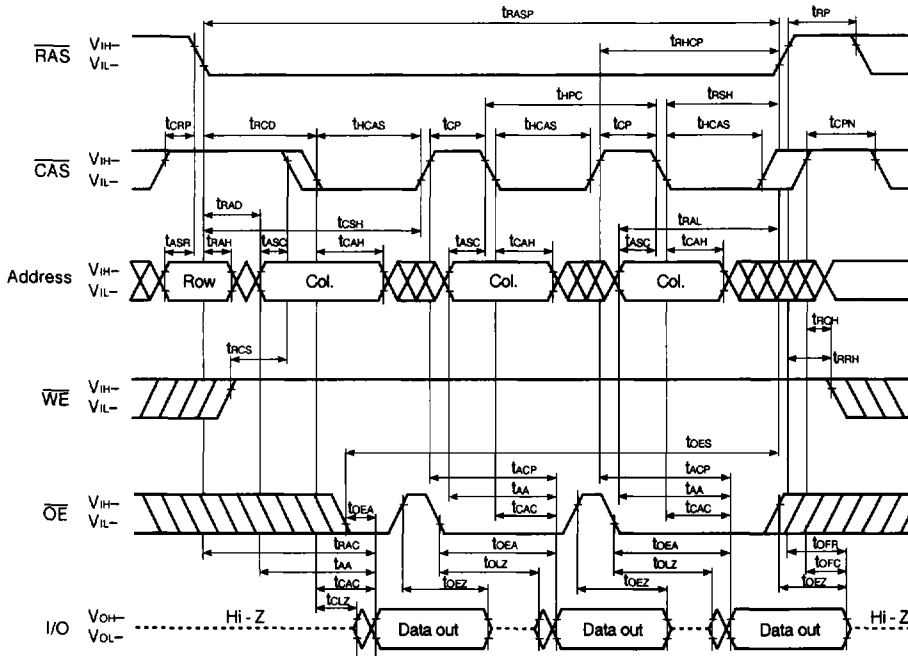
Read Modify Write Cycle



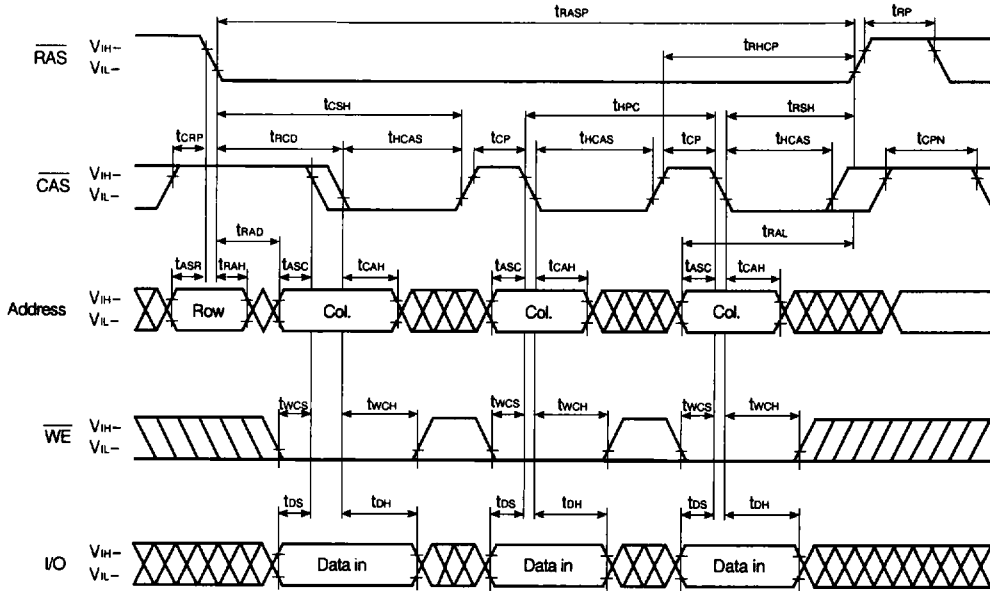
Hyper Page Mode Read Cycle



Hyper Page Mode Read Cycle (OE Control)

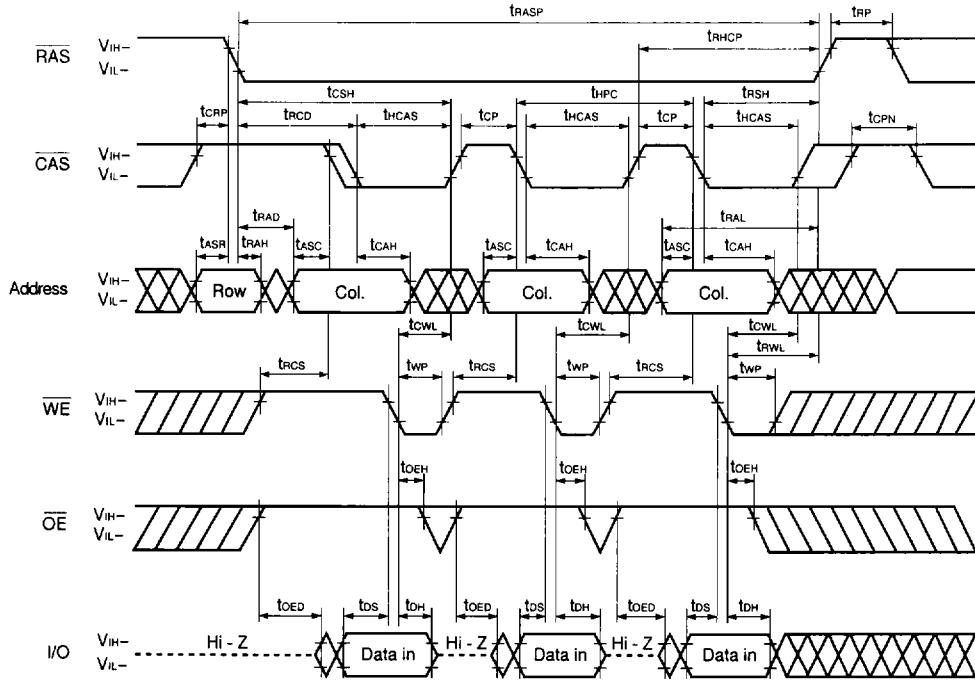


Hyper Page Mode Early Write Cycle

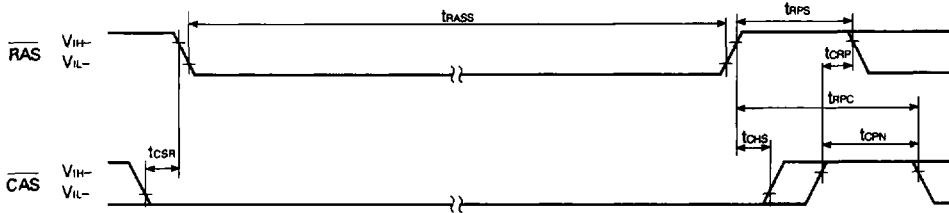


Remark \overline{OE} : Don't care

Hyper Page Mode Late Write Cycle



CAS Before RAS Self Refresh Cycle (Only for the μ PD42S4805A)



Remark Address, \overline{WE} , \overline{OE} : Don't care I/O : Hi - Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh ; However, when used in combination with burst CAS before RAS long refresh or with burst long RAS only refresh, the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

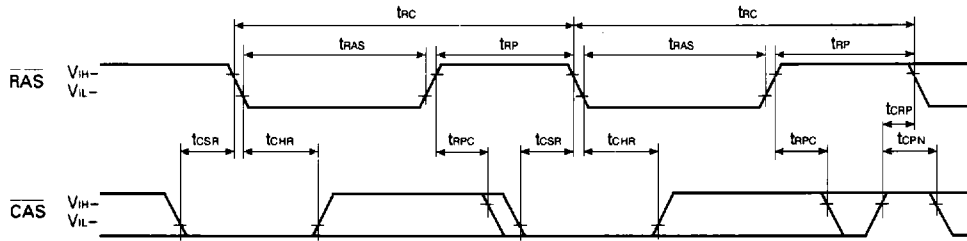
When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh 1 024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

(2) Normal Combined Use of CAS Before RAS Self Refresh and Burst Long RAS Only Refresh

When CAS before RAS self refresh and burst RAS only refresh are used in combination, please perform RAS only refresh 1 024 times within a 16 ms interval just before and after setting CAS before RAS self refresh.

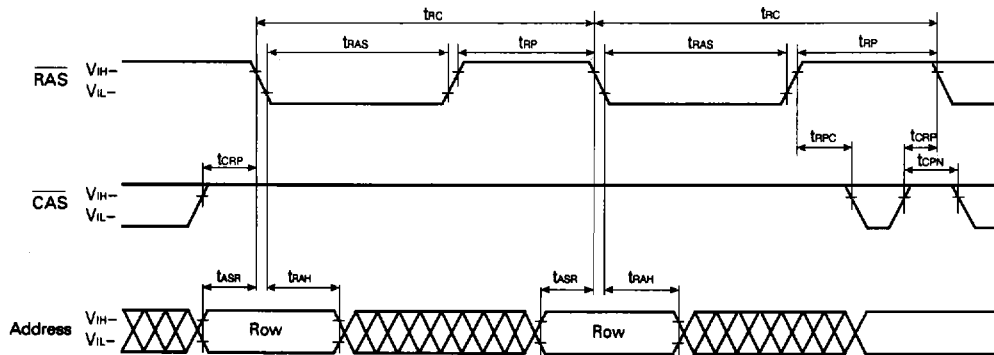
For details, please refer to **How to use DRAM User's Manual**.

CAS Before RAS Refresh Cycle



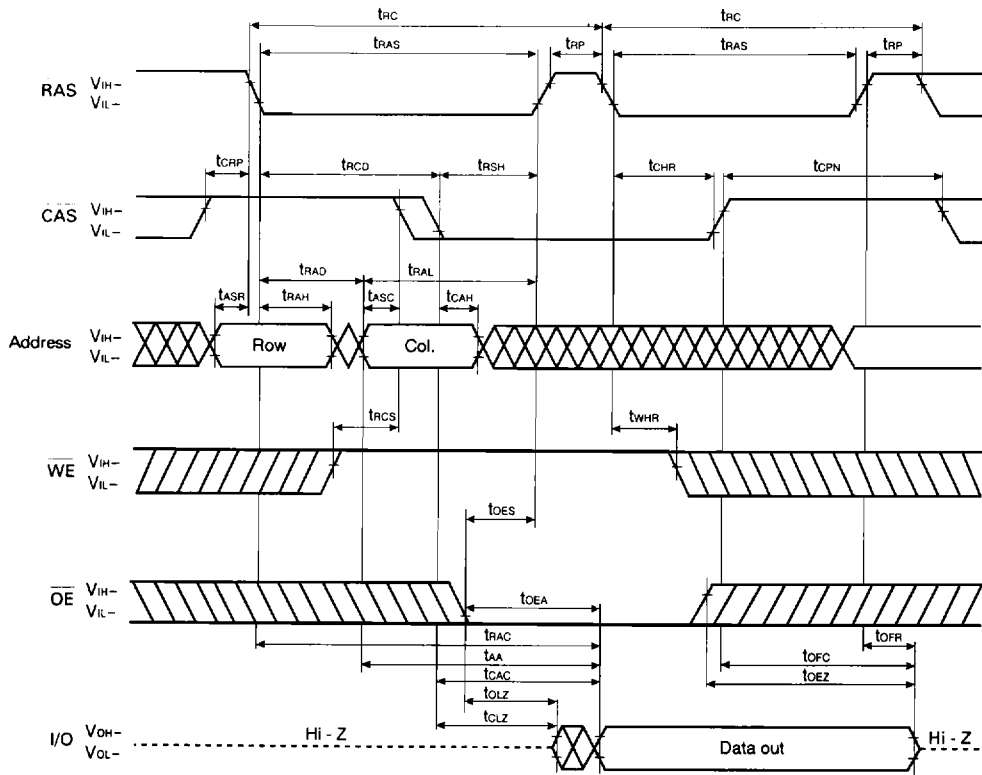
Remark Address, \overline{WE} , \overline{OE} : Don't care I/O : Hi-Z

RAS Only Refresh Cycle



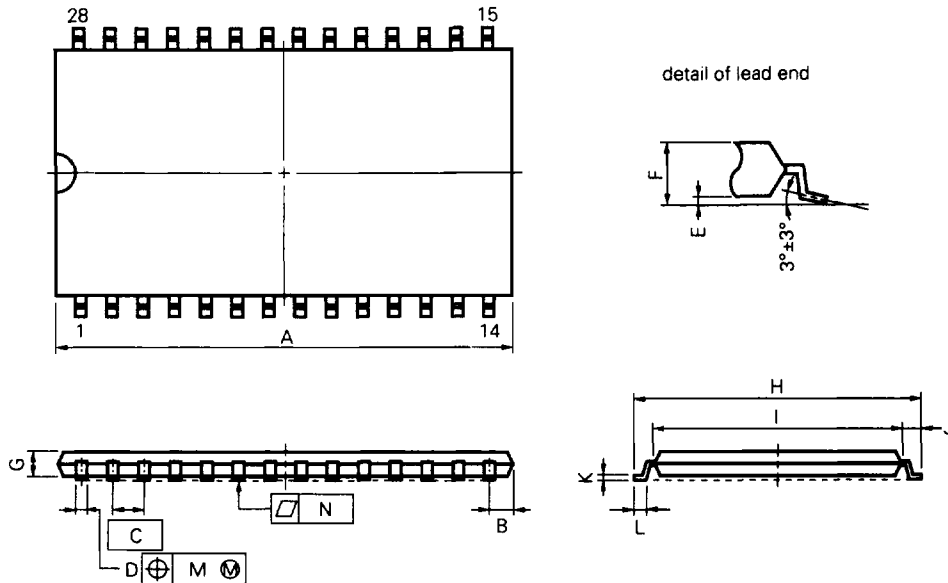
Remark \overline{WE} , \overline{OE} : Don't care I/O : Hi-Z

Hidden Refresh Cycle (Read)



Package Drawings

28 PIN PLASTIC TSOP(III) (400 mil)



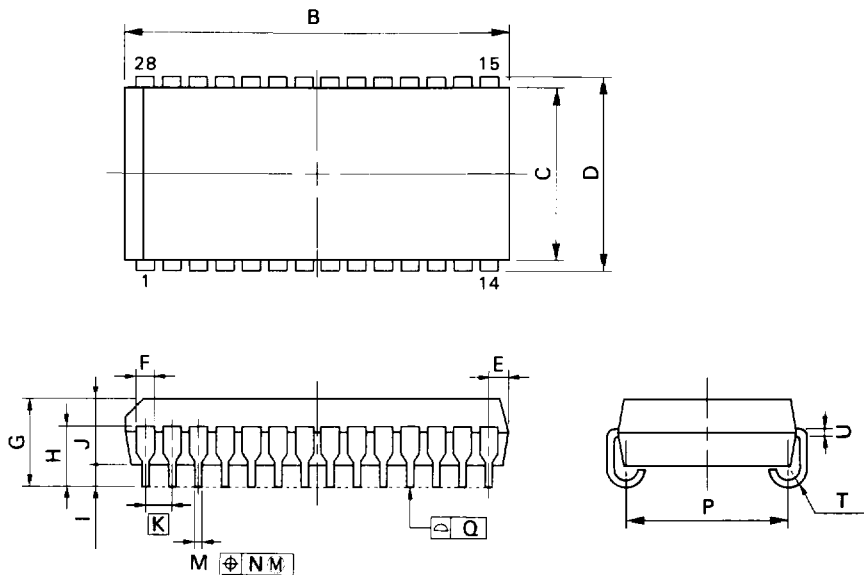
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD-2

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40±0.10	0.016 ^{+0.004} _{-0.005}
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.21	0.009
N	0.10	0.004

28PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LA-400A-1

ITEM	MILLIMETERS	INCHES
B	18.67 ^{+0.35}	0.735 ^{+0.008}
C	10.16	0.400
D	11.18 ^{+0.2}	0.440 ^{+0.008}
E	1.08 ^{+0.15}	0.043 ^{+0.008}
F	0.6	0.024
G	3.5 ^{+0.2}	0.138 ^{+0.008}
H	2.4 ^{+0.2}	0.094 ^{+0.008}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40 ^{+0.10}	0.016 ^{+0.008}
N	0.12	0.005
P	9.40 ^{+0.20}	0.370 ^{+0.008}
Q	0.15	0.006
T	R0.85	R0.033
U	0.20 ^{+0.08}	0.008 ^{+0.008}

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S4805A, 424805A.

Types of Surface Mount Device

μPD42S4805AG5-XX, 424805AG5-XX : 28-pin Plastic TSOP (II) (400 mil)

μPD42S4805ALE-XX, 424805ALE-XX : 28-pin Plastic SOJ (400 mil)