MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX109

Low Voltage, Full Duplex CVSD CODEC with Serial Control

Document #2048-0121.004 February 1995

Preliminary Information

Features

- Single Chip Full Duplex CVSD CODEC
- On-chip Input & Output Filters
- On-chip Volume Control
- Wide Frequency Reference using Ceramic Oscillator
- Low Power, Single Supply Analog CMOS

Applications

- Digital Cordless Phones
- Digital PCN/PCS Systems
- Digital Delay Lines
- Digital Voice Storage
- Multiplexers, Switches & Phones
- Time Domain Scramblers
- Rechargeable Cell Operation

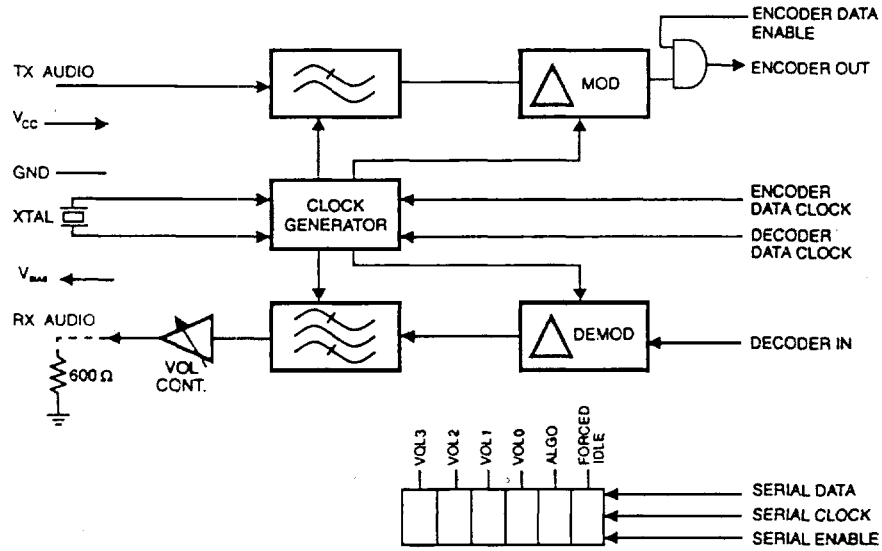
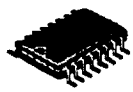
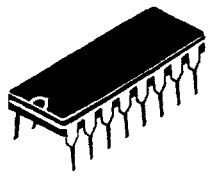


Figure 1 - Internal Block Diagram

AVAILABLE PACKAGES



MX109DW
16 pin SOIC



MX109J (CDIP)
MX109P (PDIP)
16 pins

Description

The MX109 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones. Encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be externally injected in the 8–64k bits/second range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal or ceramic resonator.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

The MX109 is a low-power CMOS device. It is available in PDIP, CDIP and SOIC packages.

PIN FUNCTION CHART

Pin	Function
1	**Xtal/Clock (I/P):** Input to the clock oscillator inverter. A 3.58 MHz Xtal input or externally derived clock is injected here. See Figure 3.
2	**$\overline{\text{Xtal}}$ (O/P):** The 3.58 MHz output of the clock oscillator inverter.
3	**Encoder Data Clock:** A logic port. External encode clock input.
4	**Encoder Output:** The encoder digital output.
5	**Encoder Data Enable:** Data is made available at the encoder output pin by control of this input. Internal 1 MΩ pullup.
6	**N/C**
7	**Encoder Input:** The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
8	V_{SS}: Negative Supply
9	**Bias Out:** Normally at $V_{DD}/2$ bias.
10	**Decoder Output:** The recovered analog signal is output at this pin. It is the buffered output of a bandpass filter and requires external components.
11	**Decoder Input:** The received digital signal input. Internal 1 MΩ pullup.
12	**Decoder Data Clock:** A logic port. External decode clock input.
13	**Serial Clock:** This is the serial clock input.
14	**Serial Data:** This is the serial data input. Data is loaded in the following order: VOL3, VOL2, VOL1, VOL0, ALGO, FORCE IDLE.
15	**Serial $\overline{\text{Load}}$/Latch Enable:** A logic 1 applied to this input will enable serial programming.
16	V_{DD}: Positive Supply.

CODEC INTEGRATION

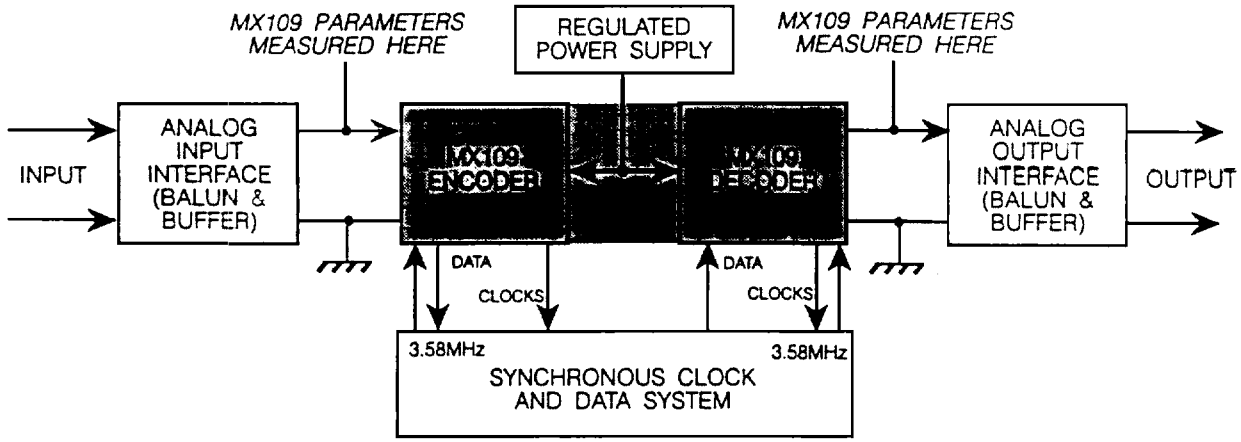
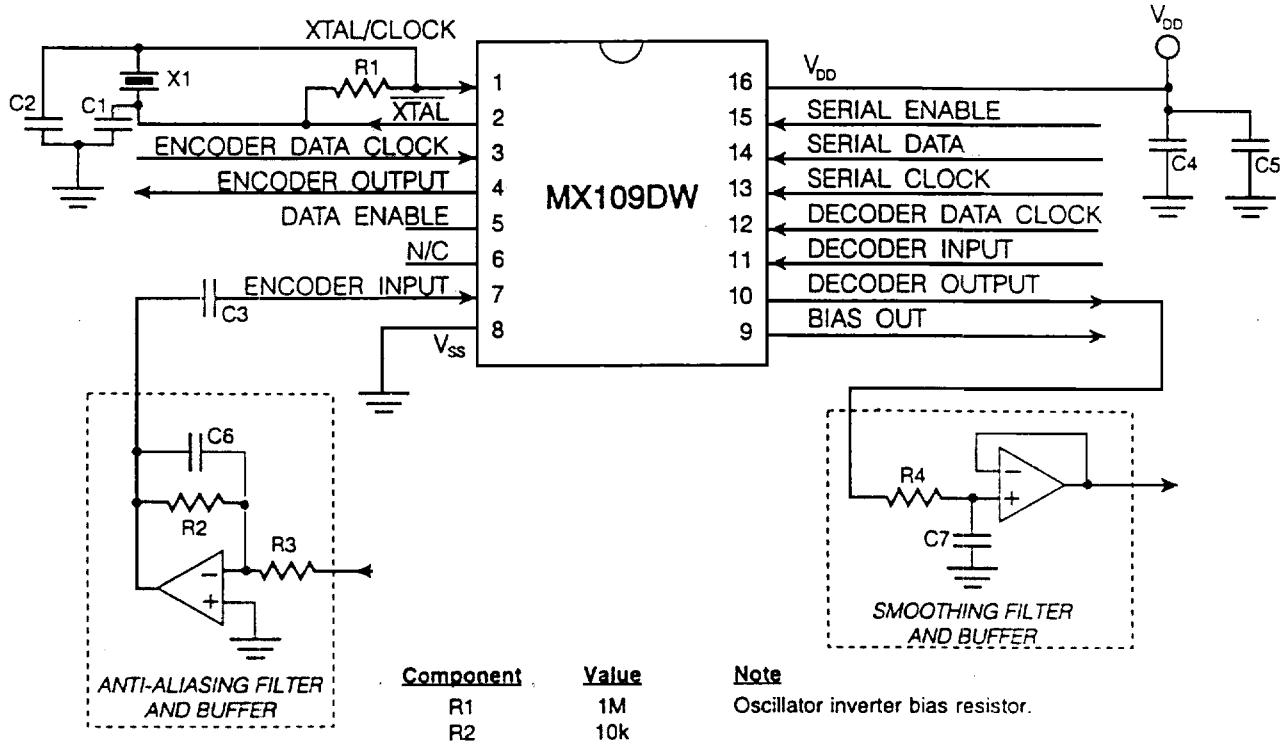


Figure 2 - System Configuration Showing the MX109



Component	Value	Note
R1	1M	Oscillator inverter bias resistor.
R2	10k	
R3	10k	
R4	10k	
C1	33p	Xtal circuit load capacitor.
C2	27p	Xtal circuit load capacitor.
C3	1.0µ	Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with an even lower source impedance.
C4	0.47µ	V_{DD} decoupling capacitor.
C5	0.001µ	
C6	0.0022µ	
C7	0.0022µ	
X1	3.58MHz	Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note (see MX-COM Product Handbook).

Tolerances: Resistors = 10%, Capacitors = 20%.

Figure 3 - Recommended External Components

CONTROL DATA

Serial data is loaded into the MX109's serial shift register together with the serial clock. When a logic "0" is applied to the Load/Latch input the serial data is loaded into the parallel register. A logic "1" on the Load/Latch input latches the data into the parallel register to be used elsewhere in the chip. The data word format and bit settings are shown below. The timing diagram for loading the serial data is shown in Figure 4.

Data Word Format

D7 VOL3	D6 VOL2	D5 VOL1	D4 VOL0	D3 ALGO	D2 FORCE IDLE	D1 RESERVED (0)	D0 RESERVED (0)
AMP/ATTENUATION LEVEL							

Bit Settings

Gain/Attenuation Selection

GAIN	VOL3	VOL2	VOL1	VOL0
9dB	1	1	1	1
6dB	1	1	1	0
3dB	1	1	0	1
0dB	1	1	0	0
-3dB	1	0	1	1
-6dB	1	0	1	0
-9dB	1	0	0	1
-12dB	1	0	0	0
-15dB	0	1	1	1
-18dB	0	1	1	0
-21dB	0	1	0	1
-24dB	0	1	0	0
-27dB	0	0	1	1
-30dB	0	0	1	0
-33dB	0	0	0	1
MUTE	0	0	0	0

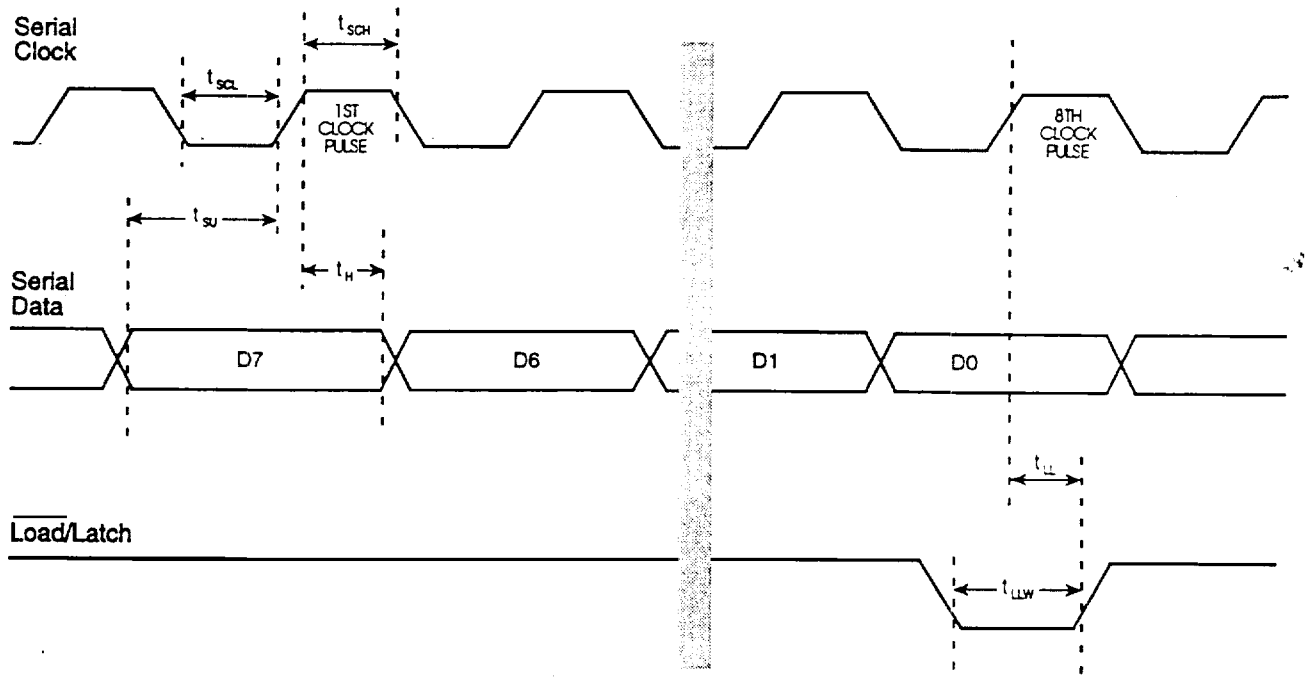
Companding Algorithm Settings

ALG	Algorithm Status
0	3-bit companding
1	4-bit companding

Forced Idle Settings

FORCE IDLE	Encoder Output
1	1010101010 . . .
0	CVSD encoded signal

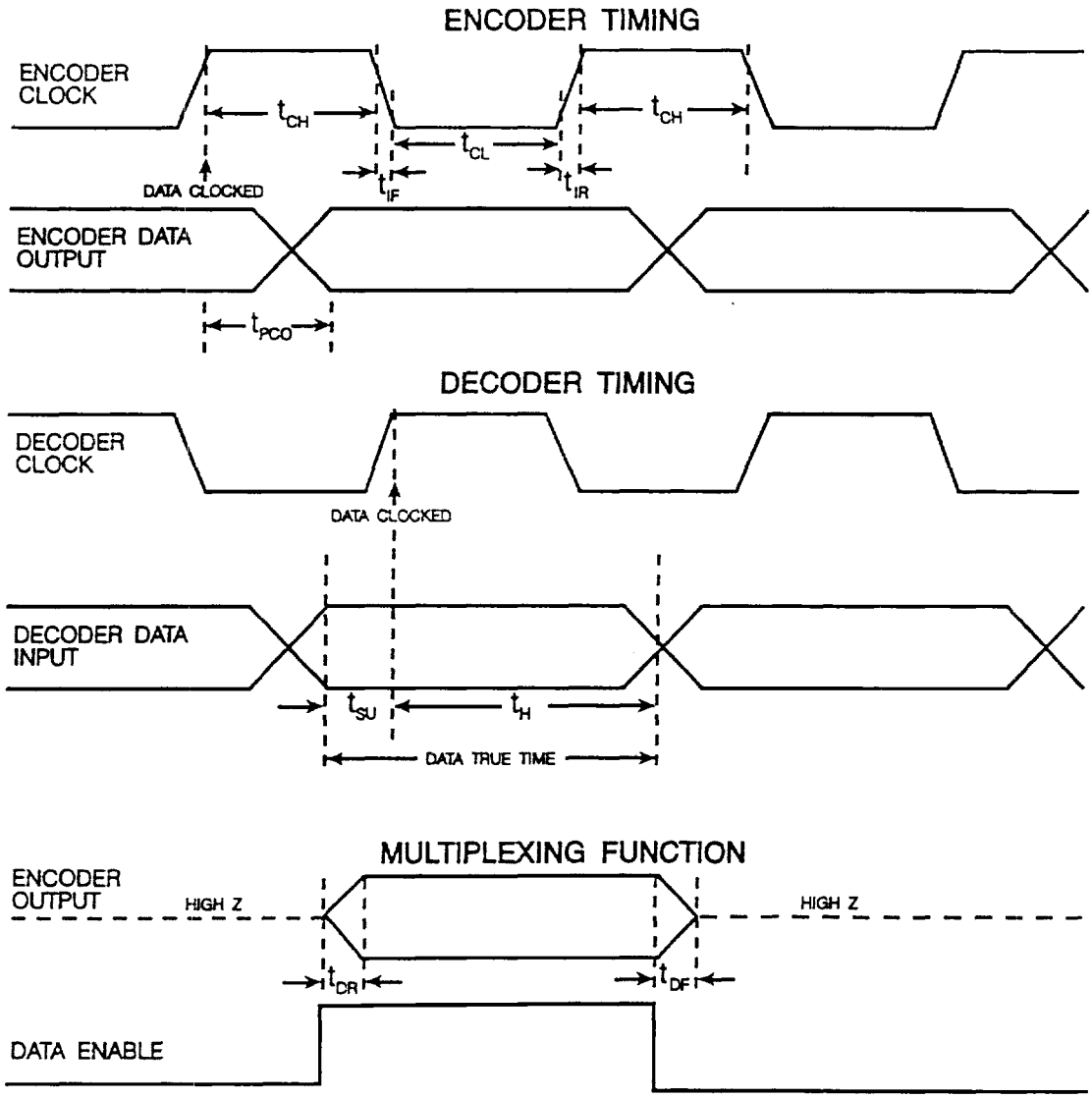
SERIAL INTERFACE TIMING



Abbreviation	Description	Time
t_{SCH}	Serial Clock high pulse width	50ns min.
t_{SU}	Data set-up time	30ns min.
t_{LL}	$\overline{\text{Load}}$/Latch set-up time	50ns min.
t_{SCL}	Serial Clock low pulse width	50ns min.
t_H	Data hold time	40ns min.
t_{LLW}	$\overline{\text{Load}}$/Latch pulse width	80ns min.

Figure 4 - Serial Interface Timing

CODEC TIMING INFORMATION



Abbreviation	Description	Time
t_{CH}	Clock pulse width (logic 1)	1.0µs min.
t_{CL}	Clock pulse width (logic 0)	1.0µs min.
t_{IR}	Clock rise time	100ns typ.
t_{IF}	Clock fall time	100ns typ.
t_{SU}	Data set-up time	450ns max.
t_H	Data hold time	600ns min.
$t_{SU} + t_H$	Data true time	1.5µs typ.
t_{PCO}	Clock to output delay time	750ns typ.
t_{DR}	Data rise time	100ns typ.
t_{DF}	Data fall time	100ns typ.
	Xtal input frequency	3.58MHz

Figure 5 - Codec Timing

CODEC PERFORMANCE

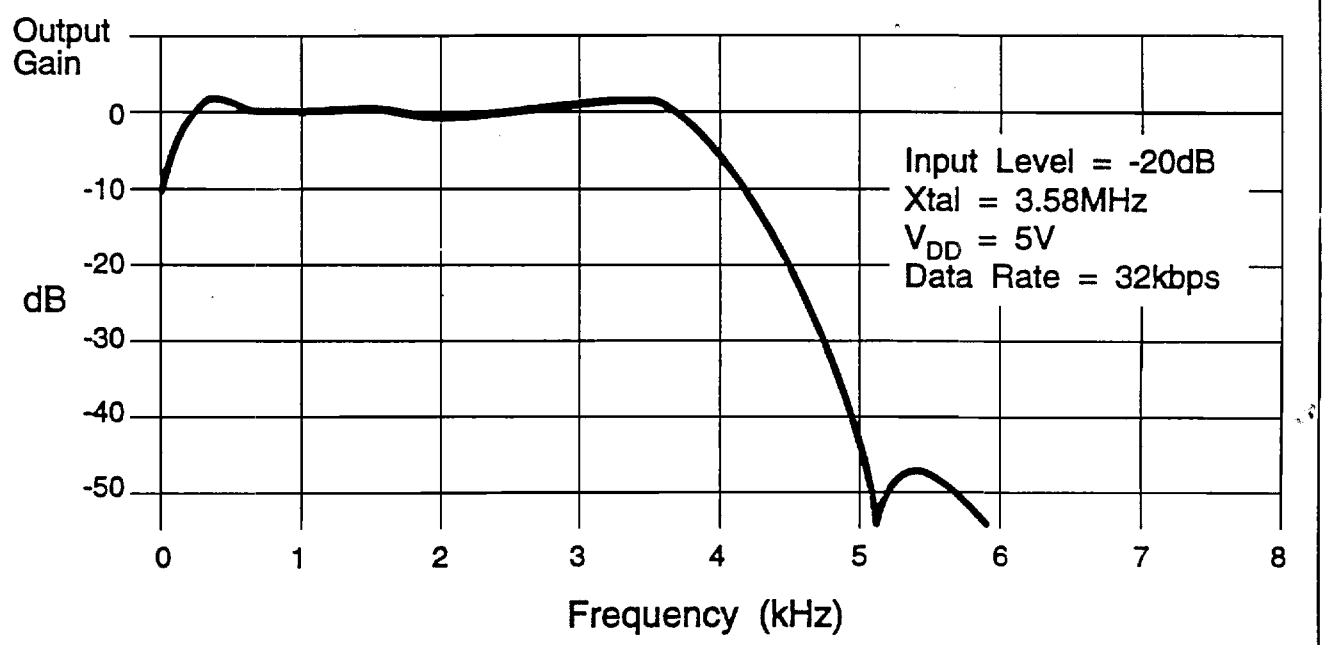


Figure 6 - Typical Codec Frequency Response

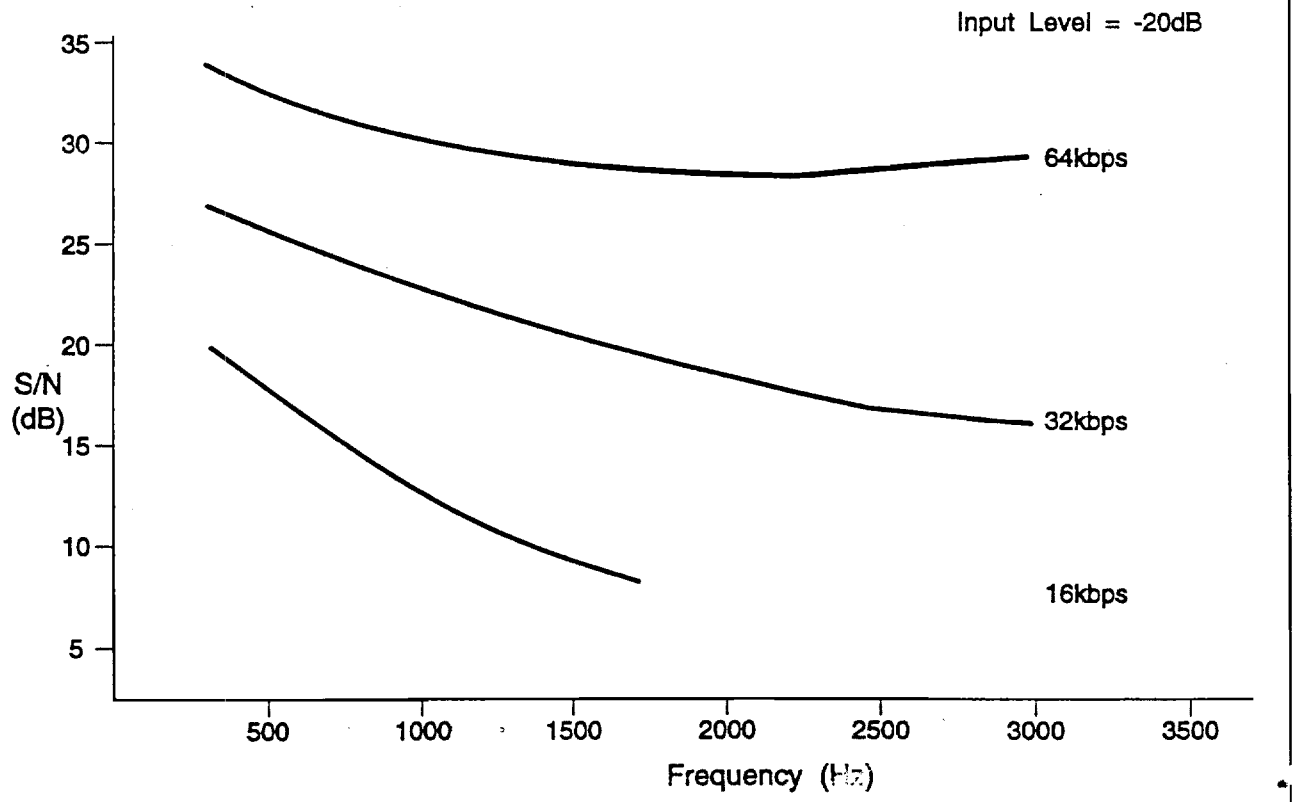


Figure 7 - Typical S/N Ratio with Input Frequency

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{ss}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current	
(Supply)	±30mA
(Other Pins)	±20mA
Total Device Dissipation (@ T_{amb}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-30°C to +70°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

Audio Test Frequency = 820Hz

T_{AMB} = 25°C

Sample Clock Rate = 32 kbps

Xtal/Clock f_o = 3.58MHz

Audio level 0dB ref (0 dBmO) = 500mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	3.6	-	5.5	V
Supply Current		-	5.0	-	mA
Input Logic "1"		70%V_{DD}	-	-	V
Input Logic "0"		-	-	30%V_{DD}	V
Output Logic "1"		80%V_{DD}	-	-	V
Output Logic "0"		-	-	20%V_{DD}	V
Digital Input Impedance					
Logic I/O Pins		-	10	-	MΩ
Logic Input Pins, Pullup Resistor	2	300	-	-	kΩ
Digital Output Impedance		-	4	-	kΩ
Analog Input Impedance		-	100	-	kΩ
Analog Output Impedance	6	-	200	-	Ω
Insertion Loss	2	-	0	-	dB
Dynamic Values	1				
Encoder:					
Analog Signal Input Levels	6	-30	-	+6	dB
Principal Integrator Frequency		-	275	-	Hz
Encoder Passband		-	3700	-	Hz
Compand Time Constant		-	4	-	ms
Decoder:					
Analog Signal Output Levels	6	-33	0	+9	dB
Decoder Passband	3	-	3700	-	Hz
Encoder/Decoder (Full Codec):					
Passband		300	-	3400	Hz
Stopband		6	-	10	KHz
Stopband Attenuation		-	60	-	dB
Passband Gain		-	0	-	dB
Passband Ripple		-3	-	+3	dB
Output Noise (Input Short Circuit)		-	-60	-	dB
Group Delay Distortion	4				
(1000Hz-2600Hz)		-	-	450	µs
(600Hz-2800Hz)		-	-	750	µs
(500Hz-3000Hz)		-	-	1.5	µs
Xtal/Clock Frequency		3.0	3.58	4.0	MHz

NOTES:

1. Dynamic characteristics specified at 5V only.
2. All logic inputs except Encoder and Decoder Data Clocks.
3. With passband gain of ±1dB.
4. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
5. Relative Timings are shown in Figure 4.
6. Recommended values.

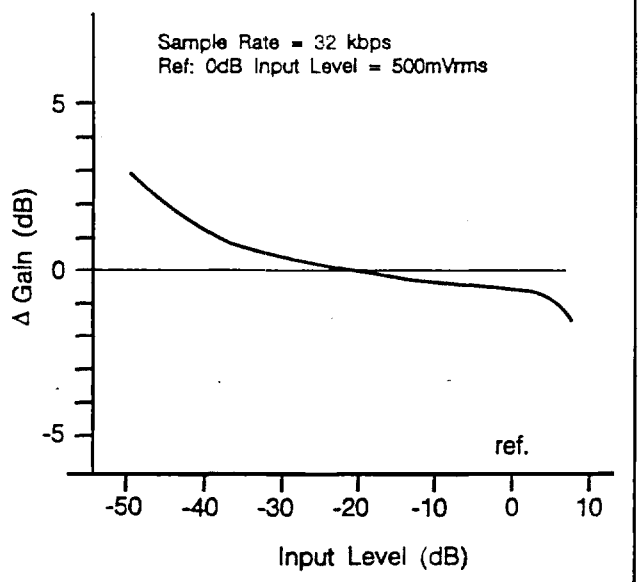


Figure 8 - Typical Variation of Gain with Input Level

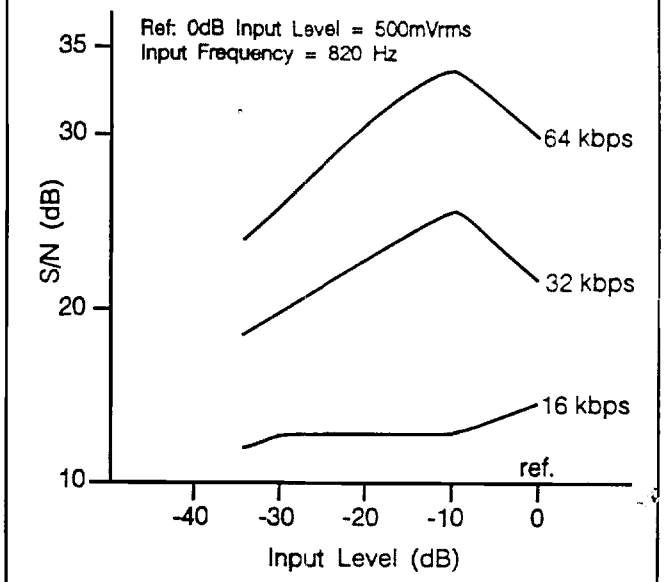


Figure 9 - Typical S/N Ratio with Input Level

Package Information

The MX109 16-lead Plastic DIP package is shown in Figure 9, the SOIC package in Figure 10, and the Ceramic DIP in Figure 11. For identification purposes the packages have an ident spot adjacent to pin 1.

Handling Precautions

The MX109 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

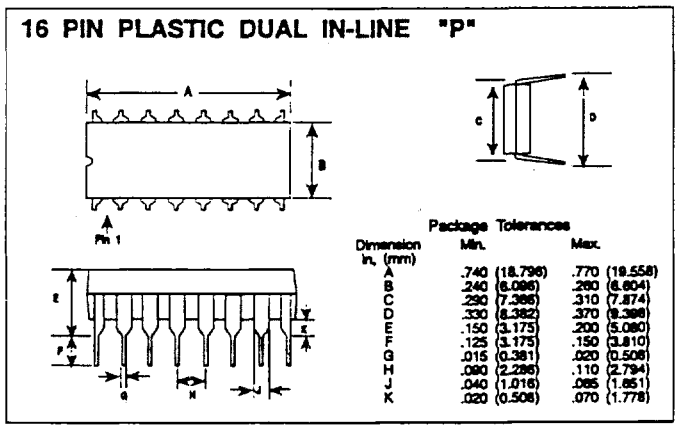


Figure 10 - MX109P

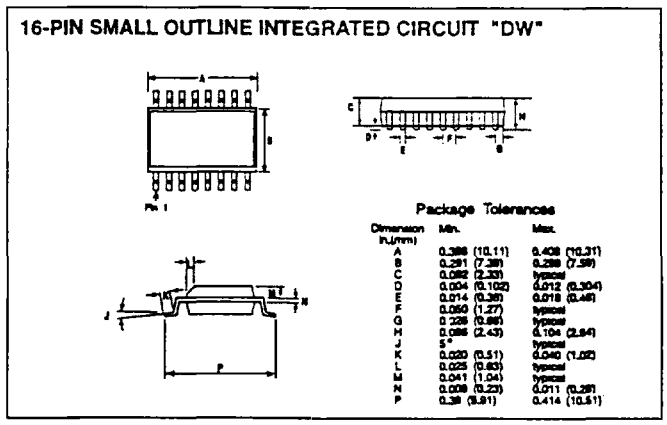


Figure 11 - MX109DW

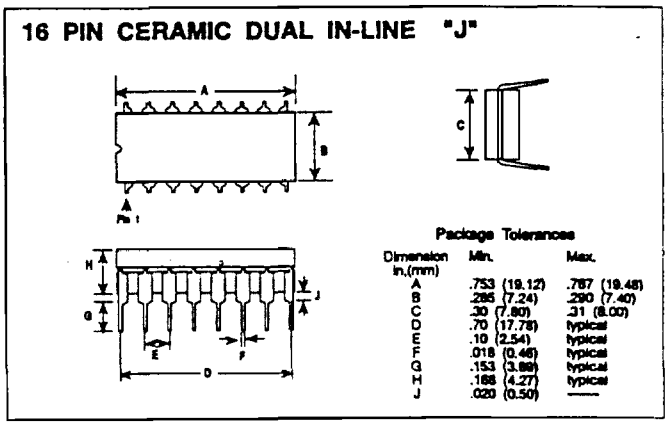


Figure 12 - MX109J