16M X 72 Bit DRAM DIMM with EDO Mode and ECC Optimized

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
STI...-60VG	60ns	20ns	110ns	30ns
STI...-70VG	70ns	25ns	130ns	33ns

- EDO Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only refresh capability
- LVTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- 8192 cycles/64ms refresh
- JEDEC standard pinout
- ECC Optimized
- Gold edge connectors

GENERAL DESCRIPTION

The Simple Technology STI7216207D1-xxVG is a 16M x 72 bit Dynamic RAM high density memory module. The module consists of eighteen 16M x 4 bit DRAMs in a 32-pin 400-mil TSOP-II packages. The DRAMs are mounted on a 168-pin glass epoxy substrate. A 0.1µF decoupling capacitor is mounted for each DRAM. Selected inputs and outputs are buffered for improved performance and easier memory subsystem design.

The STI7216207D1-xxVG is a Dual In-line Memory Module with gold edge connections, 3.3V power supply, EDO, and 8K refresh. The STI7216207D1-xxVG is optimized for ECC and intended for mounting into 168-pin edge connector sockets.

The STI7216207D1-60VG has a performance of t_{RAC}=60ns, and the STI7216207D1-70VG has a performance of t_{RAC}=70ns.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	NC	49	V_{CC}	73	V_{CC}	97	DQ_{45}	121	A_9	145	NC
2	DQ_0	26	V_{CC}	50	NC	74	DQ_{32}	98	DQ_{46}	122	A_{11}	146	NC
3	DQ_1	27	$\overline{WE}_0$	51	NC	75	DQ_{33}	99	DQ_{47}	123	NC	147	NC
4	DQ_2	28	$\overline{CAS}_0$	52	DQ_{18}	76	DQ_{34}	100	DQ_{48}	124	V_{CC}	148	NC
5	DQ_3	29	NC	53	DQ_{19}	77	DQ_{35}	101	DQ_{49}	125	NC	149	DQ_{61}
6	V_{CC}	30	$\overline{RAS}_0$	54	V_{SS}	78	V_{SS}	102	V_{CC}	126	B_0	150	DQ_{62}
7	DQ_4	31	$\overline{OE}_0$	55	DQ_{20}	79	PD_1	103	DQ_{50}	127	V_{SS}	151	DQ_{63}
8	DQ_5	32	V_{SS}	56	DQ_{21}	80	PD_3	104	DQ_{51}	128	NC	152	V_{SS}
9	DQ_6	33	A_0	57	DQ_{22}	81	PD_5	105	DQ_{52}	129	NC	153	DQ_{64}
10	DQ_7	34	A_2	58	DQ_{23}	82	PD_7	106	DQ_{53}	130	NC	154	DQ_{65}
11	DQ_8	35	A_4	59	V_{CC}	83	ID_0	107	V_{SS}	131	NC	155	DQ_{66}
12	V_{SS}	36	A_6	60	DQ_{24}	84	V_{CC}	108	NC	132	$\overline{PDE}$	156	DQ_{67}
13	DQ_9	37	A_8	61	NC	85	V_{SS}	109	NC	133	V_{CC}	157	V_{CC}
14	DQ_{10}	38	A_{10}	62	NC	86	DQ_{36}	110	V_{CC}	134	NC	158	DQ_{68}
15	DQ_{11}	39	A_{12}	63	NC	87	DQ_{37}	111	NC	135	NC	159	DQ_{69}
16	DQ_{12}	40	V_{CC}	64	NC	88	DQ_{38}	112	NC	136	DQ_{54}	160	DQ_{70}
17	DQ_{13}	41	NC	65	DQ_{25}	89	DQ_{39}	113	NC	137	DQ_{55}	161	DQ_{71}
18	V_{CC}	42	NC	66	DQ_{26}	90	V_{CC}	114	NC	138	V_{SS}	162	V_{SS}
19	DQ_{14}	43	V_{SS}	67	DQ_{27}	91	DQ_{40}	115	NC	139	DQ_{56}	163	PD_2
20	DQ_{15}	44	$\overline{OE}_2$	68	V_{SS}	92	DQ_{41}	116	V_{SS}	140	DQ_{57}	164	PD_4
21	DQ_{16}	45	$\overline{RAS}_2$	69	DQ_{28}	93	DQ_{42}	117	A_1	141	DQ_{58}	165	PD_6
22	DQ_{17}	46	$\overline{CAS}_4$	70	DQ_{29}	94	DQ_{43}	118	A_3	142	DQ_{59}	166	PD_8
23	V_{SS}	47	NC	71	DQ_{30}	95	DQ_{44}	119	A_5	143	V_{CC}	167	ID_1
24	NC	48	$\overline{WE}_2$	72	DQ_{31}	96	V_{SS}	120	A_7	144	DQ_{60}	168	V_{CC}

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PIN CONFIGURATION (continued)

Pin Names

Pin Name	Pin Function
A_0, B_0, A_1-A_{12}	Address Inputs (Buffered)
DQ_0-DQ_{71}	Data In/Out
$\overline{WE}_0$, $\overline{WE}_2$	Read/Write Input (Buffered)
$\overline{OE}_0$, $\overline{OE}_2$	Output Enable (Buffered)
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Adress Strobe
$\overline{CAS}_0$, $\overline{CAS}_4$	Column Address Strobe (Buffered)
PD_1-PD_8	Presence Detect (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID_0-ID_1	ID Bits
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect

For 4Mx72 Bits Configuration with 4M x 4 Bits chips and 8K Refresh:

PD_1=V_{CC}, PD_2=V_{CC}, PD_3=V_{CC}, PD_4=V_{CC}

For EDO:

PD_5=V_{CC}

Speed:

Pin	60ns	70ns
PD_6	V_{CC}	V_{SS}
PD_7	V_{CC}	V_{CC}

For ECC:

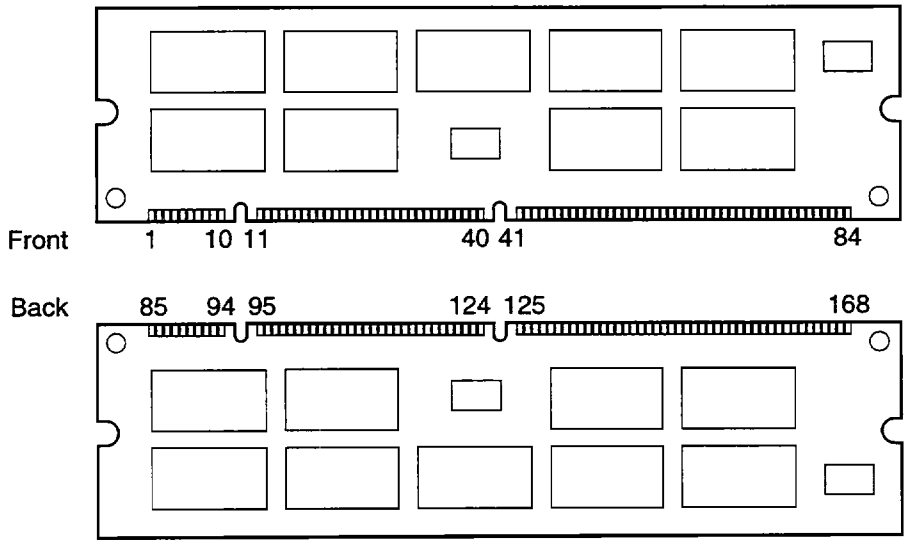
PD_8=V_{SS}

For x72 ECC:

ID_0 =V_{SS}

For Normal Refresh Mode:

ID_1=V_{SS}



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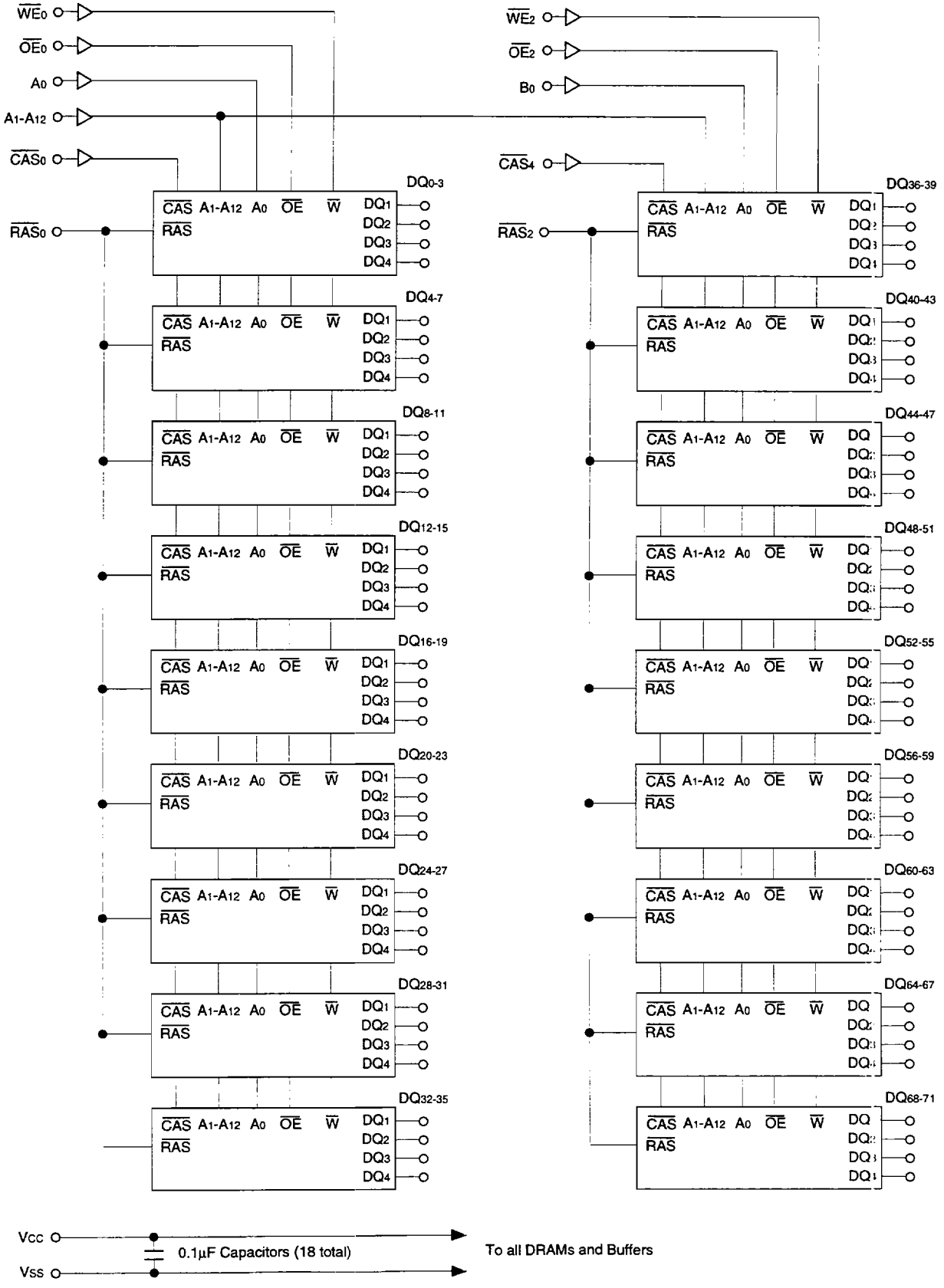
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	18	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}; T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	-0.3**	—	0.8	V

* V_{CC}+1.3V/15ns. Pulse width is measured at V_{CC}.

** -1.3V/15ns. Pulse width is measured at V_{SS}.

DC AND OPERATION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	STI...-60VG STI...-70VG	I_{CC1}	— —	1620 1440	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WE}$=V_{IH})		I_{CC2}	—	100	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	STI...-60VG STI...-70VG	I_{CC3}	— —	1620 1440	mA mA
EDO Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{HPC}=min.)	STI...-60VG STI...-70VG	I_{CC4}	— —	1800 1620	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WE}$=V_{CC}-0.2V)		I_{CC5}	—	30	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	STI...-60VG STI...-70VG	I_{CC6}	— —	1620 1440	mA mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V; all other pins not under test=0V)	All but $\overline{RAS}$ $\overline{RAS}$	I_{IL}	-5 -45	5 45	µA µA
Output Leakage Current (Data out is disabled; 0≤V_{OUT}≤V_{CC})		I_{OL}	-5	5	µA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	—	0.4	V

* I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle.

CAPACITANCE (T_A=25 °C; V_{CC}=3.3V; f=1Mhz)

Item	Symbol	Typ	Units
Input Capacitance (A_0, B_0, A_{1-12}, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN1}	20	pF
Input Capacitance ($\overline{RAS}$)	C_{IN2}	78	pF
Input/Output Capacitance (DQ_0-DQ_{71})	C_{DQ1}	22	pF

AC CHARACTERISTICS

(0 °C≤T_A≤70 °C; V_{CC}=3.3V±0.3V; V_{IH}/V_{IL}=2.0/0.8V; V_{OH}/V_{OL}=2.0/0.8V; Output loading C_L=100pF; See notes 1 and 2)

Parameter	Symbol	STI...-60VG		STI...-70VG		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		ns	
Read-modify-write cycle time	t_{RWC}	153		185		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25	ns	3,4,5,15
Access time from column address	t_{AA}		35		40	ns	3,11,15
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,15
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,15
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	20	8	25	ns	7,12,13,15
Transition time (rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	15
$\overline{CAS}$ hold time	t_{CSH}	43		48		ns	15
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	ns	14
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	40	18	45	ns	4,15
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	13	30	ns	11,15
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	15
Row address set-up time	t_{ASR}	5		5		ns	15
Row address hold time	t_{RAH}	8		8		ns	15
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	10		15		ns	
Col. addr. hold time ref. to $\overline{RAS}$	t_{AR}	43		53		ns	6,15
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		ns	15
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	9,15
Write command hold time	t_{WCH}	10		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		ns	6

continued on the next page

AC CHARACTERISTICS (continued)

Parameter	Symbol	STI...-60VG		STI...-70VG		Unit	Notes
		Min	Max	Min	Max		
Write command pulse width	t_{WP}	10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	15
Write command to $\overline{CAS}$ lead time	t_{CWL}	10		15		ns	
Data set-up time	t_{DS}	-2		-2		ns	10,15
Data hold time	t_{DH}	15		20		ns	10,15
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		ns	6
Refresh period (2K refresh)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	38		45		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	81		94		ns	8,15
Column address to $\overline{WE}$ delay time	t_{AWD}	53		60		ns	8
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	60		70		ns	
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	10		10		ns	15
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	8		13		ns	15
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	15
$\overline{CAS}$ prechrg. (C-B-R counter test cycle)	t_{CPT}	20		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45	ns	3,15
Hyper Page cycle time	t_{HPC}	30		33		ns	14
Hyper Page read-modify-write cycle time	t_{HPRWC}	77		92		ns	14
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200,000	70	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHPC}	40		45		ns	15
$\overline{OE}$ access time	t_{OEA}		20		25	ns	15
$\overline{OE}$ to data delay	t_{OED}	18		25		ns	15
Output buffer turn off delay from $\overline{OE}$	t_{OEZ}	5	18	5	25	ns	7,12,15
$\overline{OE}$ command hold time	t_{OEH}	15		20		ns	
$\overline{WE}$ to $\overline{RAS}$ precharge (C-B-R refresh)	t_{WRP}	15		15		ns	15
$\overline{WE}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	8		8		ns	15
Output data hold time	t_{DOH}	10		10		ns	15
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	3	20	ns	7,12,13
Output buffer turn off delay from $\overline{WE}$	t_{WEZ}	3	20	3	25	ns	7,12,15
$\overline{WE}$ to data delay	t_{WEC}	20		25		ns	15
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{WE}$ pulse width (Hyper Page cycle)	t_{WPE}	5		5		ns	
$\overline{PDE}$ to valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit inactive	t_{PDOFF}	2	7	2	7	ns	

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AC CHARACTERISTICS (continued)

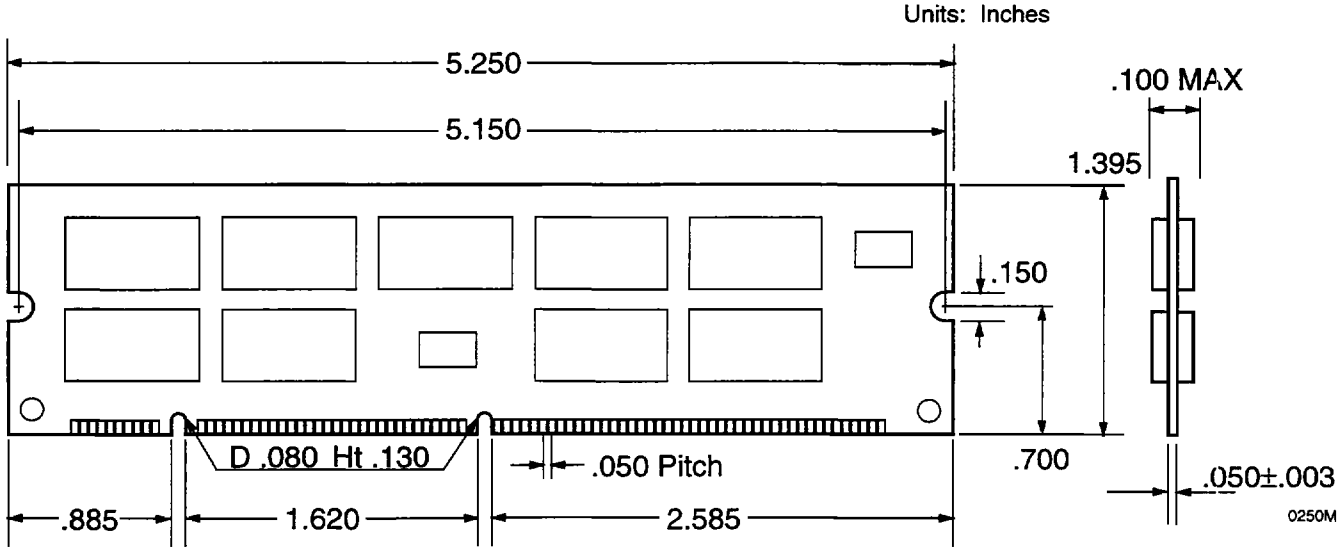
Notes

1. An initial pause of 200µs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF, V_{oh}=2.0V and V_{ol}=0.8V.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes the $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are non-restrictive operatin parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminated.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parametners are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
13. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. $t_{ASC} \geq t_{CP}$(min).
15. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

Timing Diagrams

Please refer to attached Timing Chart IX.

PACKAGE DIMENSIONS



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED