ANALOG DEVICES

OC-3 / OC-12 / GbE / OC-48 / FEC Multirate CDR for WDM Transponders

Preliminary Technical Data ADN2809

FEATURES

- **Meets SONET Requirements for**
  Jitter Transfer / Generation / Tolerance
- **Quantizer Sensitivity: 6 mV**
  Adjustable Slice Level: +/- 100 mV
  1.9GHz minimum Bandwidth
  Loss of Signal Detect Range: 4mV to 17mV
- **Single Reference Clock Frequency for all rates**
  Including 15/14 (7%) Wrapper Rate
  Choice of 19.44, 38.88, 77.76 or 155.52MHz
  LVPECL / LVDS / LVCMOS compatible inputs
  19.44MHz Crystal Oscillator for Module apps
- **Loss of Lock indicator**
- **Loopback mode for High Speed Test Data**
- **Squelch & Bypass features**
- **Single Supply Operation: 3.3 Volts (±10 %)**
  Low Power: 780 mW Typical
- **Patented Clock Recovery Architecture**
- **7 x 7 mm 48 pin LFCSP Package**

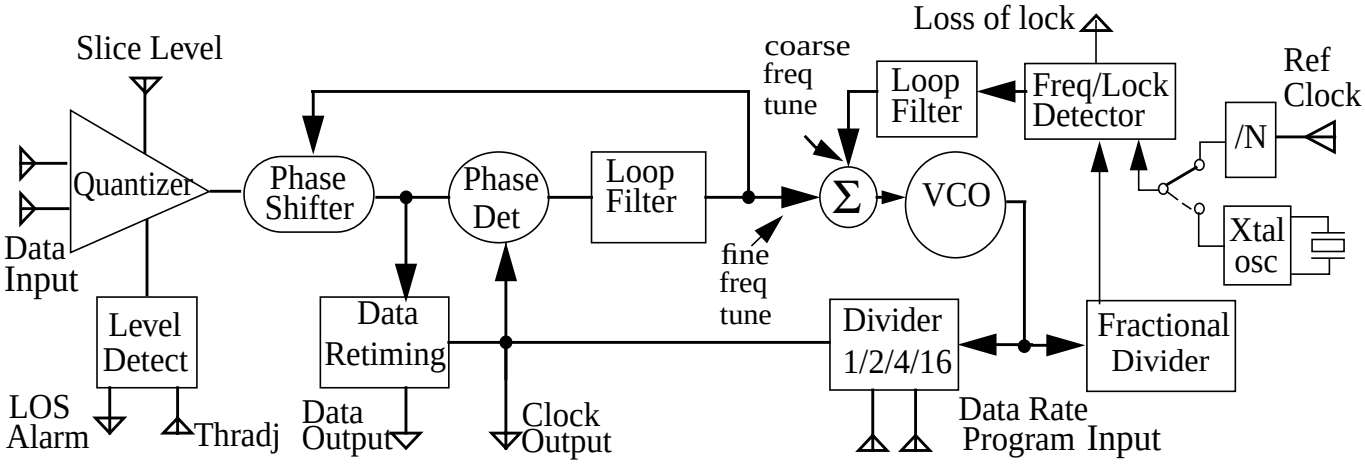
PRODUCT DESCRIPTION

The ADN2809 provides the receiver functions of Quantization, Signal Level Detect and Clock and Data Recovery at rates of OC-3, OC-12, Gigabit Ethernet, OC-48 and all FEC rates. All SONET jitter requirements are met, including: Jitter Transfer; Jitter Generation; and Jitter Tolerance. All specifications are quoted for -40 to 85C ambient temperature.

The device is intended for WDM system applications and requires an external reference clock frequency or crystal. Both native rates and 15/14 rate digital 'wrappers' are supported by the ADN2809, without any change of reference clock.

This device together with a PIN diode and a TIA preamplifier can implement a highly integrated, low cost, low power fiber optic receiver.

The receiver front end Signal Detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The Signal Detect has 3dB optical hysteresis to prevent chatter at the output.



REV. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

QUANTIZER DC CHARACTERISTICS Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Input Voltage Range	Single Ended, DC Coupled Input	0		1.2	Volts
Common Mode Voltage		0.4		1.2	V
Maximum Peak to Peak Differential Input	@PIN or NIN AC Coupled I/P (1)			2.4	V
Sensitivity, Vsense (Peak to Peak Differential)	PIN - NIN, BER< 1e-10, AC Coupled Input	10	6		mV
Overdrive, Vod	BER <1e-10	5	3		mV
Offset Voltage				1	mV
Input Current			10	20	uA
Input RMS Noise			244		uV rms

QUANTIZER AC CHARACTERISTICS Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Input Resistance	Single Ended	45	50	55	Ohm
Input Capacitance (2)		500	650	800	fF
Pulsewidth Distortion (2)			10		ps
Small Signal Bandwidth		1.9			GHz
Small Signal Gain	Differential		54		dB
Power Supply Rejection (2)	100mVp-p noise at 100MHz on Vcc		60		dB
S11 (2)	Measured at 2.5GHz			-15	dB

Notes: (1) Recommended for Optimum Sensitivity
(2) Not production tested

QUANTIZER SLICE ADJUSTMENT Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Gain (Threshold / Vin)	Vin=SliceP-SliceN	0.131		0.134	V/V
Control Voltage Range	SliceP - SliceN	-0.8		0.8	V
	SliceP or SliceN	1.3		AVCC	V
Slice Threshold Offset	Full input range	-1.0		1.0	mV

LEVEL DETECT Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Level Detect Range (see Figure 4) (Peak to Peak Differential)	Rthresh = 0	2	3	4	mV
	Rthresh = 10k	6	8.8	12	mV
	Rthresh = 200k	15	17	21	mV
Hysteresis: Electrical (AC Coupled Input)	Rthresh = 0		5	7	dB
	Rthresh = 10k		5	7	dB
	Rthresh = 200k		5	7	dB
Response Time	DC coupled	0.1	3	5	us
SDOUT O/P Logic High	Load = +2.0mA	2.7	3		V
SDOUT O/P Logic Low	Load = -2.0mA		0.2	0.4	V
	Level Detect Output is logic “1” LVCMOS compatible with no signal present				

POWER SUPPLY Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
VOLTAGE		3.0		3.6	V
CURRENT		140	236	380	mA

PHASE-LOCKED LOOP CHARACTERISTICS Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Jitter Transfer Bandwidth (see Figure 5)	OC-48		617	**2000**	kHz
	Gigabit Ethernet		282	**1000**	kHz
	OC-12		135	**500**	kHz
	OC-3		33	**130**	kHz
Jitter Tolerance Tracking Bandwidth (see Figure 5)	OC-48	**1.0**	2.6		MHz
	Gigabit Ethernet	**0.5**	2.8		MHz
	OC-12	**0.25**	2.9		MHz
	OC-3	**0.065**	3.0		MHz
Jitter Generation (12kHz to 20MHz)	OC-48		0.003	**0.01**	UI rms
			0.03	**0.1**	UIp-p
	Gigabit Ethernet		0.003	**0.01**	UI rms
			0.03	**0.1**	UIp-p
	OC-12		0.003	**0.01**	UI rms
			0.03	**0.1**	UIp-p
	OC-3		0.003	**0.01**	UI rms
			0.03	**0.1**	UIp-p
Jitter Peaking	OC-48		0.002	**0.1**	dB
	Gigabit Ethernet		0.003	**0.1**	dB
	OC-12		0.007	**0.1**	dB
	OC-3		0.027	**0.1**	dB

NOTE: SONET SPECS APPEAR IN BOLD

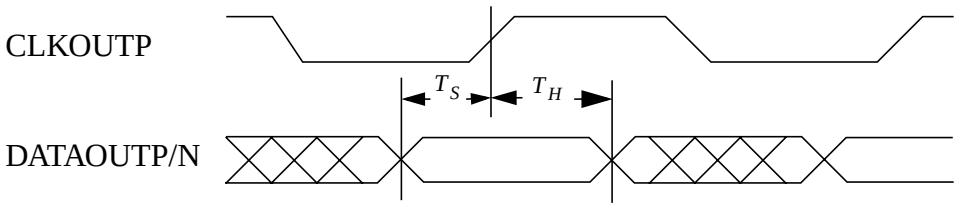
CML OUTPUT FORMAT Referred to Vcc Vcc=3.3V, Vee=gnd, Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Differential Output Voltage Swing V_{SE} (Fig 2 & Fig 11)	50 ohms to VCC	320	430	550	mV
Rise/Fall Time tR/tF	20% / 80%			120	ps
Output High Voltage V_{OH}	50 ohms to VCC	VCC			
Output Low Voltage V_{OL}	50 ohms to VCC	VCC-0.55		VCC-0.32	V
Data Setup Time (Fig 1) T_S	OC48 Gigabit Ethernet OC12 OC3	150 350 750 3150			ps
Data Hold Time (Fig 1) T_H	OC48 Gigabit Ethernet OC12 OC3	150 350 750 3150			ps

TEST DATA DC CHARACTERISTICS Vcc=3.3V, Vee=gnd, Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Input Voltage Swing V_{SE} (Fig 2)	Single Ended	0.06		0.8	V
Input Voltage Range		2.3		VCC+0.4	V

FIGURE 1 Output Timing Definitions



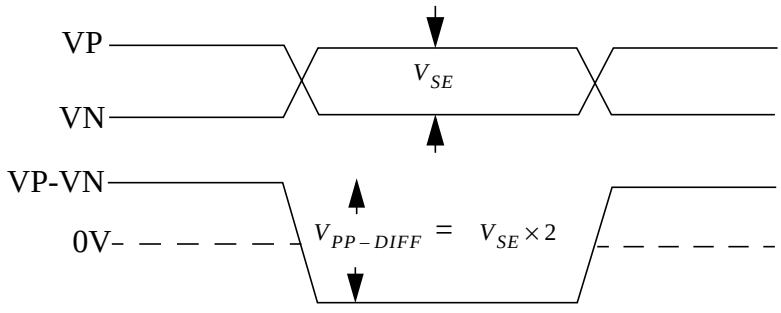
LVTTL DC CHARACTERISTICS Vcc=3.3V, Vee=gnd, Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
V_{OH} Output High Voltage	I_{OH} = -100uA	2.4			V
V_{OL} Output Low Voltage	I_{OL} = 1.0mA			0.5	V
V_{IH} Input High Voltage		2.0			V
V_{IL} Input Low Voltage				0.8	V
I_{IH} Input High Current	Vin = 2.4V			50	uA
I_{IL} Input Low Current	Vin = 0.5V	-500			uA

REFCLK DC CHARACTERISTICS Vcc=3.3V, Vee=gnd, Tamb = -40 to 85C

Parameter	Condition	Min	Typ	Max	Units
Input Voltage Swing V_{SE} (Fig 2)	Single Ended	0.032		VCC	V
Input Voltage Range		0		VCC	V

FIGURE 2 Signal Level Definition



THEORY OF OPERATION

The ADN2809 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops which share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop comprising the vco tracks the low frequency components of input jitter. The initial frequency of the vco is set by yet a third loop which compares the vco frequency with an external reference frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the vco by the fine tuning control.

The delay- and phase- loops together track the phase of the input data signal. For example, when the clock lags data, the phase detector drives the vco to higher frequency, and also, increases the delay through the phase shifter: these actions both serve to reduce the phase error between the clock and data. The faster clock picks up phase while the delayed data loses phase. Since the loop filter is an integrator, the static phase error will be driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second order phase-locked loop, and this zero is placed in the feedback path and thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Since this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay- and phase- loops together simultaneously provide wide-band jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 6 shows the jitter transfer function , Z(s)/X(s), is a second order low pass providing excellent filtering. Note the jitter transfer has no zero, unlike an ordinary second order phase-locked loop. This means that the main PLL loop has low jitter peaking, see Figure 7. This makes this circuit ideal for signal regenerator applications where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer, e(s)/X(s), has the same high pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wide-band jitter accommodation since the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering. See Figure 5 for a table of error transfer bandwidths and jitter transfer bandwidths at the various data rates.

The delay- and phase- loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case the vco is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the vco tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the vco are not large enough to track input jitter. In this case the vco control voltage becomes large and saturates and the vco frequency dwells at one or the other extreme of its tuning range. The size of the vco tuning range, therefore has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger, and so the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve . The phase shifter has a minimum range of 2UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region the gain of the integrator determines the jitter accommodation. Since the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5UI in this region. The corner frequency between the declining slope and the flat region is the closed loop bandwidth of the delay-locked loop, which is roughly 3MHz for all data rates.

FIGURE 3 Quantizer Signal Definitions

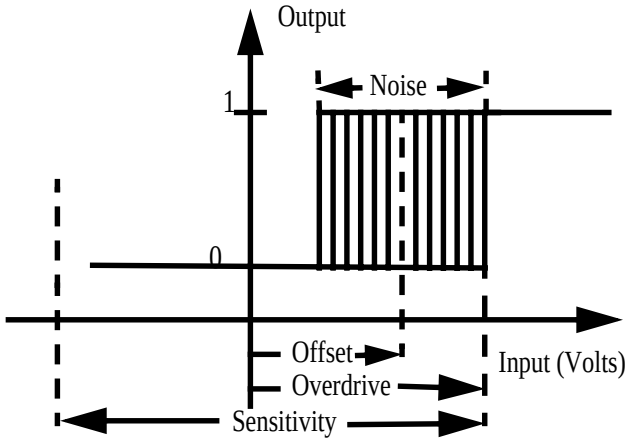


FIGURE 4 LOS Comparator Trip Point Programming

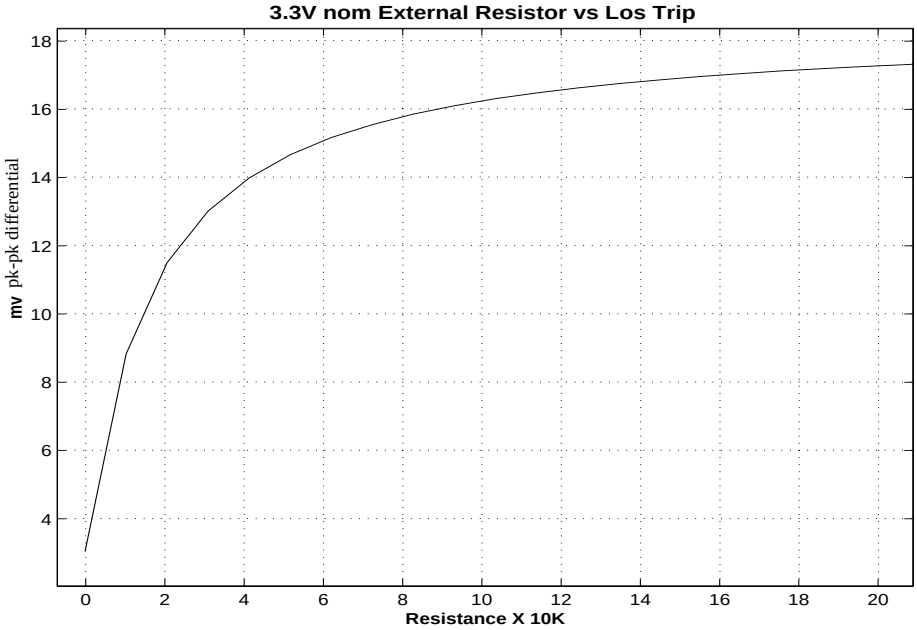
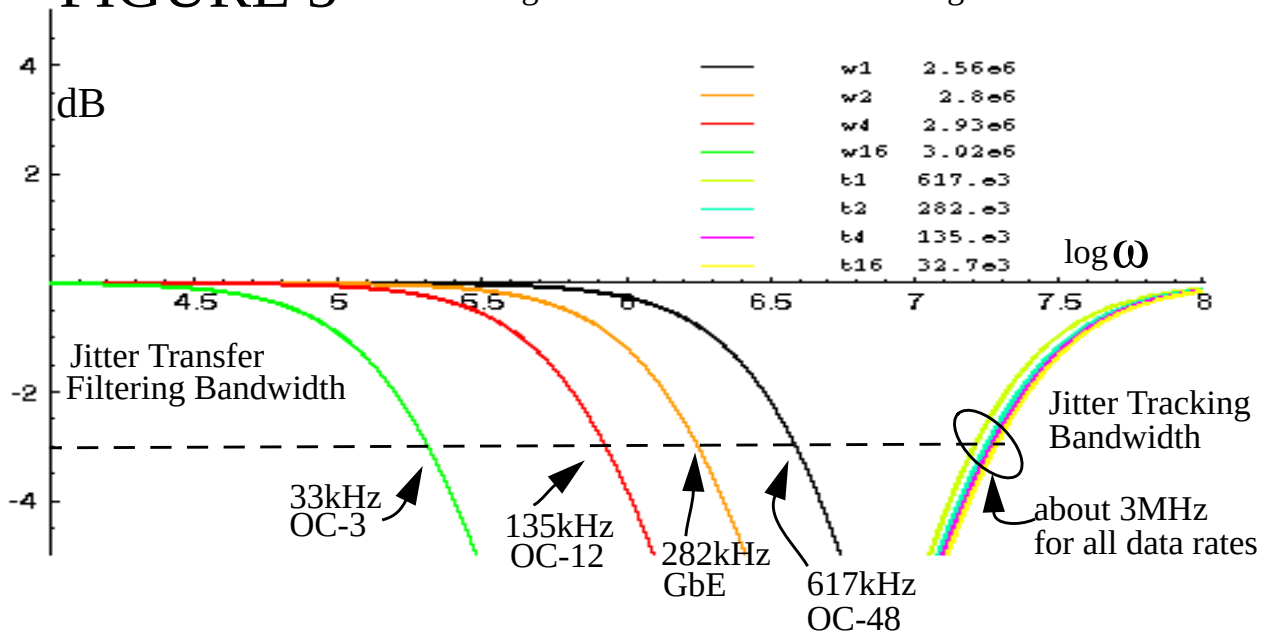


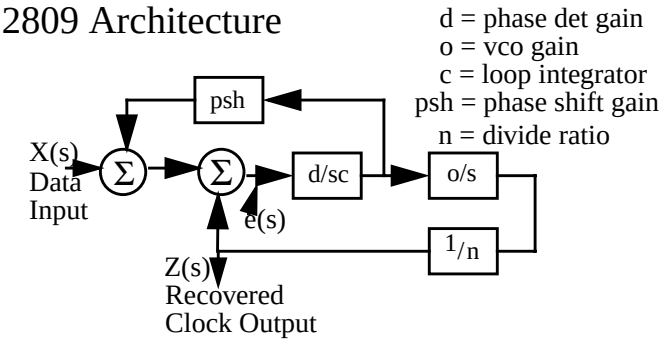
FIGURE 5 Tracking Bandwidth and Jitter Filtering



d= 16.e-6 c= 50.e-12 o= 195.e6 psh= 60.

FAST	Tol	Margin	SLOW	Tran	Margin
OC48					
2.56e6	1MHz	2.56	617.e3	2MHz	3.24
GbE					
2.8e6	500k	5.6	282.e3	1MHz	3.54
OC12					
2.93e6	250k	11.7	135.e3	500k	3.7
OC3					
3.02e6	65k	46.5	32.7e3	130k	3.98

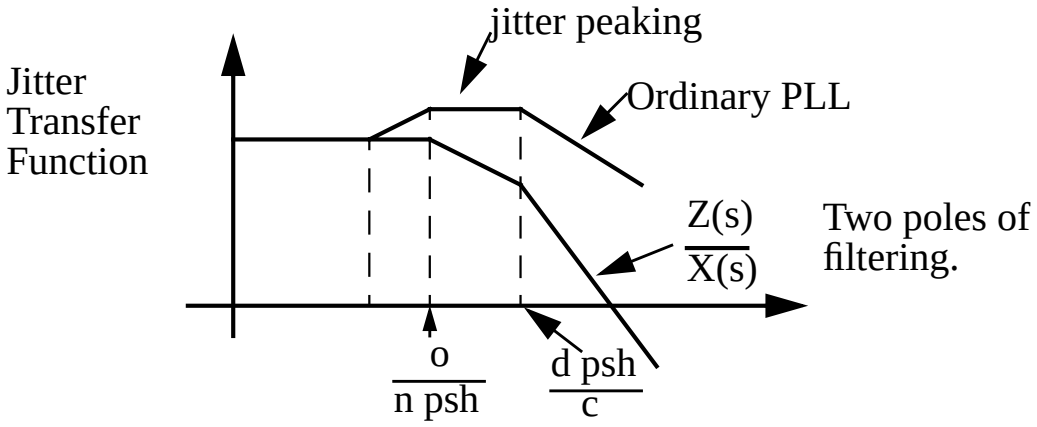
FIGURE 6 2809 Architecture



$$\frac{Z(s)}{X(s)} = \frac{1}{s^2 \frac{c\,n}{d\,o} + s \frac{n\,psh}{o} + 1}$$ Jitter Transfer Function

$$\frac{e(s)}{X(s)} = \frac{s^2}{s^2 + s \frac{d\,psh}{c} + \frac{d\,o}{c\,n}}$$ Tracking Error Transfer

FIGURE 7 2809 Jitter Response vs. Conventional PLL



FUNCTIONAL DESCRIPTION

Limamp / Bypass & Loopback

The limiting amplifier has differential inputs (PIN/NIN), which are normally AC coupled to the internal 50 ohm termination (although DC coupling is possible). Input offset is factory trimmed to achieve better than 4mV sensitivity with minimal drift. The Quantizer Slicing level can be offset by +/- 100mV to mitigate the effect of ASE (amplified spontaneous emission) noise by a differential voltage input of +/-0.8V applied to 'SLICEP/N' inputs. If no adjustment of the slice level is needed, SLICEP/N should be tied to AVCC.

When the 'Bypass' input is driven to a TTL high state, the Quantizer output is connected directly to the buffers driving the Data Out pins, thus bypassing the clock recovery circuit (Figure 8). This feature can help the system to deal with non standard bit rates.

The loopback mode can be invoked by driving the 'LOOPEN' pin to a TTL high state, which facilitates system diagnostic testing. This will connect the Test inputs (TDINP/N) to the clock and data recovery circuit (per Figure 8). The Test inputs can be left floating, when not in use. They accept AC or DC coupled signal levels, or AC coupled LVDS.

Loss of Signal (LOS) Detector

The receiver front end Signal Detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The threshold is set with a single external resistor, as illustrated in figure 4, which assumes that the slice inputs are inactive. The Signal Detect has 3dB optical hysteresis to prevent chatter at the output.

If the LOS detector is used the Quantizer Slice Adjust pins must both be tied to VCC, to avoid interaction with the LOS threshold level. Note that it is not expected to use both LOS and Slice Adjust at the same time: systems with optical amplifiers need the slice adjust to evade ASE, but a loss of signal causes the optical amplifier output to be full scale noise, thus the LOS would not detect the failure. In this case the Loss of Lock signal will indicate the failure.

Reference Clock

The ADN2809 can accept any of the following reference clock frequencies: 19.44 MHz, 38.88MHz, 77.76MHz at LVTTL/LVCMOS/LVPECL/LVDS levels or 155.52MHz at LVPECL/LVDS levels via the REFCLKN/P inputs, independent of data rate (including gigabit ethernet). The input buffer accepts any differential signal with a peak to peak differential amplitude of greater than 64mV (e.g. LVPECL or LVDS) or a standard single

ended low voltage TTL input, providing maximum system flexibility. The appropriate division ratio can be selected using the REFSEL0/1 pins, according to Table 2. Phase noise and duty cycle of the Reference Clock are not critical and 100ppm accuracy is sufficient.

A crystal oscillator is also provided, as an alternative to using the REFCLKN/P input. Details of the recommended crystal are given in Table 3.

REFSEL must be tied to VCC when the REFCLKN/P inputs are active, or tied to VEE when the oscillator is used. No connection between the XO pin and REFCLK input is necessary (see figure 9). Please note that the crystal should operate in series resonant mode, which renders it insensitive to external parasitics. No trimming capacitors are required.

Lock Detector Operation

The lock detector monitors the frequency difference between the VCO and the reference clock, and de-asserts the 'Loss of Lock' signal when the VCO is within 500ppm of center frequency. This enables the phase loop which then maintains phase lock, unless the frequency error exceeds 0.1%. Should this occur, the 'Loss of Lock' signal is re-asserted and control returns to the frequency loop which will re-acquire, and maintain a stable clock signal at the output.

Squelch Mode

When the 'Squelch' input is driven to a TTL high state, both the clock and data outputs are set to the zero state, to suppress downstream processing. If desired, this pin can be directly driven by the LOS (Loss-Of-Signal) or LOL (Loss-Of-Lock) detector outputs. If the Squelch function is not required, the pin should be tied to AVEE.

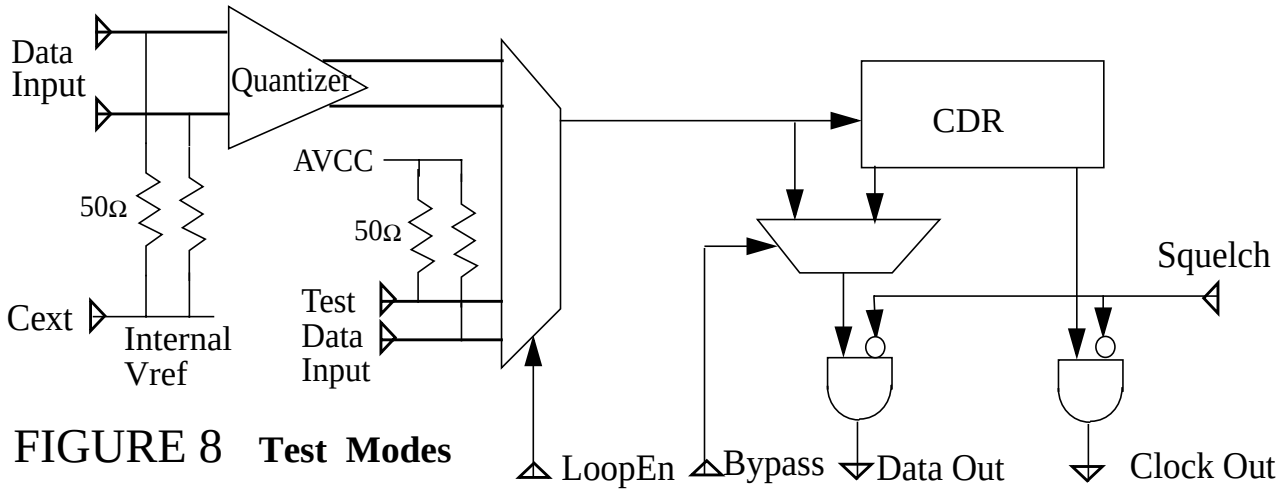
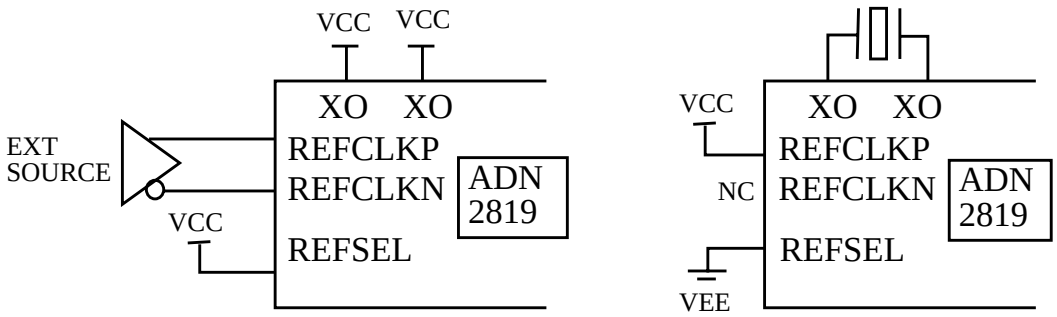


FIGURE 8 **Test Modes**

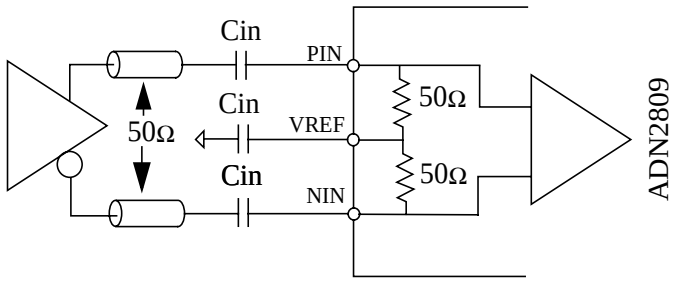
FIGURE 9 Reference Source



Configuration 1: External Reference Source

Configuration 2: Use of Crystal Oscillator

FIGURE 10 Data Input Terminations



Note:

The value of Cin required depends on the data rate, # Consecutive Identical Digits (CID) and amount of Patter Dependent Jitter (PDJ) which can be tolerated. e.g. for 1000 CID and <0.01UI pk-pk PDJ, 100nF is needed at OC48 and 1.6uF at OC3.

FIGURE 11 Recommended AC Output Termination

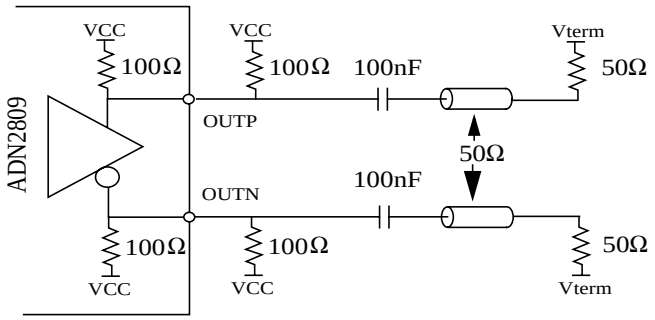


TABLE 1. Data Rate Selection

SEL2	SEL1	SEL0	Rate	Frequency
0	0	0	OC48	2.48832 GHz
0	0	1	Gigabit Ethernet	1.25 GHz
0	1	0	OC12	622.08 MHz
0	1	1	OC3	155.52 MHz
1	0	0	OC48 * 15/14	2.666 GHz
1	0	1	Gigabit Ethernet * 15/14	1.339 MHz
1	1	0	OC12 * 15/14	666.51 MHz
1	1	1	OC3 * 15/14	166.63 MHz

TABLE 2. Reference Frequency Selection

REFSEL1	REFSEL0	Applied Reference Frequency
0	0	19.44 MHz
0	1	38.88 MHz
1	0	77.76 MHz
1	1	155.52 MHz

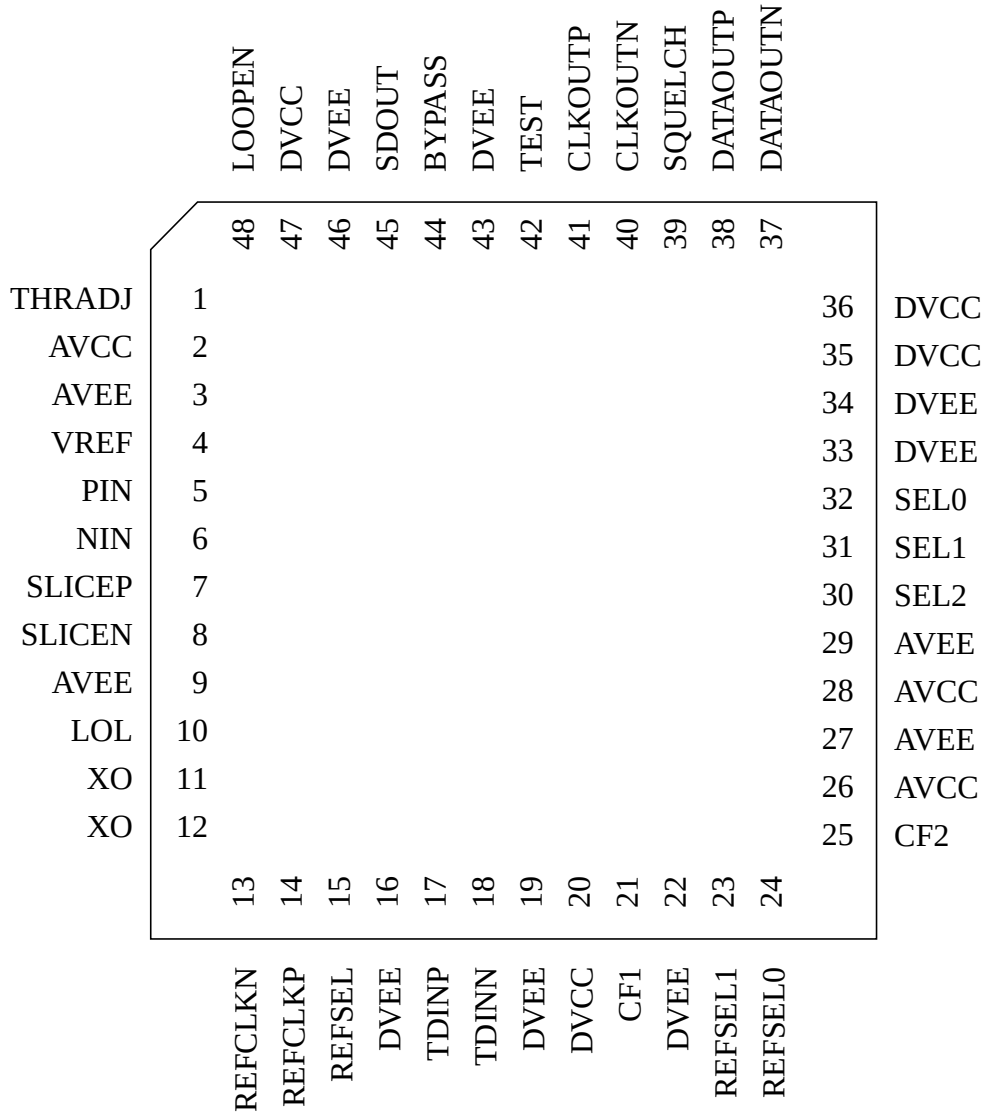
TABLE 3. Crystal Specification

Parameter	Value
Mode	Series Resonant
Frequency / Overall Stability	19.44 MHz / +/- 50 ppm
Frequency Accuracy	+/- 50 ppm/ total
Temp. Stability	
Ageing	
ESR	50 ohms max

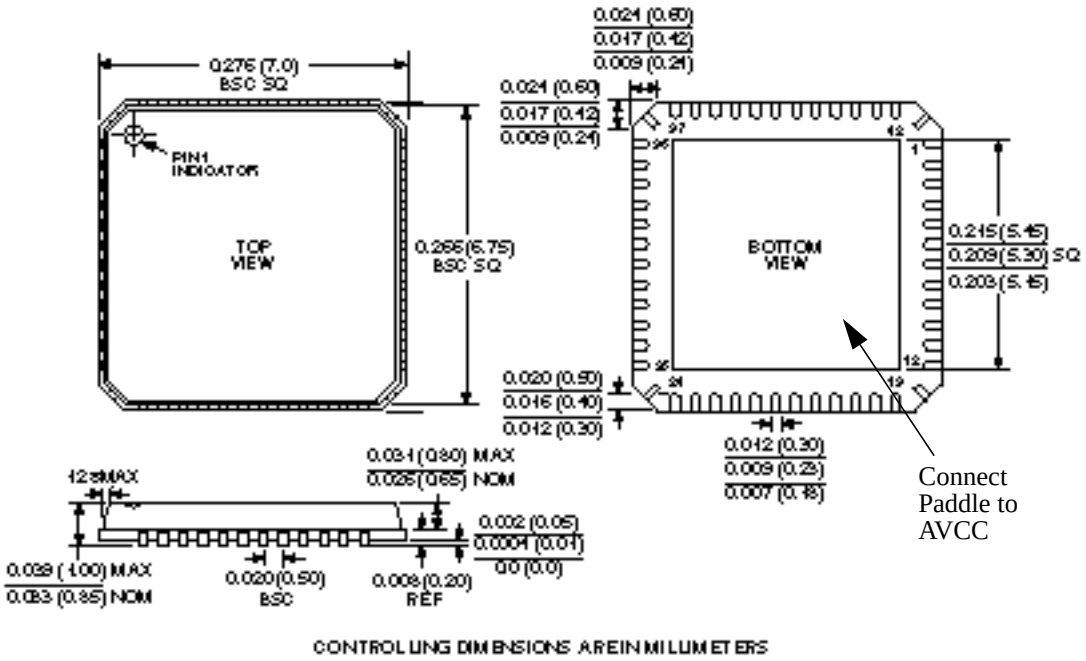
TABLE 4. Recommended Capacitor Specification

Parameter	Value
Capacitance (-40 to 85C)	>3.0uF
Leakage (-40C to 85C)	<80nA
Rating	>6.3V

Pinout


1 THRADJ
2 AVCC
3 AVEE
4 VREF
5 PIN
6 NIN
7 SLICEP
8 SLICEN
9 AVEE
10 LOL
11 XO
12 XO
13 REFCLKN
14 REFCLKP
15 REFSEL
16 DVEE
17 TDINP
18 TDINN
19 DVEE
20 DVCC
21 CF1
22 DVEE
23 REFSEL1
24 REFSEL0
25 CF2
26 AVCC
27 AVEE
28 AVCC
29 AVEE
30 SEL2
31 SEL1
32 SEL0
33 DVEE
34 DVEE
35 DVCC
36 DVCC
37 DATAOUTN
38 DATAOUTP
39 SQUELCH
40 CLKOUTN
41 CLKOUTP
42 TEST
43 DVEE
44 BYPASS
45 SDOUT
46 DVEE
47 DVCC
48 LOOPEN

Pin No.	Name	I/O	Level	Description
2,26,28, Exposed Pad	AVCC	P	3.3V	Analog power
3,9,27,29	AVEE	G	0V	Analog ground
16,19,22,33,34,43,46	DVEE	G	0V	Digital ground
20,35,36,47	DVCC	P	3.3V	Digital supply
1	THRADJ	I/O	Analog I/O	LOS threshold setting resistor
4	VREF	I/O	Analog I/O	Reference capacitor
5	PIN	I	Analog current	Differential data signal input
6	NIN	I	Analog current	Differential data signal input
7	SLICEP	I	Analog voltage	Slice level
8	SLICEN	I	Analog voltage	Slice level
10	LOL	O	LVTTL / LVCMOS	High level indicates loss of lock
11	XO	O	Analog output	Crystal oscillator
12	XO	O	Analog output	Crystal oscillator
13	REFCLKN	I	Any	Differential reference clock
14	REFCLKP	I	Any	Differential reference clock
15	REFSEL	I	LVTTL / LVCMOS	Reference source select
17	TDINP	I	CML	Differential test data input
18	TDINN	I	CML	Differential test data input
21	CF1	I/O	Analog I/O	Frequency loop capacitor
23	REFSEL1	I	LVTTL / LVCMOS	Reference rate select
24	REFSEL0	I	LVTTL / LVCMOS	Reference rate select
25	CF2	I/O	Analog I/O	Frequency loop capacitor
30	SEL2	I	LVTTL / LVCMOS	Data rate select
31	SEL1	I	LVTTL / LVCMOS	Data rate select
32	SEL0	I	LVTTL / LVCMOS	Data rate select
37	DATAOUTN	O	CML	Differential recovered data
38	DATAOUTP	O	CML	Differential recovered data
39	SQUELCH	I	LVTTL / LVCMOS	Disable clock and data outputs
40	CLKOUTN	O	CML	Differential retimed clock
41	CLKOUTP	O	CML	Differential retimed clock
42	TEST	I	LVTTL / LVCMOS	Test mode (Connect to AVEE)
44	BYPASS	I	LVTTL / LVCMOS	Disable clock and data recovery
45	SDOUT	O	LVTTL / LVCMOS	High level indicates loss of signal
48	LOOPEN	I	LVTTL / LVCMOS	Enable high speed test data inputs



ABSOLUTE MAXIMUM RATINGS

Supply Voltage.....+8 V
Input Voltage (pin x or pin xto Vcc).....TBD
Maximum Junction Temperature.....165 C
Storage Temperature Range.....-65C to +150C
Lead Temperature (Soldering 10 sec).....300C
ESD Rating (human body model).....TBD V
Notes:

Stresses greater than listed “Absolute Maximum Ratings” may damage the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.