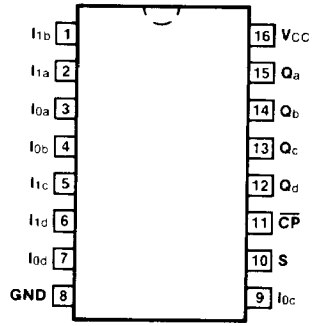
54/74298
54LS/74LS298

QUAD 2-PORT REGISTER
(Multiplexer with Storage)

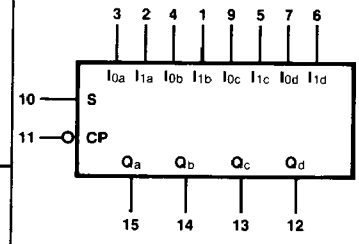
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

- **SELECT FROM TWO DATA SOURCES**
- **FULLY EDGE-TRIGGERED OPERATION**
- **TYPICAL POWER DISSIPATION OF 65 mW ('LS298)**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74298PC, 74LS298PC		9B
Ceramic DIP (D)	A	74298DC, 74LS298DC	54298DM, 54LS298DM	6B
Flatpak (F)	A	74298FC, 74LS298FC	54298FM, 54LS298FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
S	Common Select Input	1.0/1.0	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0	0.5/0.25
I0a — I0d	Source 0 Data Inputs	1.0/1.0	0.5/0.25
I1a — I1d	Source 1 Data Inputs	1.01/.0	0.5/0.25
Qa — Qd	Flip-flop Outputs	20/10	10/5.0 (2.5)

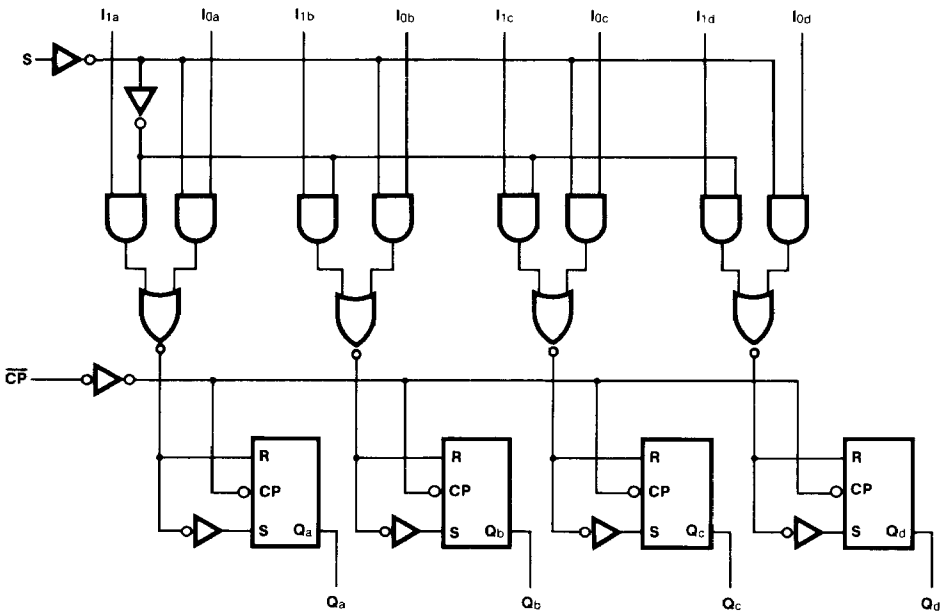
FUNCTIONAL DESCRIPTION — This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predicatable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_{0x}	I_{1x}	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS	UNITS	CONDITIONS
I_{CC}	Power Supply Current		65	21	mA	I_{0n}, I_{1n}, S = Gnd $\overline{CP}$ = ⊓_, V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		27 32		25 25	ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW S to $\overline{CP}$	25 25		25 25		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW S to $\overline{CP}$	0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW I_{0x} or I_{1x} to $\overline{CP}$	15 15		15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW I_{0x} or I_{1x} to $\overline{CP}$	5.0 5.0		5.0 5.0		ns	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width HIGH or LOW	20 20		20 20		ns	Fig. 3-9