

T-46-07-07

KS54HCTLS 76A Dual J-K Flip-Flops with Preset and Clear

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74HCTLS: -40°C to $+85^{\circ}\text{C}$
KS54HCTLS: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

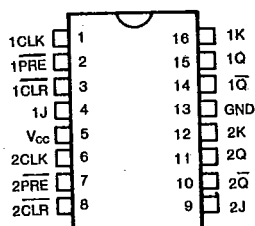
DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

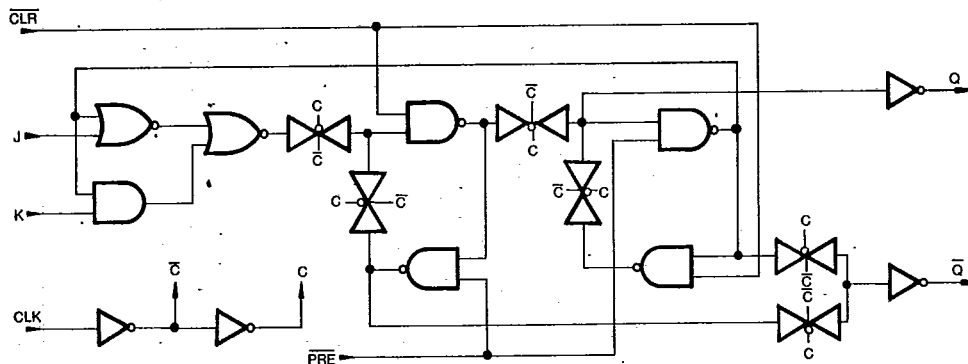


FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	\bar{L}
H	L	X	X	X	L	H
L	L	X	X	X	$H \cdot Q_0$	$H \cdot \bar{Q}_0$
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	\bar{Q}_0

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

LOGIC DIAGRAM



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KS74HCTLS

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{stg} ... -65°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} .. 0V to V_{CC}
 Operating Temperature

Range KS74HCTLS: -40°C to +85°C
 KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS76A

Characteristic	Symbol	Condition†	T _a = 25°C		KS74HCTLS		KS54HCTLS		Unit
			V _{CC} = 5.0V		T _a = -40°C to +85°C		T _a = -55°C to +125°C		
					V _{CC} = 5.0V ± 10%		V _{CC} = 5.0V ± 10%		
			Typ		Guaranteed Limits				
Maximum Clock Frequency	f _{max}		40	30	25	21			MHz
Maximum Propagation Delay, CLK to Q or \bar{Q}	t _{PLH}	C _L = 50pF	15	20	25	30			ns
	t _{PHL}		15	20	25	30			ns
Maximum Propagation Delay, PRE or CLR to Q or \bar{Q}	t _{PLH}		15	20	25	30			ns
	t _{PHL}		15	20	25	30			ns
Minimum Setup Time before CLK↓	Data	t _{su}	10	13	17	20			ns
	$\overline{\text{PRE}}$ or CLR Inactive		10	13	17	20			ns
Minimum Hold Time, J or K after CLK↓	t _h		-3	0	0	0			ns
Minimum Pulse Width	CLK High or Low	t _w	10	13	17	20			ns
	$\overline{\text{PRE}}$ or CLR Low		10	13	17	20			ns
Maximum Input Capacitance	C _{IN}		5						pF
Power Dissipation Capacitance*	C _{PD} (per flip-flop)		40						pF

* C_{PD} determines the no-load dynamic power dissipation: P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}.

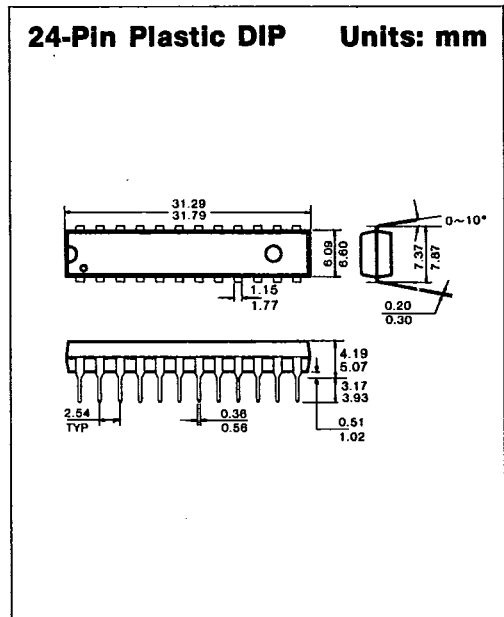
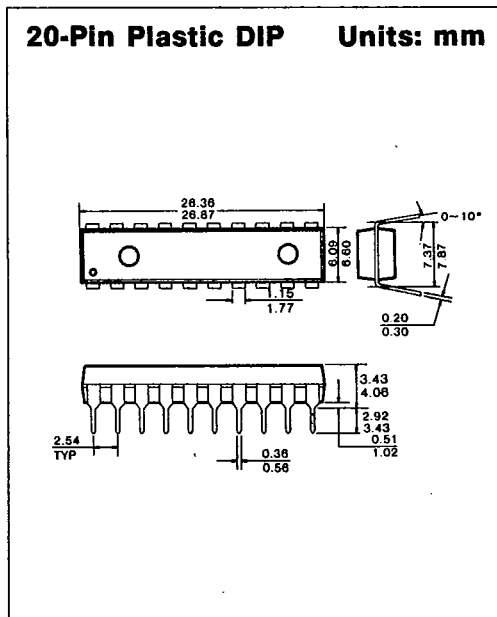
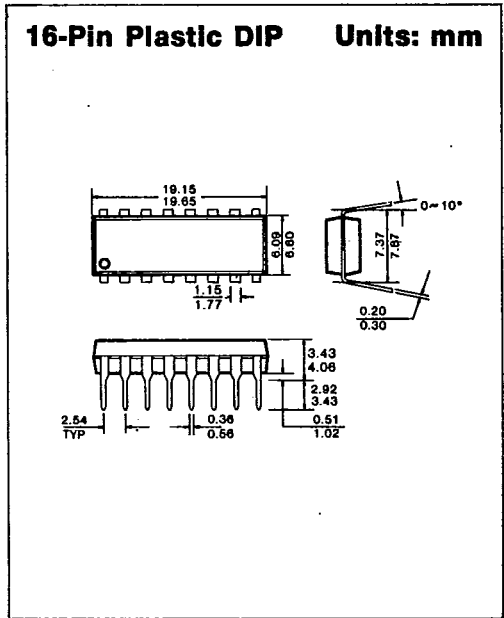
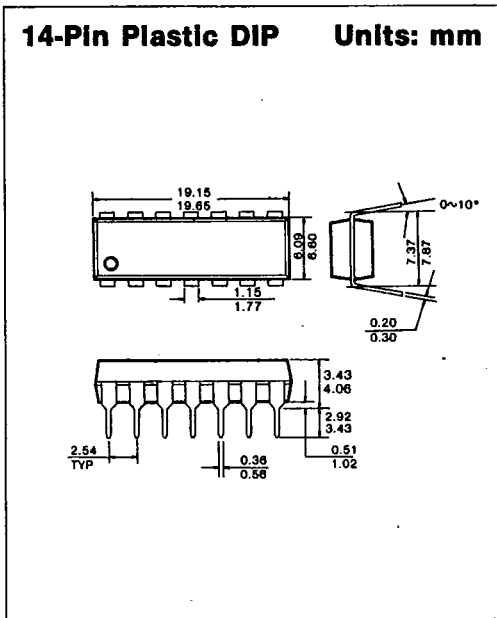
† For AC switching test circuits and timing waveforms see section 2.

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PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES



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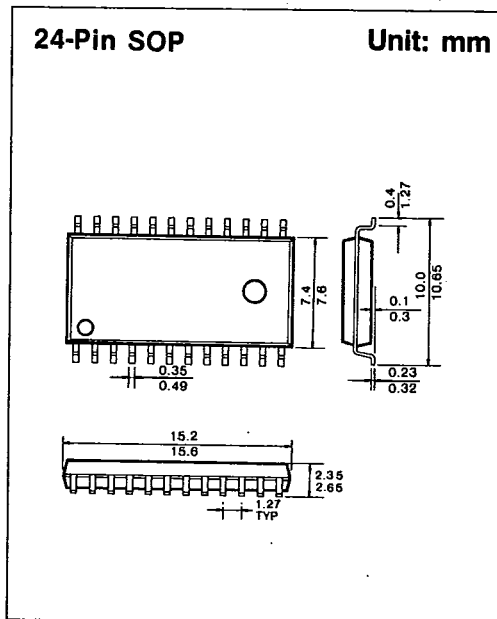
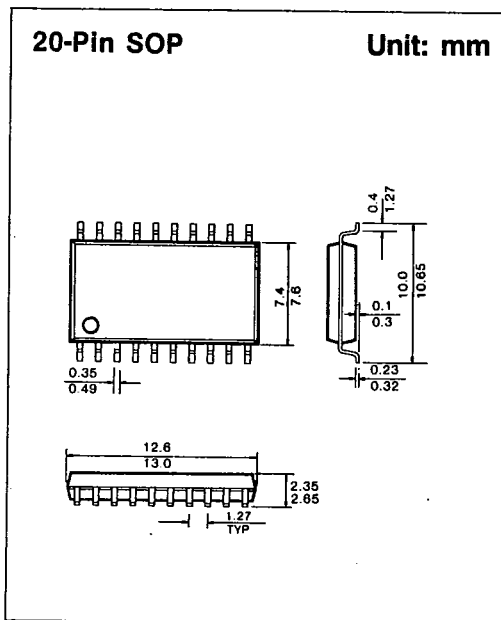
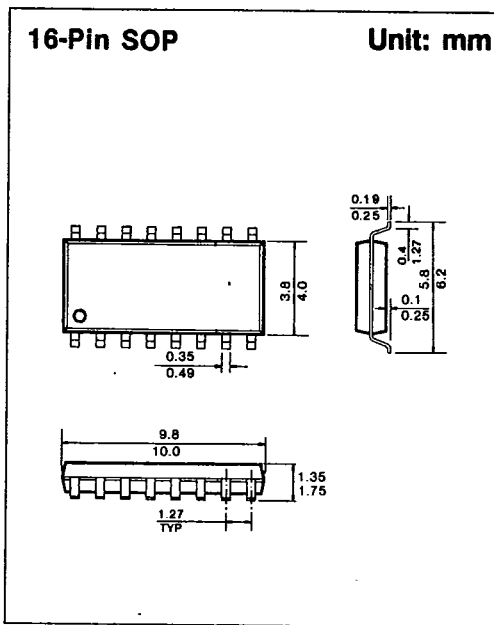
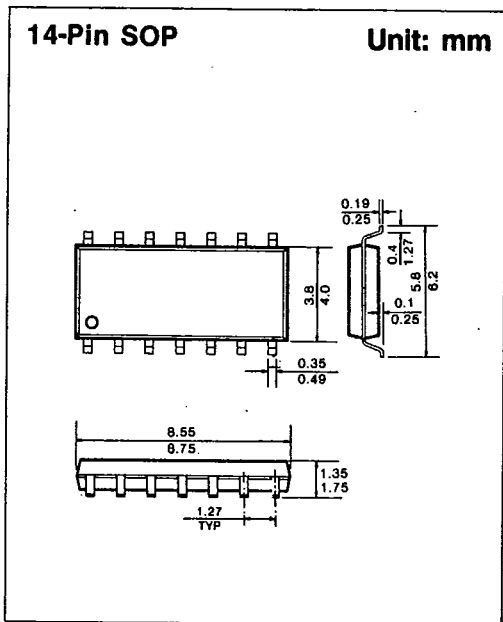
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PACKAGE DIMENSIONS

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PACKAGE DIMENSIONS

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2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.33
E	8.10	8.60
E ₁	7.77	7.95
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.776
S	1.85	1.93

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