19-2327; Rev 0; 1/02

MAXIM

LVTTL/TTL/CMOS-to-Differential LVECL/ECL Translators

General Description

The MAX9360/MAX9361 are low-skew, single LVTTL/TTL/CMOS-to-differential LVECL/ECL translators designed for high-speed signal and clock driver applications. For interfacing to LVTTL/TTL/CMOS input signals, these devices operate over a 3.0V to 5.5V supply range, allowing high-performance clock or data distribution. For interfacing to differential LVECL/ECL output signals, these devices operate from a -2.25V to -5.5V supply.

The MAX9360 is a 3.3V LVTTL/CMOS-to-LVECL/ECL translator that operates at a typical speed of 3GHz. The MAX9361 is a 5V TTL/CMOS-to-LVECL/ECL translator that operates at a typical speed of 1.3GHz. Both devices can be used to drive either LVECL devices or standard ECL devices with a negative supply range of -2.25V to -5.5V.

The devices default to high if the input is disconnected, and feature ultra-low propagation delay 440ps for the MAX9360, 810ps for the MAX9361.

The MAX9360 is specified for operation from -40°C to +85°C in an 8-pin SO package, and 0°C to +85°C in a space-saving, 8-pin SOT23 package.

The MAX9361 is specified for operation from -40°C to +85°C for both 8-pin SO and SOT23 packages.

Applications

Clock/Data-Level Translation

Features

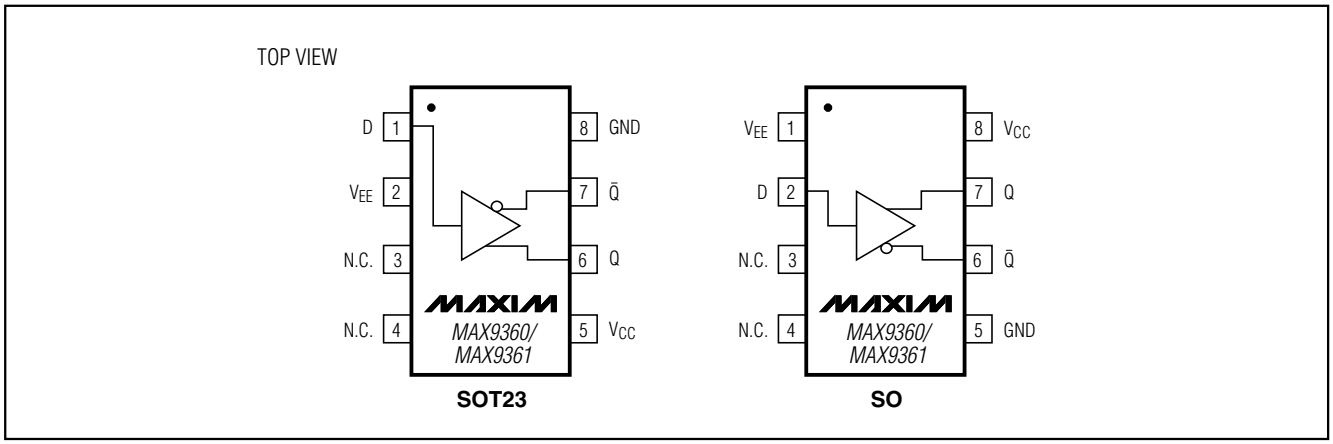
- **Output High with Input Open**
- **-2.25V to -5.5V LVECL/ECL Operation**
- **ESD Protection >2kV (Human Body Model)**
- **3.0V to 3.6V LVTTL/CMOS Operation (MAX9360)**
  - **Improved Second Source of the MC100EPT24**
  - **Low 13.8mA (typ) I_{EE} Supply Current**
  - **440ps (typ) Propagation Delay**
  - **>300mV Output at 1GHz**
- **4.5V to 5.5V TTL Operation (MAX9361)**
  - **Improved Second Source of the MC100ELT24**
  - **Low 6.6mA (typ) I_{EE} Supply Current**
  - **810ps (typ) Propagation Delay**
  - **>300mV Output at 250MHz**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9360UKA-T	0°C to +85°C	8 SOT23-8	AAJI
MAX9360ESA	-40°C to +85°C	8 SO	—
MAX9361EKA-T*	-40°C to +85°C	8 SOT23-8	AAJJ
MAX9361ESA*	-40°C to +85°C	8 SO	—

**Future product—contact factory for availability.*

Pin Configurations



LVTTL/TTL/CMOS-to-Differential LVECL/ECL Translators

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
V_{EE} to GND .....-6V to 0
D to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Output Current 50mA
Surge Output Current.....100mA
Junction-to-Ambient Thermal Resistance in Still Air
8-Pin SOT23.....+112°C/W
8-Pin SO.....+170°C/W
Junction-to-Ambient Thermal Resistance
with 500LFPM Airflow
8-Pin SOT23.....+78°C/W
8-Pin SO.....+99°C/W
Junction-to-Case Thermal Resistance
8-Pin SOT23.....+80°C/W
8-Pin SO.....+40°C/mW
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW
8-Pin SO (derate 5.9mW/°C above +70°C).....470mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
ESD Protection
Human Body Model (D, Q, $\overline{Q}$).....>2kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—MAX9360

(V_{CC} = 3.0V to 3.6V, V_{EE} = -2.25V to -5.5V, GND = 0, outputs terminated with 50Ω ±1% to -2.0V. Typical values are at V_{CC} = 3.3V, V_{IH} = 2.0V, V_{IL} = 0.8V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	0°C (SOT23) -40°C (SO)			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
LVTTL INPUT (D)												
Input High Current	I_{IH}	V_{IN} = 2.7V			-20			-20			-20	µA
		V_{IN} = V_{CC}			∓10			∓10			±10	
Input Low Current	I_{IL}	V_{IN} = 0.5V		-51	-200		-60	-200		-67	-200	µA
Input Clamp Voltage	V_{IK}	I_{IN} = -18mA			-1.2			-1.2			-1.2	V
Input High Voltage	V_{IH}		2.0	1.4		2.0	1.4		2.0	1.4		V
Input Low Voltage	V_{IL}				0.8		1.4	0.8			0.8	V
LVECL/ECL OUTPUTS (Q, $\overline{Q}$)												
Output High Voltage	V_{OH}		-1.145		-0.885	-1.145		-0.885	-1.145		-0.885	V
Output Low Voltage	V_{OL}		-1.935		-1.625	-1.935		-1.625	-1.935		-1.625	V
Differential Output Swing (V_{OH} - V_{OL})	V_{OH} - V_{OL}		550			550			550			mV
Power-Supply Current	I_{CC}	(Note 4)		4.3	7.0		5.0	7.0		5.6	7.0	mA
Internal Chip Current	I_{EE}	(Note 4)		12.3	20		13.8	20		15.2	20	mA

DC ELECTRICAL CHARACTERISTICS—MAX9361

(V_{CC} = 4.5V to 5.5V, V_{EE} = -2.25V to -5.5V, GND = 0, outputs terminated with 50Ω ±1% to -2.0V. Typical values are at V_{CC} = 5V, V_{IH} = 2.0V, V_{IL} = 0.8V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C (SO)			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TTL INPUT (D)												
Input High Current	I_{IH}	V_{IN} = 2.7V			-30			-30			-30	µA
		V_{IN} = V_{CC}			±10			±10			±10	
Input Low Current	I_{IL}	V_{IN} = 0.5V		-55	-200		-61	-200		-71	-200	µA
Input Clamp Voltage	V_{IK}	I_{IN} = -18mA			-1.2			-1.2			-1.2	V
Input High Voltage	V_{IH}		2.0			2.0			2.0			V
Input Low Voltage	V_{IL}				0.8			0.8			0.8	V
LVECL/ECL OUTPUTS (Q, $\overline{Q}$)												
Output High Voltage	V_{OH}		-1.025		-0.88	-1.025		-0.88	-1.025		-0.88	V
Output Low Voltage	V_{OL}		-1.83		-1.555	-1.81		-1.62	-1.81		-1.62	V
Differential Output Swing (V_{OH} - V_{OL})	V_{OH} - V_{OL}		550	640		550	689		550	695		mV
POWER SUPPLY												
Power-Supply Current	I_{CC}	(Note 4)		2.5	7.0		2.9	7.0		3.3	7.0	mA
Internal Chip Current	I_{EE}	(Note 4)		5.8	20		6.6	20		7.2	20	mA

LVTTL/TTL/CMOS-to-Differential LVECL/ECL Translators

AC ELECTRICAL CHARACTERISTICS—MAX9360

(V_{CC} = 3.0V to 3.6V, V_{EE} = -2.25V to -5.5V, GND = 0, outputs terminated with 50Ω ±1% to -2.0V, input frequency = 1.0GHz, input transition time = 125ps (20% to 80%). Typical values are at V_{CC} = 3.3V, V_{IH} = 2.0V, V_{IL} = 0.8V, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	0°C (SOT23) -40°C (SO)			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Toggle Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 300mV	1.0	3.0		1.0	3.0		1.0	3.0		GHz
		V_{OH} - V_{OL} ≥ 500mV	0.85	1.5		0.85	1.5		0.85	1.5		
Input-to-Output Propagation Delay	t_{PLHD}, t_{PHLD}	Figure 1	300		800	300		800	300		800	ps
Output Rise/Fall Time	t_R, t_F	Figure 1	70	97	150	80	105	150	100	122	150	ps
Added Deterministic Jitter (Note 6)	t_{DJ}	2Gbps 2^{23} - 1 PRBS pattern		43	70		43	70		43	70	$ps_{(P-P)}$
Added Random Jitter (Note 6)	t_{RJ}	1.0GHz clock pattern		1.4	3.0		1.5	3.0		1.5	3.0	$ps_{(RMS)}$

AC ELECTRICAL CHARACTERISTICS—MAX9361

(V_{CC} = 4.5V to 5.5V, V_{EE} = -2.25V to -5.5V, GND = 0, outputs terminated with 50Ω ±1% to -2.0V, input frequency = 100MHz, input transition time = 125ps (20% to 80%). Typical values are at V_{CC} = 5.0V, V_{IH} = 2.0V, V_{IL} = 0.8V, unless otherwise noted.) (Note 5)

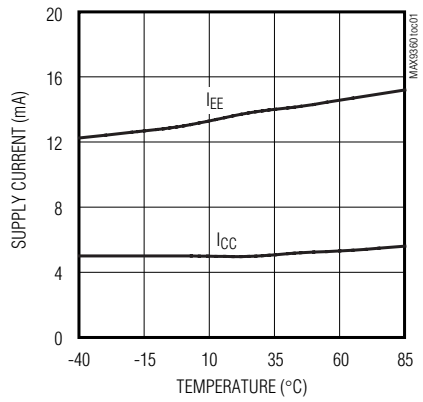
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Toggle Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 300mV	250	1300		250	1300		250	1300		MHz
		V_{OH} - V_{OL} ≥ 500mV	150	400		150	400		150	400		
Input-to-Output Propagation Delay	t_{PLHD}, t_{PHLD}	Figure 1	500	780	1000	600	810	1100	700	820	1200	ps
Output Rise/Fall Time	t_R, t_F	Figure 1	250	414	1000	250	428	1000	250	453	1000	ps
Added Deterministic Jitter (Note 6)	t_{DJ}	200Mbps 2^{23} - 1 PRBS pattern		46	100		46	100		49	100	$ps_{(P-P)}$
Added Random Jitter (Note 6)	t_{RJ}	100MHz clock pattern		2	10		3	10		3	10	$ps_{(RMS)}$

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterization over the full operating temperature range.
Note 4: All pins are open except V_{CC}, V_{EE}, and GND.
Note 5: Guaranteed by design and characterization. Limits are set to ±6 sigma.
Note 6: Device jitter added to the input signal.

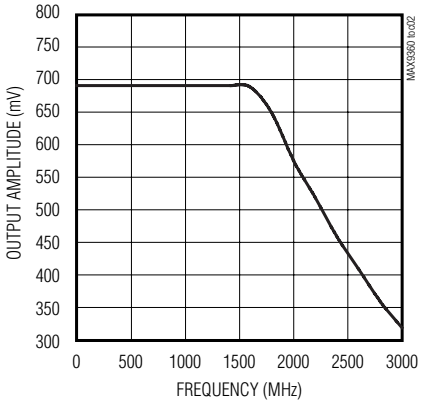
Typical Operating Characteristics

(MAX9360: V_{CC} = 3.3V and V_{EE} = -5V, V_{IH} = 2.0V, V_{IL} = 0.8V, T_A = +25°C, outputs terminated with 50Ω to -2V, input frequency = 1GHz, input transition time = 125ps (20% to 80%), unless otherwise noted.)

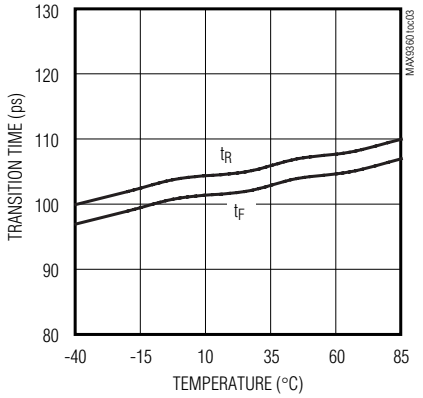
SUPPLY CURRENT vs. TEMPERATURE



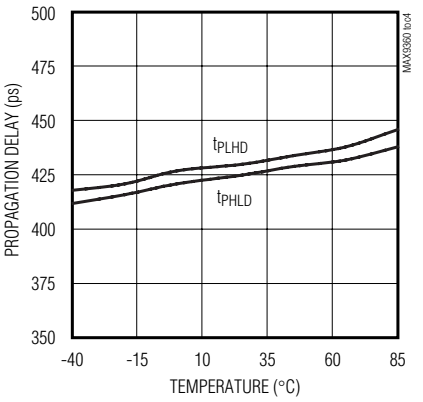
OUTPUT AMPLITUDE vs. FREQUENCY



TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



LVTTL/TTL/CMOS-to-Differential LVECL/ECL Translators

Pin Description

PIN		NAME	FUNCTION
SO	SOT23		
1	2	V_{EE}	Negative Supply Voltage. Bypass V_{EE} to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	1	D	LVTTL/CMOS Input for MAX9360. TTL/CMOS input for MAX9361.
3, 4	3, 4	N.C.	No Connect. Connect to GND.
5	8	GND	Ground
6	7	$\overline{Q}$	Inverting Differential LVECL/ECL Output. Typically terminate with 50Ω resistor to -2V.
7	6	Q	Noninverting Differential LVECL/ECL Output. Typically terminate with 50Ω resistor to -2V.
8	5	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

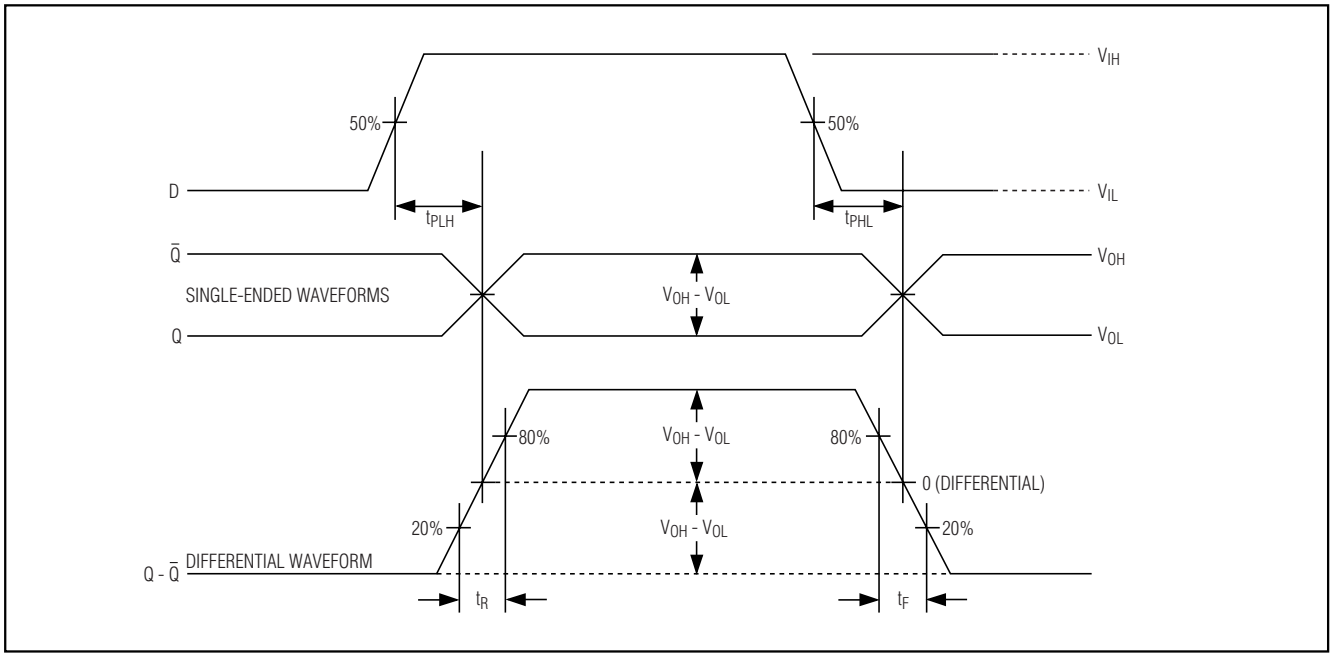


Figure 1. Input-to-Output Propagation Delay and Transition Timing Diagram

Detailed Description

The MAX9360/MAX9361 are low-skew, single LVTTL/CMOS/TTL-to-differential LVECL/ECL translators designed for high-speed signal and clock driver applications. For interfacing to LVTTL/TTL/CMOS input signals, these devices operate over a 3.0V to 5.5V supply range, allowing high-performance clock or data distribution in systems with a nominal 3.3V or 5.0V supply. For interfacing to differential LVECL/ECL output signals, these devices operate from a -2.25V to -5.5V supply.

The MAX9360 is a 3.3V LVTTL/CMOS-to-LVECL/ECL translator that operates at typical speeds of 3GHz. The MAX9361 is a 5V TTL/CMOS-to-LVECL/ECL translator that operates at typical speeds of 1.3GHz. Both devices can be used to drive either LVECL devices or standard ECL devices with a negative supply range of -2.25V to -5.5V.

Input

The MAX9360/MAX9361 inputs accept standard LVTTL/TTL/CMOS levels. The input has pullup circuitry that drives the outputs to a differential high if the inputs are open.

Differential Output

Output levels are referenced to GND and are considered ECL or LVECL, depending on the level of the V_{EE} supply. With GND connected to 0 and V_{EE} at -4.2V to -5.5V, the outputs are ECL. The outputs are LVECL when GND is connected to 0 and V_{EE} is at -2.25V to -3.8V.

Applications Information

Supply Bypassing

Bypass V_{CC} and V_{EE} to ground with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF value capacitor closest to the device. Use multiple parallel vias for low inductance.

Traces

Input and output trace characteristics affect the performance of the MAX9360/MAX9361. Connect each signal of a differential output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

On the MAX9360, if the input edge rate approaches the electrical length of the interconnect, then controlled-impedance transmission lines should be used for the input traces.

Output Termination

Terminate outputs through 50Ω to -2V or use an equivalent Thevenin termination. Terminate both outputs and use the same termination on each for the lowest output-to-output skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q is used as a single-ended output, terminate both Q and $\overline{Q}$.

Ensure that the output currents do not exceed the continuous safe output current limit or surge output current limit as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device's total thermal limits should be observed.

Chip Information

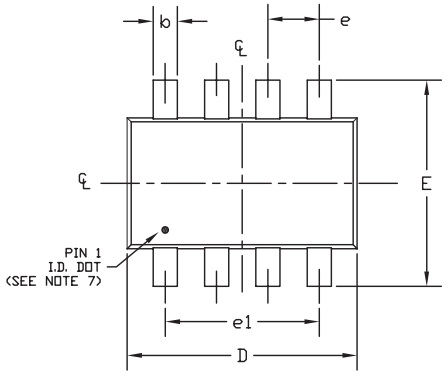
TRANSISTOR COUNT: 330

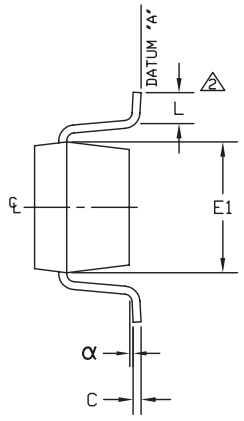
PROCESS: Bipolar

LVTTL/TTL/CMOS-to-Differential LVECL/ECL Translators

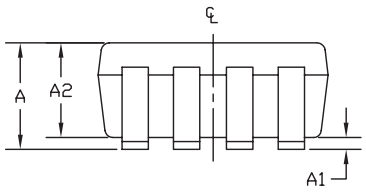
Package Information

SOT23, 8L.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.

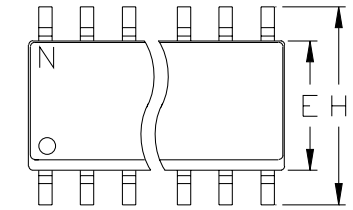
MAXIM
PROPRIETARY INFORMATION

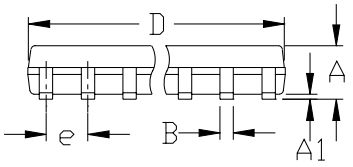
TITLE:
PACKAGE OUTLINE, SOT-23, 8L

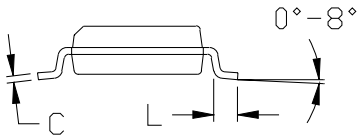
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	C	1/1

Package Information (continued)

SOICN.EPS







	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM	PACKAGE FAMILY OUTLINE: SOIC .150"	1/1	21-0041 A
120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION	TITLE		DOCUMENT CONTROL NUMBER REV