December 1999 FN2783.5

Two Dimensional Convolver

The Intersil HSP48908/883 is a high speed Two Dimensional Convolver which provides a single chip implementation of a video data rate 3 x 3 kernel convolution on two dimensional data. It eliminates the need for external data storage through the use of the on-chip row buffers which are programmable for row lengths up to 1024 pixels.

There are internal register banks for storing two independent 3 x 3 filter kernels, thus, facilitating the implementation of adaptive filters and multiple filter operations on the same data. The pixel data path also includes an on-chip ALU for performing real-time arithmetic and logical pixel point operations.

Data is provided to the HSP48908/883 in a raster scan noninterlaced fashion, and is internally buffered on images up to 1024 pixels wide for the 3 x 3 convolution operation. Images with larger rows and convolution with larger kernel sizes can be accommodated by using external row buffers and/or multiple HSP48908/883s. Coefficient and pixel input data are 8-bit signed or unsigned integers, and the 20-bit convolver output guarantees no overflow for kernel sizes up to 4 x 4. Larger kernel sizes can be implemented however, since the filter coefficients will normally be less than their maximum 8-bit values.

The HSP48908/883 is manufactured using an advanced CMOS process, and is a low power fully static design. The configuration of the device is controlled through a standard microprocessor interface and all inputs/outputs are TTL compatible.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Single Chip 3 x 3 Kernel Convolution
- Programmable On-Chip Row Buffers
- DC to 27MHz Clock Rate
- Cascadable for Larger Kernels and Images
- On-Chip 8-Bit ALU
- Dual Coefficient Mask Registers, Switchable in a Single Clock Cycle
- 8-Bit Signed or Unsigned Input and Coefficient Data
- 20-Bit Extended Precision Output
- Standard µP Interface

Applications

- Image Filtering
- Edge Detection
- Adaptive Filtering
- Real Time Video Filter

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HSP48908GM-20/883	-55 to 125	84 Ld CPGA	G84.A
HSP48908GM-27/883	-55 to 125	84 Ld CPGA	G84.A

Pinout

84 PIN PGA
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11	CASO6	DOUT0	DOUT1	GND	DOUT5	DOUT6	DOUT8	DOUT10	DOUT12	DOUT13	DOUT15
10	CASO4	CASO5	CASO7	DOUT2	DOUT4	DOUT9	GND	DOUT11	DOUT14	GND	DOUT17
9	CASO3	GND			DOUT3	DOUT7	V_{CC}			DOUT16	DOUT18
8	CASO1	CASO2								DOUT19	GND
7	$\overline{OE}$	GND	V_{CC}						CASI1	$\overline{FRAME}$	CASI0
6	DIN1	CASO0	DIN0						CASI2	V_{CC}	$\overline{RESET}$
5	DIN2	DIN3	DIN4						CASI5	CASI4	CASI3
4	DIN5	DIN6								CASI7	CASI6
3	DIN7	CIN1			CIN9	HOLD	$\overline{LD}$			CASI10	CASI8
2	CIN0	CIN3	CIN4	CIN7	GND	V_{CC}	A2	EALU	CASI13	CASI11	CASI9
1	CIN2	CIN5	CIN6	CIN8	CLK	A1	$\overline{CS}$	A0	CASI15	CASI14	CASI12

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC
Voltage Range . . . . . +4.5V to +5.5V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PGA Package	35.0	6.0

Maximum Package Power Dissipation at 125^oC
PGA Package. 1.45W
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 175^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Number of Transistors or Gates . . . . . 190,000 Transistors

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUP	TEMPERATURE (^oC)	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	0.8	V
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = 400mA, V_{CC} = 4.75V (Note 2)	1, 2, 3	$-55 \le T_A \le 125$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.5V (Note 2)	1, 2, 3	$-55 \le T_A \le 125$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open (Note 5)	1, 2, 3	$-55 \le T_A \le 125$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20.0MHz, V_{CC} = 5.5V Outputs Open, (Note 3, 5)	1, 2, 3	$-55 \le T_A \le 125$	-	160.0	mA
Functional Test	FT	(Notes 4, 5)	7, 8	$-55 \le T_A \le 125$	-	-	-

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating supply current is proportional to frequency, typical rating is 8.0mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \ge 1.5V$, $V_{OL} \le 1.5V$, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.
5. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Tested at: V_{CC} = 5.0V ±10%, T_A = -55°C to 125°C (Note 9)

PARAMETER	SYMBOL	NOTES	GROUP A SUBGROUP	TEMP (°C)	-27 (27MHz)		-20 (20MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	t_{CYCLE}		9, 10, 11	$-55 \le T_A \le 125$	37	-	50	-	ns
Clock Pulse Width High	t_{PWH}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
Clock Pulse Width Low	t_{PWL}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
Data Input Setup Time	t_{DS}		9, 10, 11	$-55 \le T_A \le 125$	16	-	17	-	ns
Data Input Hold Time	t_{DH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
Clock to Data Out	t_{OUT}		9, 10, 11	$-55 \le T_A \le 125$	-	19	-	28	ns
Address Setup Time	t_{AS}		9, 10, 11	$-55 \le T_A \le 125$	15	-	15	-	ns
Address Hold Time	t_{AH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
Configuration Data Setup Time	t_{CDS}		9, 10, 11	$-55 \le T_A \le 125$	17	-	20	-	ns
Configuration Data Hold Time	t_{CDH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
$\overline{LD}$ Pulse Width	t_{LPW}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
$\overline{LD}$ Setup Time	t_{LCS}	Note 6	9, 10, 11	$-55 \le T_A \le 125$	30	-	37	-	ns
CIN7-0 Setup to CLK	t_{CS}		9, 10, 11	$-55 \le T_A \le 125$	17	-	20	-	ns
CIN7-0 Hold to CLK	t_{CH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
$\overline{CS}$ Setup to $\overline{LD}$	t_{CSS}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
$\overline{CS}$ Setup to $\overline{LD}$	t_{CSH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
$\overline{RESET}$ Pulse Width	t_{RPW}		9, 10, 11	$-55 \le T_A \le 125$	37	-	50	-	ns
$\overline{FRAME}$ Setup to Clock	t_{FS}	Note 7	9, 10, 11	$-55 \le T_A \le 125$	25	-	30	-	ns
$\overline{FRAME}$ Pulse Width	t_{FPW}		9, 10, 11	$-55 \le T_A \le 125$	37	-	50	-	ns
EALU Setup Time	t_{ES}		9, 10, 11	$-55 \le T_A \le 125$	15	-	17	-	ns
EALU Hold Time	t_{EH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
HOLD Setup Time	t_{HS}		9, 10, 11	$-55 \le T_A \le 125$	13	-	14	-	ns
HOLD Hold Time	t_{HH}		9, 10, 11	$-55 \le T_A \le 125$	2	-	2	-	ns
Output Enable Time	t_{EN}	Note 8	9, 10, 11	$-55 \le T_A \le 125$	-	19	-	28	ns

NOTES:

6. This specification applies only to the case where the HSP48908/883 is being written to during an active convolution cycle. It must be met in order to achieve predictable results at the next rising clock edge. In most applications, the configuration data and coefficients are loaded asynchronously and the t_{LCS} Specification may be disregarded.
7. While $\overline{FRAME}$ is an asynchronous signal, it must be deasserted a minimum of t_{FS} ns prior to the rising clock edge which is to begin loading pixel data for a new frame.
8. Transition is measured at ±200mV from steady state voltage with loading as specified in test load circuit with C_L = 40pF.
9. AC Testing is performed as follows: Input levels (CLK input) 4.0V and 0V, input levels (all other inputs) 0V and 3.0V, timing reference levels (CLK) = 2.0V, (others) = 1.5V. Output load per test load circuit with C_L = 40pF. Output transition is measured at $V_{OH} \ge 1.5V$ and $V_{OL} \le 1.5V$.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMP (^oC)	-27		-20		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open f = 1MHz, all measurements are referenced to device GND	10	T_A = 25	-	10	-	10	pF
Output Capacitance	C_O	V_{CC} = Open f = 1MHz, all measurements are referenced to device GND	10	T_A = 25	-	12	-	12	pF
Output Disable Time	t_{OZ}		10, 11	$-55 \le T_A \le 125$	-	35	-	40	ns
Output Rise Time	t_r	From 0.8V to 2.0V	10, 11	$-55 \le T_A \le 125$	-	6	-	6	ns
Output Fall Time	t_f	From 2.0V to 0.8V	10, 11	$-55 \le T_A \le 125$	-	6	-	6	ns

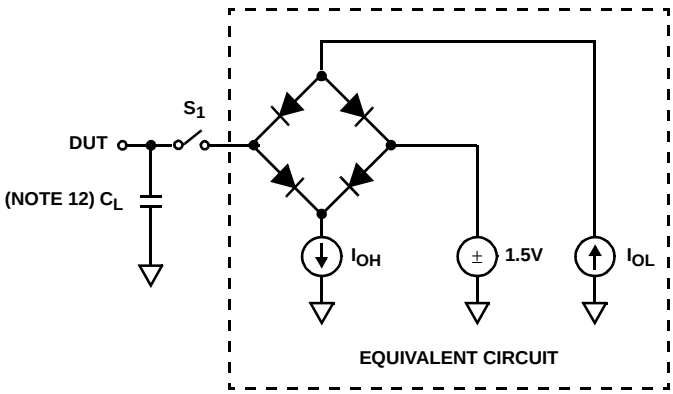
NOTES:

10. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
11. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Test Load Circuit



NOTES:

12. Includes stray and jig capacitance.
13. Switch S_1 Open for I_{CCSB} and I_{CCOP} Tests.

Burn-In Circuit

	A	B	C	D	E	F	G	H	J	K	L
11	CASO6	DOUT0	DOUT1	GND	DOUT5	DOUT6	DOUT8	DOUT10	DOUT12	DOUT13	DOUT15
10	CASO4	CASO5	CASO7	DOUT2	DOUT4	DOUT9	GND	DOUT11	DOUT14	GND	DOUT17
9	CASO3	GND			DOUT3	DOUT7	V_{CC}			DOUT16	DOUT18
8	CASO1	CASO2								DOUT19	GND
7	$\overline{OE}$	GND	V_{CC}						CASI1	$\overline{FRAME}$	CASI0
6	DIN1	CASOd	DIN0						CASI2	V_{CC}	$\overline{RESET}$
5	DIN2	DIN3	DIN4						CASI6	CASI14	CASI13
4	DIN5	DIN6								CASI7	CASI16
3	DIN7	CIN1			CIN9	HOLD	$\overline{LD}$			CASI10	CASI18
2	CIN0	CIN3	CIN4	CIN7	GND	V_{CC}	A2	EALU	CASI13	CASI11	CASI9
1	CIN2	CIN5	CIN6	CIN8	CLK	A1	$\overline{CS}$	A0	CASI15	CASI14	CASI12

PGA BURN-IN SCHEMATIC

PIN NAME	PGA PIN	BURN-IN SIGNAL	PIN NAME	PGA PIN	BURN-IN SIGNAL	PIN NAME	PGA PIN	BURN-IN SIGNAL
CIN2	A1	F13	POUT1	C11	$V_{CC}/2$	CASI.13	J2	F5
CIN0	A2	F12	CIN8	D1	F14	CASI.5	J5	F5
DIN7	A3	F7	CIN7	D2	F12	CASI.2	J6	F2
DIN5	A4	F5	POUT2	D10	$V_{CC}/2$	CASI.1	J7	F1
DIN2	A5	F2	GND	D11	GND	POUT14	J10	$V_{CC}/2$
DIN1	A6	F1	CLK	E1	F0	POUT12	J11	$V_{CC}/2$
OE	A7	F10	GND	E2	GND	CASI.14	K1	F6
CASO.1	A8	$V_{CC}/2$	CIN9	E3	F14	CASI.11	K2	F3
CASO.3	A9	$V_{CC}/2$	POUT3	E9	$V_{CC}/2$	CASI.10	K3	F2
CASO.4	A10	$V_{CC}/2$	POUT4	E10	$V_{CC}/2$	CASI.7	K4	F7
CASO.6	A11	$V_{CC}/2$	POUT5	E11	$V_{CC}/2$	CASI.4	K5	F4
CIN5	B1	F12	A1	F1	F13	V_{CC}	K6	V_{CC}
CIN3	B2	F13	V_{CC}	F2	V_{CC}	FRAME	K7	F15
CIN1	B3	F12	HOLD	F3	F14	POUT19	K8	$V_{CC}/2$
DIN6	B4	F6	POUT7	F9	$V_{CC}/2$	POUT16	K9	$V_{CC}/2$
DIN3	B5	F3	POUT9	F10	$V_{CC}/2$	GND	K10	GND
CASO.0	B6	$V_{CC}/2$	POUT6	F11	$V_{CC}/2$	POUT13	K11	$V_{CC}/2$
GND	B7	GND	CS	G1	F12	CASI.12	L1	F4
CASO.2	B8	$V_{CC}/2$	A2	G2	F14	CASI.9	L2	F1
GND	B9	GND	LOAD	G3	F11	CASI.8	L3	F0
CASO.5	B10	$V_{CC}/2$	V_{CC}	G9	V_{CC}	CASI.6	L4	F6
POUT0	B11	$V_{CC}/2$	GND	G10	GND	CASI.3	L5	F3
CIN6	C1	F13	POUT8	G11	$V_{CC}/2$	RESET	L6	F16
CIN4	C2	F13	A0	H1	F12	CASI.0	L7	F0
DIN4	C5	F4	EALU	H2	F8	GND	L8	GND
DIN0	C6	F0	POUT11	H10	$V_{CC}/2$	POUT18	L9	$V_{CC}/2$
V_{CC}	C7	V_{CC}	POUT10	H11	$V_{CC}/2$	POUT17	L10	$V_{CC}/2$
CASO.7	C10	$V_{CC}/2$	CASI.15	J1	F7	POUT15	L11	$V_{CC}/2$

NOTES:

14. $V_{CC}/2$ (2.7 ±10%) used for outputs only.
15. 47kΩ (±20%) resistor connected to all pins except V_{CC} and GND.
16. V_{CC} = 5.5 ±0.5V.
17. 0.1µF (minimum) capacitor between V_{CC} and GND per position.
18. F0 = 100kHz ±10%, F1 - F0/2, F2 = F1/2...F11 = F10/2, 40 - 60% duty cycle.
19. Input Voltage Limits: V_{IL} = 0.8V maximum, V_{IH} = 4.5V ±10%.

Die Characteristics

DIE DIMENSIONS:

341 mils x 322 mils x 19 mils ±1 mil

METALLIZATION:

Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

WORST CASE CURRENT DENSITY:

2×10^5 A/cm^2

GLASSIVATION:

Type: Nitrox
Thickness: 10kÅ

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