DDR5 SDRAM 3DS R-DIMM
Based on 16Gb M-die

HMCT04MEERAxxxN
HMCT14MEERAxxxN

*SK hynix reserves the right to change products or specifications without notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Sep.2020	
0.2	Updated JEDEC Specification	Dec.2020	
1.0	Updated IDD Specification	Aug.2021	

Description

SK hynix Registered DDR5 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

Features

- DRAM VDD/VDDQ = 1.1V (-33mV / +66mV)
- DRAM VPP = 1.8V (–54mV / +108mV)
- 32 Bank with x4/x8
- 16 Bank with x16
- 8 BG(Bank Group) for X4/X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Temperature Encoding
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Package Output Driver Test Mode
- Training Modes:
    - VrefDQ / VrefCA / VrefCS Training
    - Read Training Mode
    - CA Training Mode
    - CS Training Mode
    - Per Pin VREFDQ Training
    - Write Leveling Training Mode
    - Duty Cycle Adjuster (DCA) for Read - Global
    - Per Pin DCA(Duty Cycle Adjuster) for Read - Per Pin(DQ)

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks
HMCT04MEERAxxxN	128GB	16Gx80	TSV 2Hi 8Gx4(H5CG54MEEDXxxxN)*40	4
HMCT14MEERAxxxN	256GB	32Gx80	TSV 4Hi 16Gx4(H5CG64MEEDXxxxN)*40	8

Key Parameters

MT/s	Grade	tCK (ns)	tAA (ns)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR5-4800	-EE	0.416	18.75	16.000	16.000	32.00	48.000	46-39-39

Address Table

		128GB (4Rx4)	256GB (8Rx4)
Bank Address	**# of Bank Groups**	8	8
	BG Address	BG0~BG2	BG0~BG2
	Bank Address in a BG	BA0~BA1	BA0~BA1
Row Address		R0~R15	R0~R15
Column Address		C0~C9	C0~C9
Page size		1KB	1KB

DDR5 SDRAM DIMM Part Number Decoder

HMX XX X X XX X X XXX X

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

1-3) Product Mode & Type

HMC	DDR5 Module

4-5) Product Density

G6	8GB
G7	16GB
G8	32GB
G9	64GB
T0	128GB
T1	256GB
T2	512GB

6) Organization

4	X4
8	X8

7) Generation.

M	1st

8-9) Speed

EB	4800 40-39-39
EE	4800 46-39-39 (for 3DS)

10) Module Type

R	RDIMM (X80)
Q	RDIMM (X72)

11) Extra Info. (Die density, DIMM Profile, Temperatue)

A	16Gb, Low Profile, CT(0~95℃)

12-14) Serial Code

Code	RCD	DB	PMIC	Etc.
107	Montage Gen1.0	-	MPS 5010	-
109	Montage Gen1.0	-	MPS 5000	-
112	Rambus Gen1.0	-	Renesas(IDT) 5000	-
113	Renesas(IDT) Gen1.0	-	TI 5010	-
115	Renesas(IDT) Gen1.0	-	MPS 5010	-
116	Montage Gen1.0	-	TI 5010	-
121	Renesas(IDT) Gen1.0	-	TI 5000	-
123	Renesas(IDT) Gen1.0	-	MPS 5000	-
124	Montage Gen1.0	-	TI 5000	-
129	Renesas(IDT) Gen1.0	-	TI 5000	3DS 2Hi
131	Renesas(IDT) Gen1.0	-	MPS 5000	3DS 2Hi
133	Montage Gen1.0	-	TI 5000	3DS 2Hi
135	Montage Gen1.0	-	MPS 5000	3DS 2Hi
137	Rambus Gen1.0	-	Renesas(IDT) 5000	3DS 2Hi
146	Renesas(IDT) Gen1.0	-	TI 5000	3DS 4Hi
147	Renesas(IDT) Gen1.0		MPS 5000	3DS 4Hi
150	Montage Gen1.0	-	TI 5000	3DS 4Hi
152	Montage Gen1.0	-	MPS 5000	3DS 4Hi
154	Rambus Gen1.0	-	Renesas(IDT) 5000	3DS 4Hi
174	Rambus Gen1.0	-	Renesas(IDT) 5000	

15) Sales Type

N	Normal

※ Codes can be added, deleted or changed by internal management.

※ This decoder can be used only for understanding SK hynix's part number. It doesn't mean supportability for all kinds of products.

Pin Descriptions

Pin Name	Description	Pin Name	Description
CA0_A - CA6_A	Register command address input to channel A. (DDR)	CA0_B - CA6_B	Register command address input to channel B. (DDR)
CS0_A_n - CS1_A_n	DIMM Rank Select Lines input for channel A.	CS0_B_n - CS1_B_n	DIMM Rank Select Lines input for channel B.
DQ0_A - DQ31_A	DIMM memory data bus for channel A.	DQ0_B - DQ31_B	DIMM memory data bus for channel B.
CB0_A - CB7_A	DIMM ECC check bits for channel A.	CB0_B - CB7_B	DIMM ECC check bits for channel B.
TDQS0_A_t-TDQS9_A_t	Dummy loads for mixed populations of x4 based and x8 based RDIMMs in channel A. (positive line of differential pair)	TDQS0_B_t-TDQS9_B_t	Dummy loads for mixed populations of x4 based and x8 based RDIMMs in channel B. (positive line of differential pair)
TDQS0_A_c-TDQS9_A_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs in channel A. (negative line of differential pair)	TDQS0_B_c-TDQS9_B_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs in channel B. (negative line of differential pair)
DQS0_A_t - DQS9_A_t	Data Buffer data strobes in channel A.(positive line of differential pair)	DQS0_B_t - DQS9_B_t	Data Buffer data strobes in channel B.(positive line of differential pair)
DQS0_A_c - DQS9_A_c	Data Buffer data strobes in channel A.(negative line of differential pair)	DQS0_B_c - DQS9_B_c	Data Buffer data strobes in channel B.(negative line of differential pair)
PAR_A	Register parity input for channel A.	PAR_B	Register parity input for channel B.
RSP_A_n	Response signal for NVDIMM-P(channel A). Asynchronous, active-LOW, pulse-width modulated signal from DIMM to host indicating transactional/handshake signals such as when a read data packet is available, or when a status or error condition exists.	RSP_B_n	Response signal for NVDIMM-P(channel B). Asynchronous, active-LOW, pulse-width modulated signal from DIMM to host indicating transactional/handshake signals such as when a read data packet is available, or when a status or error condition exists.
VIN_BULK	12 V power input supply pin to the PMIC.	VSS	Power supply return (ground)
VIN_MGMT	3.3 V power input supply pin to the PMIC for VOUT_1.8V & VOUT_1.0V LDO output,side band management access, internal memory read operation.	PWR_GOOD / FAIL_n	Output for Power good indicator from the PMIC. The PMIC ensures this pin high when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. Otherwise PMIC will drive this pin low. The PMIC disables its output regulator when this pin is low
SCL	Side-band bus serial bus clock for SPD-Hub.	ALERT_n	Register ALERT_n output

Pin Name	Description	Pin Name	Description
SDA	Side-band bus serial data line for SPD-Hub.	RESET_n	Set Register and SDRAMs to a Known State
SAA	Side-band bus Host ID and Hub device type ID selection.	LBD	Loopback Data Inputs to register
CK_t	Register clock input (positive line of dif-ferential pair)	LBS	Loopback Strobe Inputs to register
CK_c	Register clocks input (negative line of differential pair)	RFU	Reserved for future use

Input/Output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA6_A, CA0_B - CA6_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins mat not be interchanged between devices on the same bus.
PAR_A PAR_B		
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB7_A, CB0_B - CB7_B	Input	DIMM ECC check bits
DQS0_A_t - DQS9_A_t DQS0_A_c - DQS9_A_c DQS0_B_t - DQS9_B_t DQS0_B_c - DQS9_B_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS0_A_c-DQS9_A_c, TDQS0_B_c-DQS9_B_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via MR5:OP[4]=0.
DM0_A_n-DM3_A_n, DM0_B_n-DM3_B_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
LBDQ	Output	Loopback Data Output: The Output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0]
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HIZ based on MR36:OP[2:0]

Symbol	Type	Function
ALERT_n	Input/ Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
SCL	Input	Host SidebandBus bus clock, supplied by the master.
SDA	Input/ Output	Host SidebandBus data, connected from the master to bubs or host bus client devices.
SAA	Input	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C Basic address range.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
PWR_GOOD	Input/ Output	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
VIN_MGMT	Supply	3.3V power input supply pin to the PMIC for VOUT_1.8V & VOUT_1.0V LDO output, side band management access, internal memory read operation. Vendor usage of 3.3V input supply may vary.
VIN_BULK	Supply	12V power input supply to the PMIC for analog circuits.
VSS	Supply	Ground

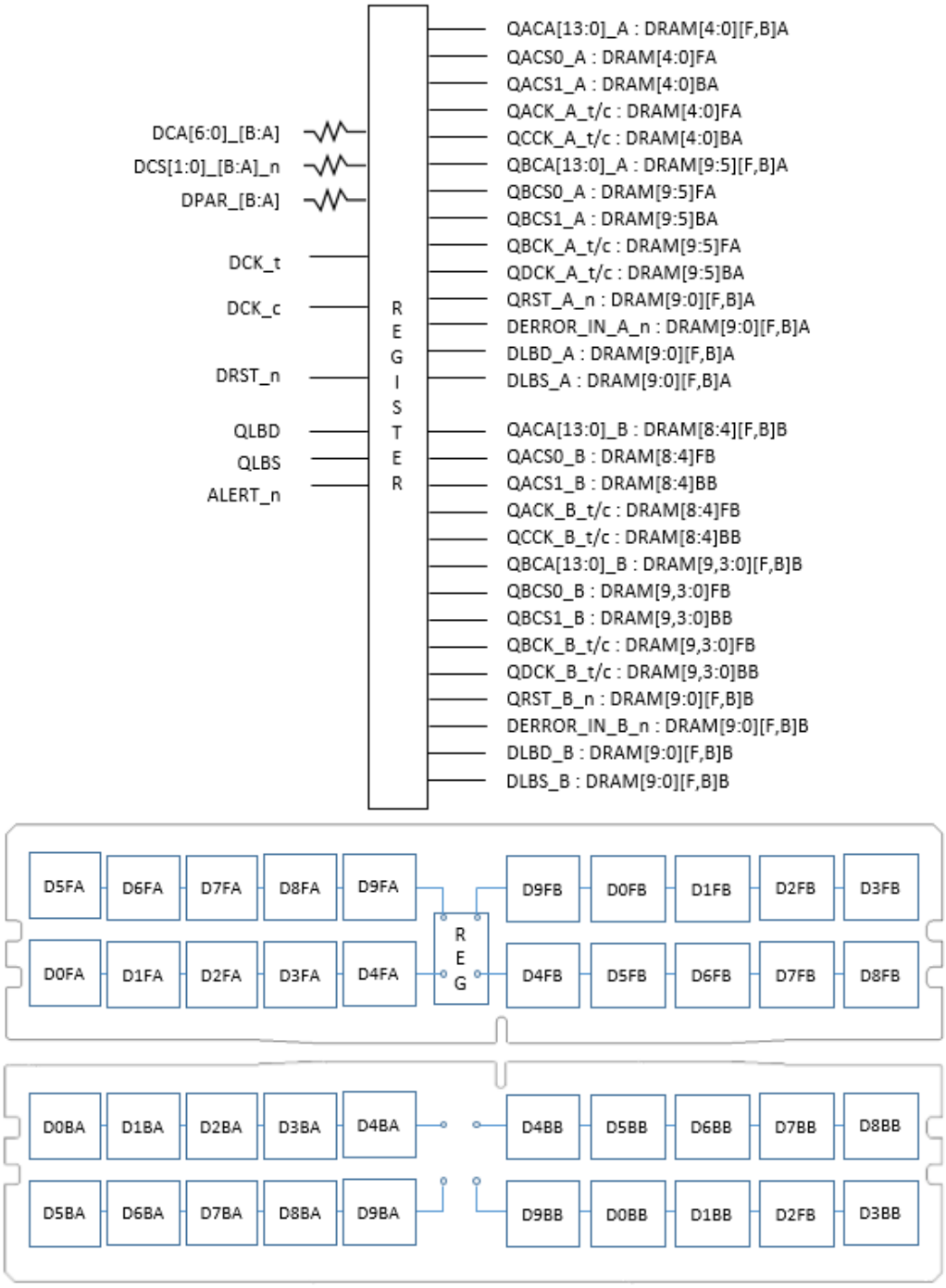
Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	VIN_BULK	145	VIN_BULK	74	PAR_A	218	CK_c
2	RFU	146	VIN_BULK	75	VSS	219	VSS
3	VIN_MGMT	147	PWR_GOOD /FAIL_n	KEY			
4	SCL	148	SAA				
5	SDA	149	RFU	76	CA0_B	220	RFU
6	VSS	150	RFU	77	VSS	221	CA1_B
7	DQ0_A	151	VSS	78	CA2_B	222	VSS
8	VSS	152	DQ2_A	79	VSS	223	CA3_B
9	DQ1_A	153	VSS	80	CA4_B	224	VSS
10	VSS	154	DQ3_A	81	VSS	225	CA5_B
11	DQS0_A_T	155	VSS	82	CA6_B	226	VSS
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	83	VSS	227	PAR_B
13	VSS	157	DQS5_A_T, TDQS5_A_T	84	CS0_B_n	228	VSS
14	DQ4_A	158	VSS	85	VSS	229	CS1_B_n
15	VSS	159	DQ6_A	86	LBD, RSP_A_n	230	VSS
16	DQ5_A	160	VSS	87	LBS, RSP_B_n	231	RFU
17	VSS	161	DQ7_A	88	VSS	232	RFU
18	DQ8_A	162	VSS	89	CB4_B	233	VSS
19	VSS	163	DQ10_A	90	VSS	234	CB6_B
20	DQ9_A	164	VSS	91	CB5_B	235	VSS
21	VSS	165	DQ11_A	92	VSS	236	CB7_B
22	DQS1_A_t	166	VSS	93	DQS9_B_t, TDQS9_B_t	237	VSS
23	DQS1_A_C	167	DQS6_A_c, TDQS6_A_c	94	DQS9_B_C, TDQS9_B_C	238	DQS4_B_c
24	VSS	168	DQS6_A_t, TDQS6_A_t	95	VSS	239	DQS4_B_t
25	DQ12_A	169	VSS	96	CB0_B	240	VSS
26	VSS	170	DQ14_A	97	VSS	241	CB2_B
27	DQ13_A	171	VSS	98	CB1_B	242	VSS
28	VSS	172	DQ15_A	99	VSS	243	CB3_B
29	DQ16_A	173	VSS	100	DQ0_B	244	VSS
30	VSS	174	DQ18_A	101	VSS	245	DQ2_B
31	DQ17_A	175	VSS	102	DQ1_B	246	VSS
32	VSS	176	DQ19_A	103	VSS	247	DQ3_B
33	DQS2_A_t	177	VSS	104	DQS0_B_t	248	VSS

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
34	DQS2_A_c	178	DQS7_A_C, TDQS7_A_C	105	DQS0_B_c	249	DQS5_B_C
35	VSS	179	DQS7_A_t, TDQS7_A_t	106	VSS	250	DQS5_B_t, TDQS5_B_t
36	DQ20_A	180	VSS	107	DQ4_B	251	VSS
37	VSS	181	DQ22_A	108	VSS	252	DQ6_B
38	DQ21_A	182	VSS	109	DQ5_B	253	VSS
39	VSS	183	DQ23_A	110	VSS	254	DQ7_B
40	DQ24_A	184	VSS	111	DQ8_B	255	VSS
41	VSS	185	DQ26_A	112	VSS	256	DQ10_B
42	DQ25_A	186	VSS	113	DQ9_B	257	VSS
43	VSS	187	DQ27_A	114	VSS	258	DQ11_B
44	DQS3_A_T	188	VSS	115	DQS1_B_T	259	VSS
45	DQS3_A_c	189	DQS8_A_c, TDQS8_A_c	116	DQS1_B_c	260	DQS6_B_c, TDQS6_B_c
46	VSS	190	DQS8_A_T, TDQS8_A_T	117	VSS	261	DQS6_B_T, TDQS6_B_T
47	DQ28_A	191	VSS	118	DQ12_B	262	VSS
48	VSS	192	DQ30_A	119	VSS	263	DQ14_B
49	DQ29_A	193	VSS	120	DQ13_B	264	VSS
50	VSS	194	DQ31_A	121	VSS	265	DQ15_B
51	CB0_A	195	VSS	122	DQ16_B	266	VSS
52	VSS	196	CB2_A	123	VSS	267	DQ18_B
53	CB1_A	197	VSS	124	DQ17_B	268	VSS
54	VSS	198	CB3_A	125	VSS	269	DQ19_B
55	DQS4_A_t	199	VSS	126	DQS2_B_t	270	VSS
56	DQS4_A_c	200	DQS9_A_c, TDQS9_A_c	127	DQS2_B_C	271	DQS7_B_c, TDQS7_B_c
57	VSS	201	DQS9_A_t, TDQS9_A_t	128	VSS	272	DQS7_B_t, TDQS7_B_t
58	CB4_A	202	VSS	129	DQ20_B	273	VSS
59	VSS	203	CB6_A	130	VSS	274	DQ22_B
60	CB5_A	204	VSS	131	DQ21_B	275	VSS
61	VSS	205	CB7_A	132	VSS	276	DQ23_B
62	ALERT_n	206	VSS	133	DQ24_B	277	VSS
63	VSS	207	RESET_n	134	VSS	278	DQ26_B
64	CS0_A_n	208	VSS	135	DQ25_B	279	VSS
65	VSS	209	CS1_A_n	136	VSS	280	DQ27_B
66	CA0_A	210	VSS	137	DQS3_B_t	281	VSS
67	VSS	211	CA1_A	138	DQS3_B_c	282	DQS8_B_c, TDQS8_B_c
68	CA2_A	212	VSS	139	VSS	283	DQS8_B_t, TDQS8_B_t

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
69	VSS	213	CA3_A	140	DQ28_B	284	VSS
70	CA4_A	214	VSS	141	VSS	285	DQ30_B
71	VSS	215	CA5_A	142	DQ29_B	286	VSS
72	CA6_A	216	VSS	143	VSS	287	DQ31_B
73	VSS	217	CK_t	144	RFU	288	VSS

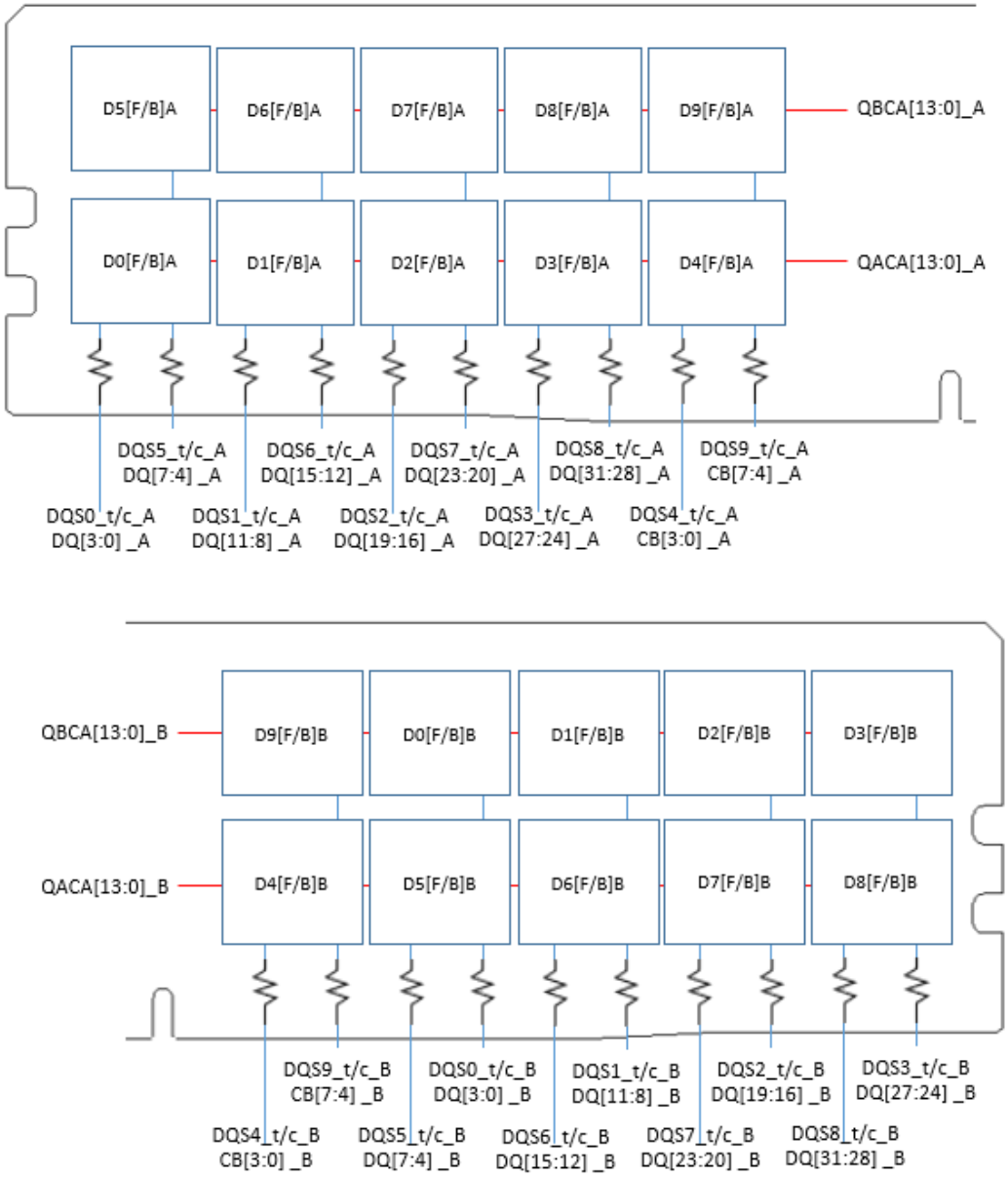
128GB 16Gx80 Module (2Rank of x4) RDIMM - page1



Note :

1. Unless otherwise noted resistors are 15 Ω±5 %.

128GB 16Gx80 Module (2Rank of x4) RDIMM - page2



Note :

1. Unless otherwise noted, resistor values are 15 Ω ±5%.
2. Each DRAM ZQ Pin need to be connected with a separate resistor, 240 Ω ±1%.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note(s):
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times. When VDD and VDDQ are less than 500 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5.Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

AC & DC Operating Conditions

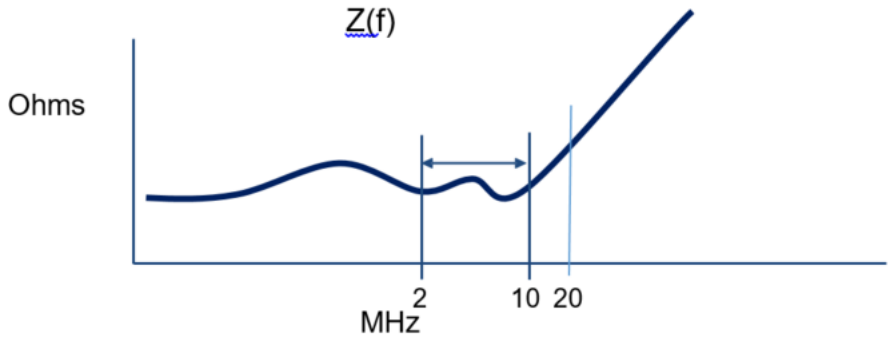
Recommended DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz		Notes
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhm	20	mOhm	3

Note(s):

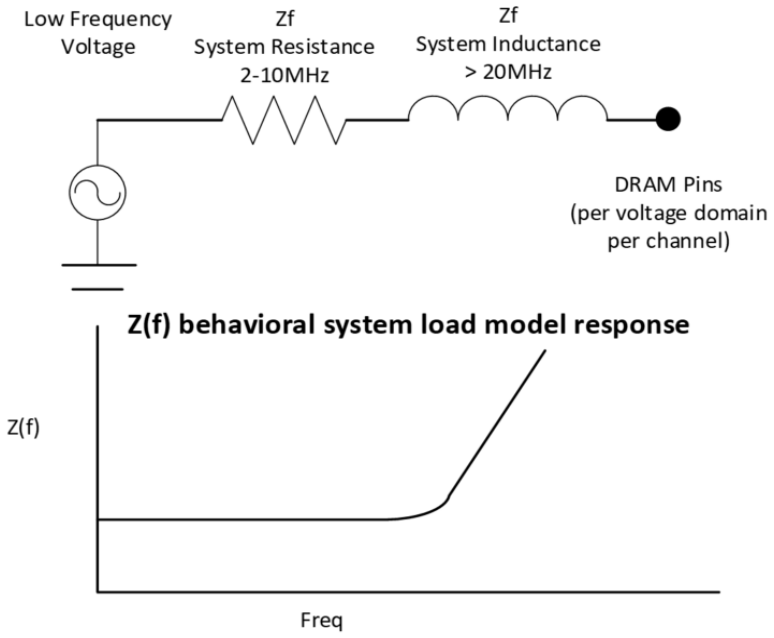
1. VDD must be within 66mv of VDDQ
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.
4. Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die.

Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component)



Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component)

A simplified electrical system load model for Z(F) with the general frequency response is shown in the figure below. The resistance and inductance can be scaled to generalize the spec response to the DRAM pin.



Simplified Z(f) electrical model and frequency response of PDN at the DRAM pin without the DRAM component

1. AC & DC Input Measurement Levels

1.1 Overshoot and Undershoot specifications for CAC - No Ballot

1.2 CA Rx voltage and timings

Note: The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

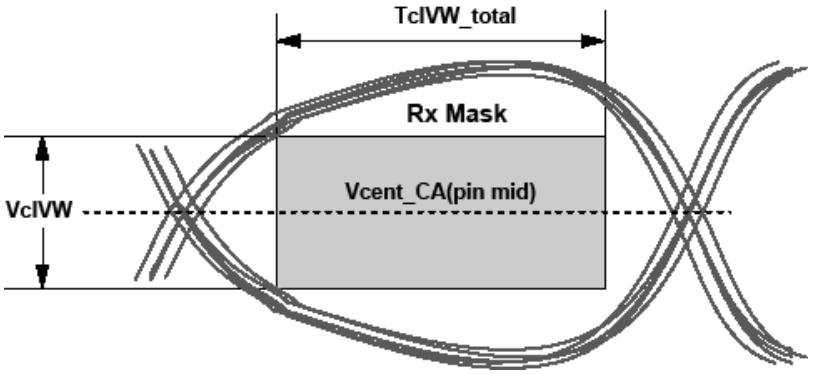


Figure 1 — CA Receiver (Rx) mask

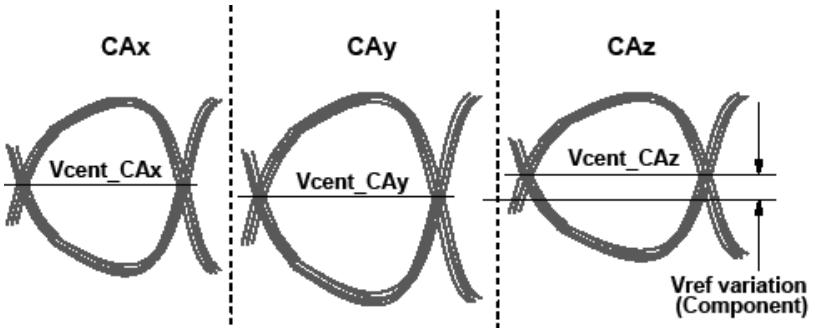


Figure 2 — Across pin V_{REF}CA voltage variation

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 3. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.

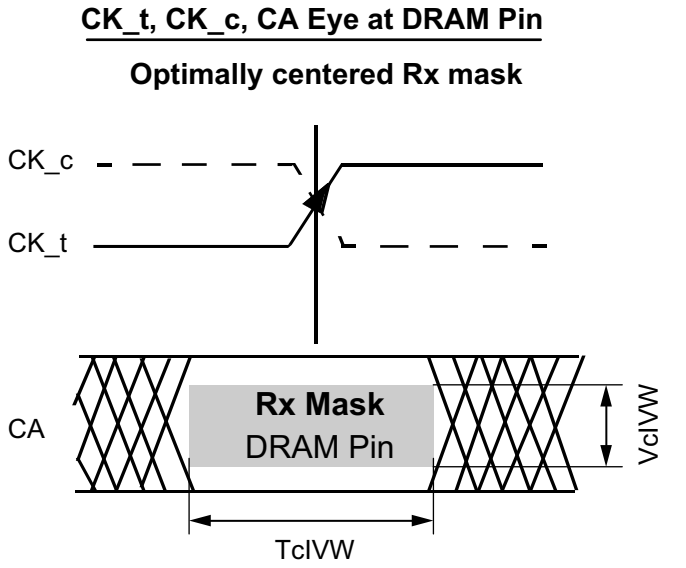
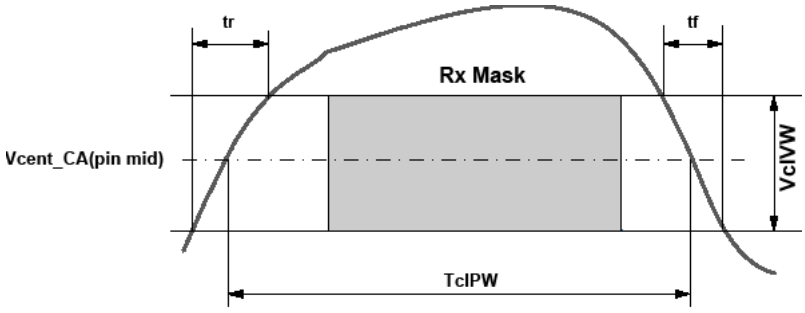


Figure 3 — CA Timings at the DRAM Pins

All of the timing terms in figure 3 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).



Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 4 — CA TcIPW and SRIN_cIVW definition (for each input pulse)

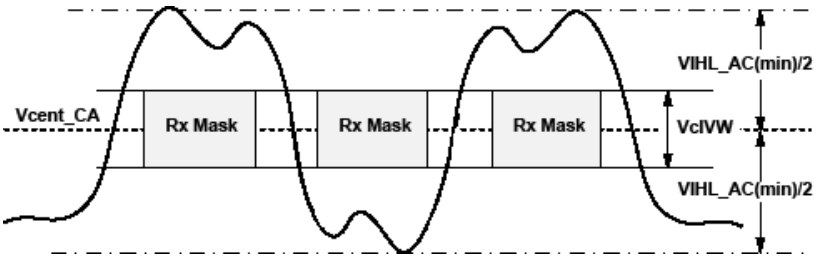


Figure 5 — CA VIHL_AC definition (for each input pulse)

Table 1 — DRAM CA, CS Parametric values for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	140	-	140	-	140	-	130	-	130	mV	1,2,4
Rx Timing Window	TcIVW	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	UI*	1,2,3,4, 8
CA Input Pulse Amplitude	VIHL_AC	-	160	-	160	-	160	-	150	-	150	mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		UI*	5,8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	V/ns	6

Note(s):

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.
8. *** UI=tCK(avg)min**

1.3 tREFI and tRFC parameters

The maximum average refresh interval (tREFI) requirement for the DDR5 SDRAM depends on the refresh mode setting (Normal or FGR), and the device's case temperature (Tcase). When the refresh mode is set to Normal Refresh mode, REFab commands are issued (tRFC1), and Tcase<=85°C, the maximum average refresh interval (tREFI1) is tREFI. When the refresh mode is set to FGR mode, REFab commands are issued (tRFC2) and Tcase<=85°C, the maximum average refresh interval (tREFI2) is tREFI/2. This same tREFI/2 interval value is also appropriate if the refresh mode is set to Normal Refresh mode and REFab commands are issued (tRFC1) but 85°C<Tcase<=95°C. Finally, if the refresh mode is set to FGR mode, REFab commands are issued (tRFC2), and 85°C<Tcase<=95°C, the maximum average refresh interval (tREFI2) is tREFI/4.

The DDR5 SDRAM includes an optional method for the host to indicate when Refresh commands are being issued at the 2x (tREFI2) refresh interval rate. The 2x Refresh Interval Rate indicator (MR4:OP[3]) alerts the DRAM if the host supports the refresh interval rate indication as part of the REF command using CA8. If enabled (MR4:OP[3]=1), the host will issue 1x REF commands with CA8=H (Tcase<=85°C), and the host will issue 2x REF commands with CA8=L (Tcase any allowable temperature). MR4:OP[3] is a Status Read/Write "SR/W" MR bit which shows DDR5 SDRAM support of this optional feature. Reading MR4:OP[3] will return a "1" if the 2x Refresh Interval Rate indicator is supported. A "0" will be returned if not supported.
tREFI is based on the 8,192 refresh commands that need to be issued within the baseline tREF=32ms refresh period on the DDR5 SDRAM.

1.3.1 tREFI and tRFC parameters for 3DS devices

Typical platforms are designed with the assumption that no more than one physical rank is refreshed at the same time. In order to limit the maximum refresh current (I_{DD5B1}) for a 3D stacked SDRAM, it will be required to stagger the refresh commands to each logical rank in a stack.

The tRFC time for a single logical rank is defined as tRFC_slr and is specified as the same value as for a monolithic DDR5 SDRAM of equivalent density. The minimum amount of stagger between refresh commands sent to different logical ranks (tRFC_dlr) or physical ranks (tRFC_dpr) is specified to be approximately tRFC_slr/3 - Table 4.

Table 2 — tREFI parameters for REFab and REFsb Commands (including 3DS)

Command	Refresh Mode	Symbol & Range		Expression	Value	Unit	Notes
REFab	Normal	tREFI1	0°C <= TCASE <= 85°C	tREFI	3.9	us	1,2
			85°C < TCASE <= 95°C	tREFI/2	1.95	us	1,2
REFab	Fine Granularity	tREFI2	0°C <= TCASE <= 85°C	tREFI/2	1.95	us	1,2
			85°C < TCASE <= 95°C	tREFI/4	0.975	us	1,2
REFsb	Fine Granularity	tREFIsb	0°C <= TCASE <= 85°C	tREFI/(2*n)	1.95/n	us	1,2,3
			85°C < TCASE <= 95°C	tREFI/(4*n)	0.975/n	us	1,2,3

Note(s):

1 - All 3D Stacked (3DS) devices follow the same requirements as the monolith die regardless of logical rank.

2 - 3DS specification covers up to 16Gb density. Future densities such as 24Gb or 32Gb could require different tREFI requirements.

3 - *n* is the number of banks in a bank group (e.g. 8G: n=2; 16G: n=4).

Table 3 — tRFC parameters by device density

Refresh Operation	Symbol	16Gb	Units	Notes
Normal Refresh (REFab)	tRFC1(min)	295	ns	
Fine Granularity Refresh (REFab)	tRFC2(min)	160	ns	
Same Bank Refresh (REFsb)	tRFCsb(min)	130	ns	

Table 4 — 3DS tRFC parameters by logical rank density

Refresh Operation	Symbol	8Gb	16Gb	24Gb	32Gb	Units	Notes
Normal Refresh with 3DS same logical rank	tRFC1_slr(min)	tRFC1(min)				ns	1
Fine Granularity Refresh with 3DS same logical rank	tRFC2_slr(min)	tRFC2(min)				ns	1
Same Bank Refresh with 3DS same logical rank	tRFCsb_slr(min)	tRFCsb(min)				ns	1
Normal Refresh with 3DS different logical rank	tRFC1_dlr(min)	tRFC1(min)/3				ns	3
Normal Refresh with 3DS different physical rank	tRFC1_dpr(min)	tRFC1min/3				ns	2, 3
Fine Granularity Refresh with 3DS different logical rank	tRFC2_dlr(min)	tRFC2(min)/3				ns	3
Fine Granularity Refresh with 3DS different physical rank	tRFC2_dpr(min)	tRFC2min/3				ns	2, 3
Same Bank Refresh with 3DS different logical rank	tRFCsb_dlr(min)	tRFCsb(min)/3				ns	3

Note(s):

1. All 3D Stacked (3DS) devices follow the same requirements as the monolith die for same logical ranks
2. Parameter applies to dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JESD301-1 “PMIC 50x0 Specification”, but may not apply to DIMMs built with higher current capacity PMICs.
3. 3DS tRFC parameters are to be rounded up to the nearest 1ns after the “tRFC*min”/3 calculation.

Table 5 — Same Bank Refresh parameters

Refresh Mode	Symbol	16Gb	Units
Same Bank Refresh to ACT delay	tREFSBRD(min)	30	ns

Table 6 — Same Bank Refresh parameters for 3DS 2H, 4H

Refresh Mode	Symbol	16Gb	Units
Same Bank Refresh to ACT delay SLR	tREFSBRD_slr(min)	30	ns
Same Bank Refresh to ACT delay DLR	tREFSBRD_dlr(min)	15	ns

1.4 Input Clock Jitter Specification

1.4.1 Overview

The clock is being driven to the DRAM either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules (**Figure 6**).

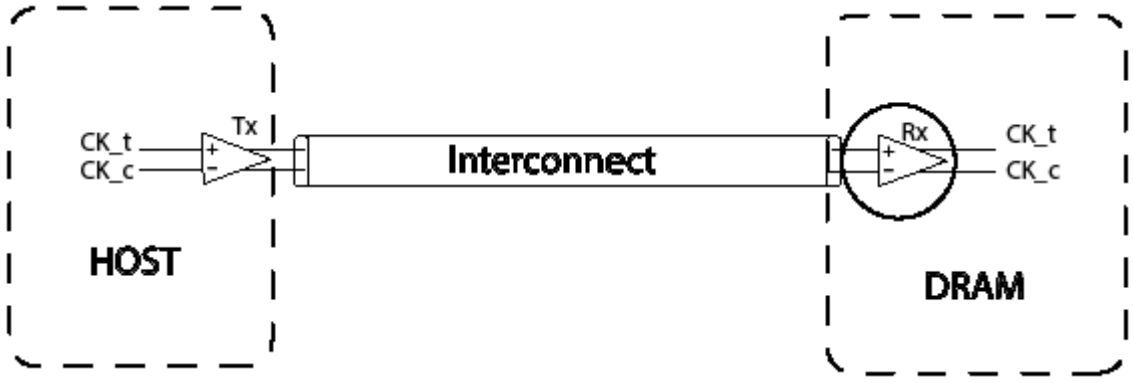


Figure 6 — HOST driving clock signals to the DRAM

1.4.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

Table 7 — DRAM Input Clock Jitter Specifications for DDR5-3200 to 4400

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	tCK	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	0.9999 * f0	1.0001 * f0	MHz	1,11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.05	-	0.05	-	0.05	-	0.05		0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0037	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.030	-	0.030	-	0.030	-	0.030	-	0.030	UI	3,6,11
Tj value of 1-UI Jitter	tCK_1UI_Tj_NoBUJ	-	0.090	-	0.090	-	0.090	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.0040	-	0.0040	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.074	-	0.074	-	0.074	-	0.074	-	0.074	UI	3,7,11
Tj value of N-UI Jitter, where N=2,3	tCK_NUI_Tj_NoBUJ, where N=2,3	-	0.140	-	0.140	-	0.140	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI	3,10,11,12
Tj value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI	3,10,11,12

Note(s):

1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600
2. Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

1.5 Differential Input Clock (CK_t, CK_c) Cross Point Voltage (VIX)

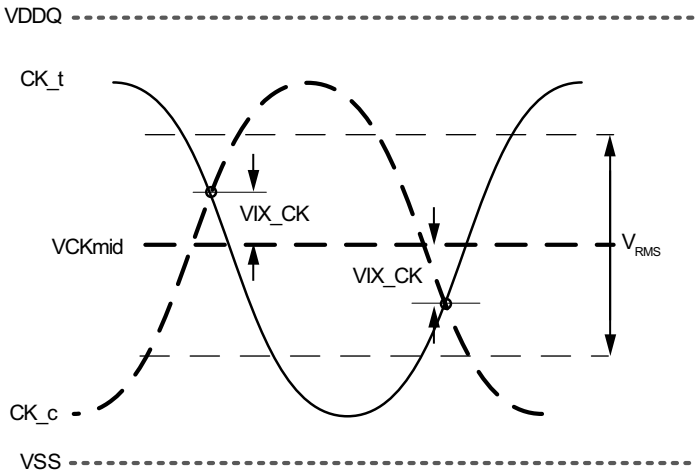


Figure 139 - VIX Definition (CK)

Table 8 — Crosspoint Voltage (VIX) for Differential Input Clock

Parameter	Symbol	DDR5-3200 - 4800		Unit	Notes
		Min	Max		
Clock differential input crosspoint voltage ratio	VIX_CK_Ratio	-	50	%	1,2,3

Note(s):
1. The VIX_CK voltage is referenced to VCKmid(mean) = (CK_t voltage + CK_c voltage) /2, where the mean is over 8 UI
2. VIX_CK_Ratio = (|VIX_CK| / |V_{RMS}|)*100%, where V_{RMS} = RMS(CK_t voltage - CK_c voltage)
3. Only applies when both CK_t and CK_c are transitioning

1.6 Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the Rx voltage sensitivity requirement. The system input swing to the DRAM must be larger than the DRAM Rx at the specified BER

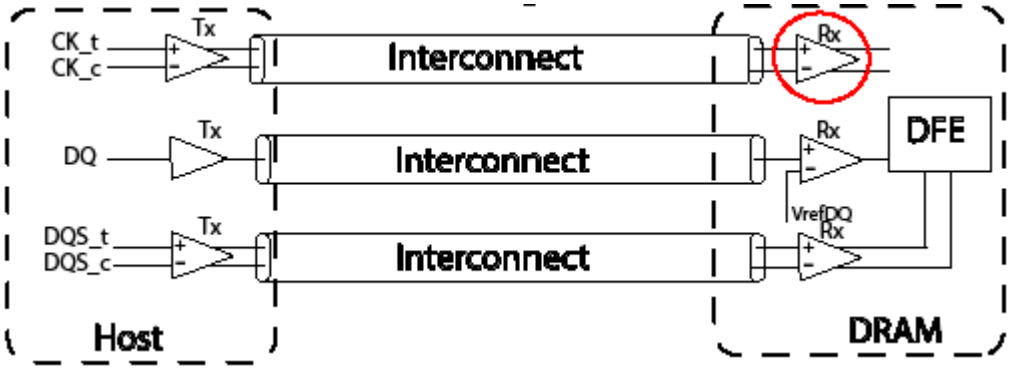


Figure 7 — Example of DDR5 Memory Interconnect

1.6.1 Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

Table 9 — Differential Input Clock Voltage Sensitivity Parameter for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input Clock Voltage Sensitivity (differential pp)	VRx_CK	-	200	-	200	-	180	-	180	-	160	mV	1,2

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)

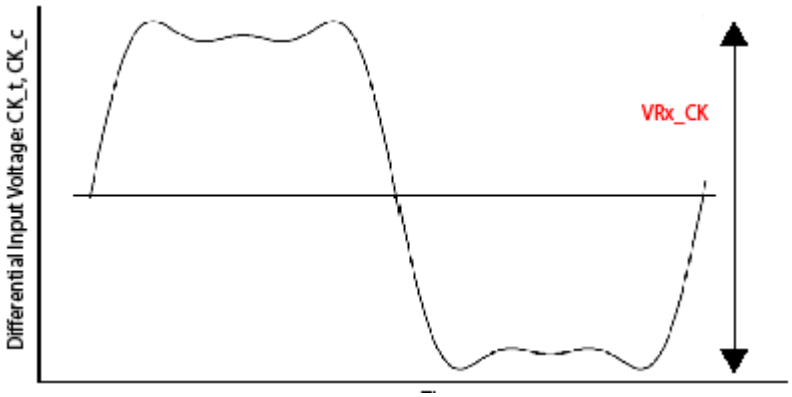


Figure 8 — VRx_CK

1.6.2 Differential Input Voltage Levels for Clock

Table 10 — Differential Clock (CK_t, CK_c) Input Levels for DDR5-3200 to DDR5-6400

From	Parameter	DDR5 3200-6400	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK_t, CK_c)	0.75 x $V_{diffpk-pk}$	1,2
$V_{ILdiff}CK$	Differential input low measurement level (CK_t, CK_c)	0.25 x $V_{diffpk-pk}$	1,2

Note(s):
1. $V_{diffpk-pk}$ defined in **Figure 188**
2. Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
3. All parameters are defined over the entire clock common mode range

1.6.3 Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below.

Figure 9 — Differential Input Slew Rate Definition for CK_t, CK_c

Table 11 — Differential Input Slew Rate Definition for CK_t, CK_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (CK_t - CK_c)	$VIL_{diff}CK$	$VIH_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) / deltaTRdiff	
Differential Input slew rate for falling edge (CK_t - CK_c)	$VIH_{diff}CK$	$VIL_{diff}CK$	($VIH_{diff}CK$ - $VIL_{diff}CK$) / deltaTFdiff	

Note(s):

Table 12 — Differential Input Slew Rate for CK_t, CK_c for DDR5-3200 to DDR5-4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for CK_t, CK_c	SRIdiff_CK	2	14	2	14	2	14	2	14	2	14	V/ns	

Note(s):

1.7 Rx DQS Jitter Sensitivity

The receiver DQS jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no cross-talk nor ISI is applied, and must pass through the combination of applied DCD and Rj.

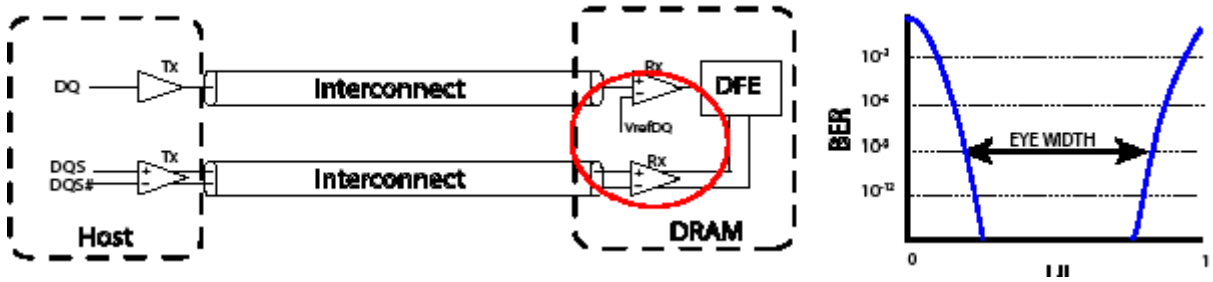


Figure 10 — SDRAM's Rx Forwarded Strobes for Jitter Sensitivity Testing

1.7.1 Rx DQS Jitter Sensitivity Specification

The following table provides Rx DQS Jitter Sensitivity Specification for the DDR5 DRAM receivers when operating at various possible transfer rates. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 13 — Rx DQS Jitter Sensitivity Specification for DDR5-3200 to 4800

[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj =Random Jitter]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ Timing Width	tRx_DQ_tMargin	0.900	-	0.875	-	0.825	-	0.825	-	0.825	-	UI	1,2,3,8, 9,10
Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in DQS	ΔtRx_DQ_tMargin_ DQS_DCD	-	0.06	-	0.06	-	0.06	-	0.06	-	0.06	UI	1,4,8,9, 10
Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in DQS	ΔtRx_DQ_tMargin_ DQS_Rj	-	0.09	-	0.09	-	0.09	-	0.09	-	0.09	UI	1,5,8,9, 10
Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in DQS	ΔtRx_DQ_tMargin_ DQS_DCD_Rj	-	0.15	-	0.15	-	0.15	-	0.15	-	0.15	UI	1,2,6,8, 9,10
Delay of any data lane relative to the DQS_t/DQS_c crossing	tRx_DQS2DQ	1	3	1	3	1	3	1	3.25	1	3.5	UI	1,7,8,9, 10

Note(s):

1. Validation methodology will be defined in future ballots. 2UI is defined as 1tCK for this parameter
2. Each of ΔtRx_DQ_tMargin_DQS_DCD, ΔtRx_DQ_tMargin_DQS_Rj, and ΔtRx_DQ_tMargin_DQS _DCD_Rj can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by 5% or more
3. DQ Timing Width - timing width for any data lane using repetitive patterns (check note 4 for the pattern) measured at BER=E-9
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 "1s" and 3 "0s"
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx DQS Jitter Sensitivity Testing.
7. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8. All measurements at BER=E-9

9. This test should be done after the DQS and DQ Voltage Sensitivity tests are completed and passing

10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

1.7.2 Test Conditions for Rx DQS Jitter Sensitivity Tests

Table 2 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx DQS Jitter Sensitivity parameters specified in **Table 13** and **Table 194**.

Table 14 — Test Conditions for Rx DQS Jitter Sensitivity Testing for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Applied DCD to the DQS	tRx_DQS_DCD	-	0.045	-	0.045	-	0.045	-	0.045	-	0.045	UI	1,2,3,6, 7,10
Applied Rj RMS to the DQS	tRx_DQS_Rj	-	0.0075	-	0.0075	-	0.0075	-	0.0075	-	0.0075	UI (RMS)	1,2,,4,6, 8,10
Applied DCD and Rj RMS to the DQS	tRx_DQS_DCD_Rj	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	-	0.045UI DCD + 0.0075UI Rj RMS	UI	1,2,5,6, 7,9, 10

Note(s):

1. While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2. The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin
3. Various DCD values should be tested, complying within the maximum limits
4. Various Rj values should be tested, complying within the maximum limits
5. Various combinations of DCD and Rj should be tested, complying within the maximum limits.The maximum timing margin degradation as a result of these injected jitter is specified in a separate table
6. Although DDR5 has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7. Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI)
8. RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
9. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI)
10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

1.8 Rx DQS Voltage Sensitivity

1.8.1 Overview

The receiver DQS (strobe) input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

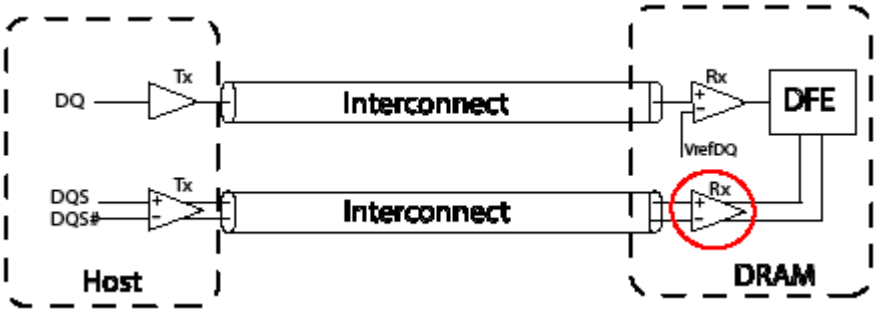


Figure 11 — Example of DDR5 Memory Interconnect

1.8.2 Receiver DQS Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 15 — Rx DQS Input Voltage Sensitivity Parameter for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS Rx Input Voltage Sensitivity (differential pp)	VRx_DQS	-	130	-	115	-	105	-	100	-	100	mV	1,2,3

Note(s):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)
3. Test using clock like pattern of repeating 3 "1s" and 3 "0s"

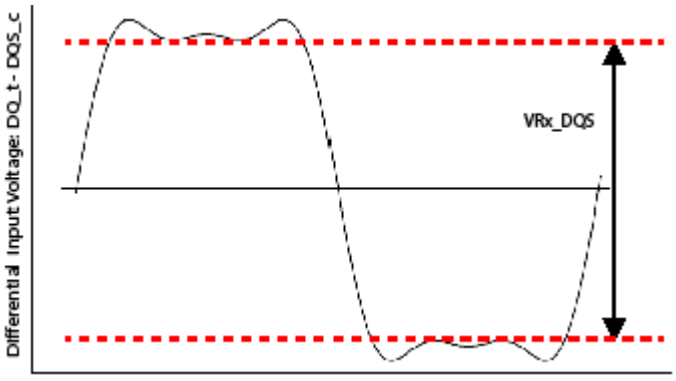


Figure 12 — VRx_DQS

1.9 Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (VIX)

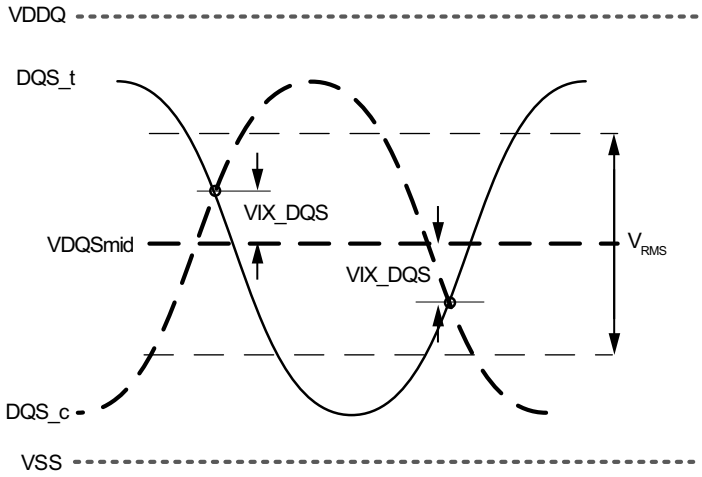


Figure 13 — VIX Definition (DQS)

Table 16 — Crosspoint Voltage (VIX) for DQS Differential Input Signals

Parameter	Symbol	DDR5-3200 - 4800		Unit	Notes
		Min	Max		
DQS differential input crosspoint voltage ratio	VIX_DQS_Ratio	-	50	%	1,2,3

Note(s):
1. The VIX_DQS voltage is referenced to VDQSmid(mean) = (DQS_t voltage + DQS_c voltage) /2, where the mean is over 8 UI
2. VIX_DQS_Ratio = (|VIX_DQS| / $|V_{RMS}|$)*100%, where V_{RMS} = RMS(DQS_t voltage - DQS_c voltage)
3. Only applies when both DQS_t and DQS_c are transitioning (including preamble)

1.9.1 Differential Input Levels for DQS

Table 17 — Differential Input Levels for DQS (DQS_t, DQS_c) for DDR5-3200 to DDR5-6400

From	Parameter	DDR5 3200-6400	Note
$V_{IHdiff}DQS$	Differential input high measurement level (DQS_t, DQS_c)	0.75 x $V_{diffpk-pk}$	1,2,3
$V_{ILdiff}DQS$	Differential input low measurement level (DQS_t, DQS_c)	0.25 x $V_{diffpk-pk}$	1,2,3

Note(s):
1. $V_{diffpk-pk}$ defined in **Figure 14**
2. $V_{diffpk-pk}$ is the mean high voltage minus the mean low voltage over TBD samples
3. All parameters are defined over the entire clock common mode range

1.9.2 Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals are defined and measured as shown below.

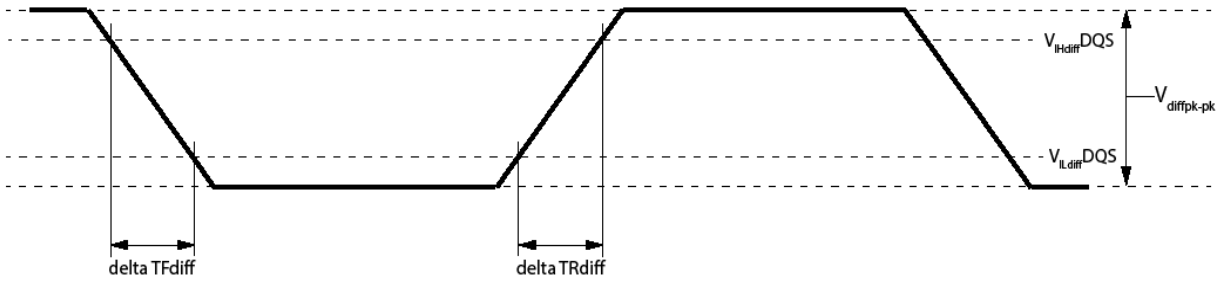


Figure 14 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Table 18 — Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined by	Notes
	From	To		
Differential Input slew rate for rising edge (DQS_t, DQS_c)	$V_{ILdiff}DQS$	$V_{IHdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTRdiff	1,2,3
Differential Input slew rate for falling edge (DQS_t, DQS_c)	$V_{IHdiff}DQS$	$V_{ILdiff}DQS$	($V_{IHdiff}DQS$ - $V_{ILdiff}DQS$) /deltaTFdiff	1,2,3

Note(s):

Table 19 — Differential Input Slew Rate for DQS_t, DQS_c for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for DQS_t, DQS_c	SRIdiff_DQS	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	V/ns	1

Note(s):

1.10 Rx DQ Voltage Sensitivity

1.10.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

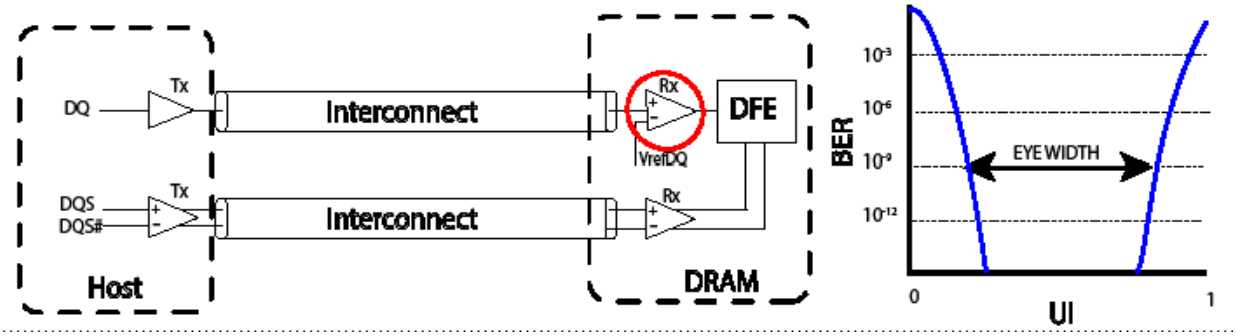


Figure 15 — Example of DDR5 Memory Interconnect

1.10.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5.

Table 20 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	85	-	75	-	70	-	65	-	65	mV	1,2,3

NOTE(S):

1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)
3. Recommend testing using clock like pattern such as repeating 3 "1s" and 3 "0s"

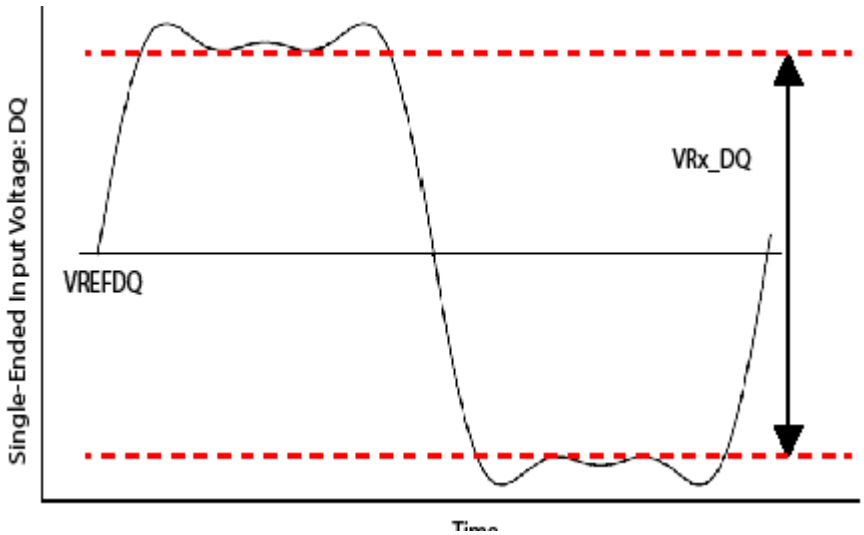
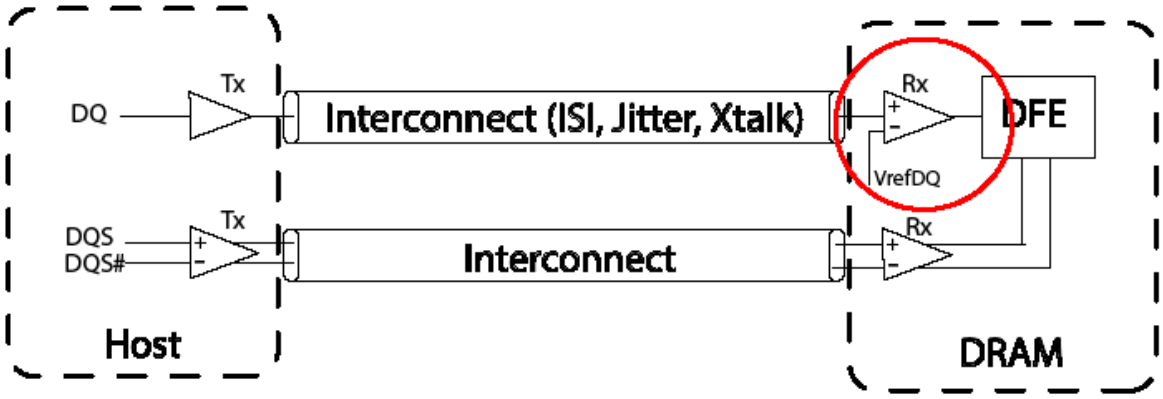


Figure 16 — VRx_DQ

1.11 Rx Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

Figure 17 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk



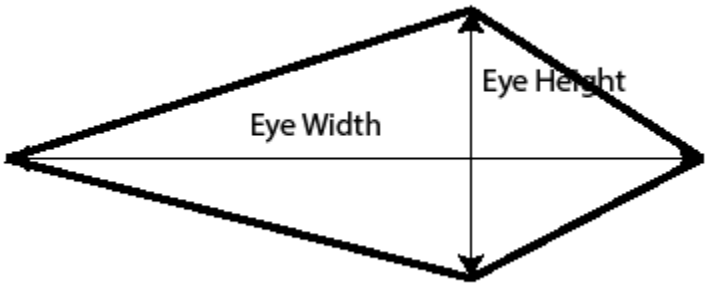


Figure 18 — Example of Rx Stressed Eye Height and Eye Width

1.11.1 Parameters for DDR5 Rx Stressed Eye Tests

Table 21 — Test Conditions for Rx Stressed Eye Tests for DDR5-3200 to 4800

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye height of stressed eye for Golden Reference Channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	-	95	-	85	-	80	-	75	-	70	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye Golden Reference Channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	-	600	mV	1.2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	0	125	mV p-p	1,2
Golden Reference Channel 1 Characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dB	3

Note(s):

1. Must meet minimum BER of $1E^{-16}$ or better requirement with the stressed eye at the slice of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER E^{-9} and extrapolating to BER E^{-16}.
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 shall be less than 60mV (|Tap-2| + |Tap-3| + |Tap-4| < 60mV).
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth spec, see DC Operating Conditions
7. The stressed eye is to be assumed to have a diamond shape
8. The VREFDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test, including the limits placed in Note 3.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, VrefDQ, and DFE solution to give the best eye margin.

1.12 Connectivity Test Mode - Input level and Timing Requirement

During CT Mode, input levels are defined below.
TEN pin: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ
CS_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
Test Input pins: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.
RESET_n: CMOS rail-to-rail with AC high and low at 80% and 20% of VDDQ.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

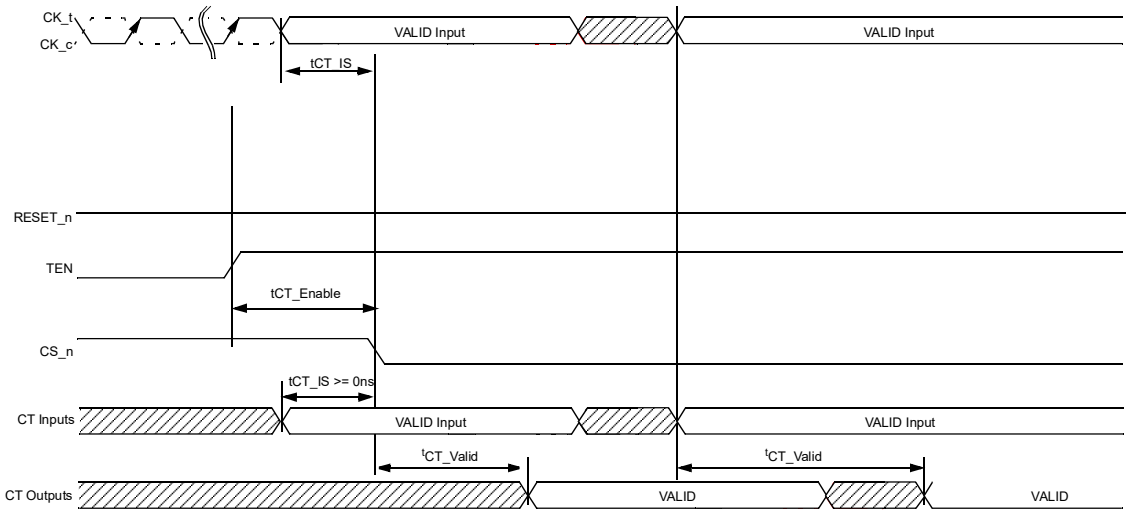


Figure 19 — Timing Diagram for Connectivity Test (CT) Mode

Table 22 — AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

1.12.1 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

Table 23 — CMOS rail to rail Input Levels for TEN, CS_n and Test inputs

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDDQ	VDDQ	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDDQ	VDDQ	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDDQ	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDDQ	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

Note(s):
1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

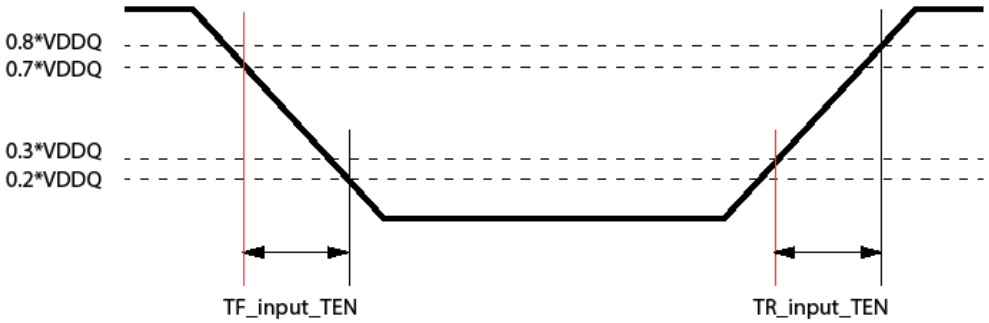


Figure 20 — TEN Input Slew Rate Definition

1.12.2 CMOS rail to rail Input Levels for RESET_n

Table 24 — CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDDQ	VDDQ	V	5
DC Input High Voltage	VIH(DC)_RESET	0.7*VDDQ	VDDQ	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDDQ	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDDQ	V	6
Rising time	TR_RESET	-	1.0	us	
RESET pulse width	tPW_RESET	1.0	-	us	3,4

Note(s):

1.After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. This definition is applied only for “Reset Procedure at Power Stable”.
5. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
6. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

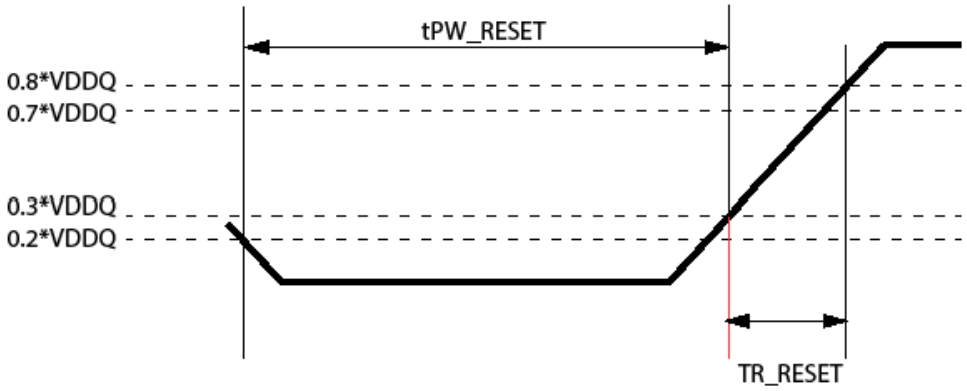


Figure 21 — RESET_n Input Slew Rate Definition

2. AC & DC Output Measurement Levels and Timing

2.1 Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

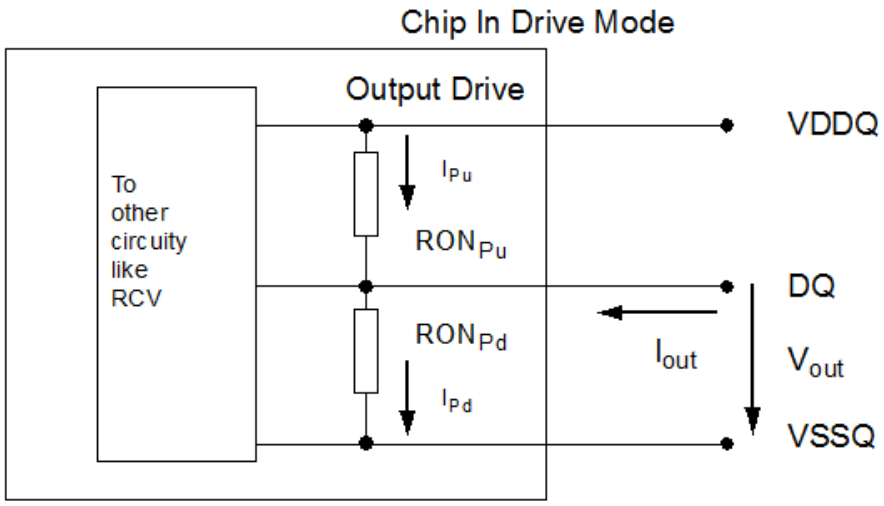


Table 25 — Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ron-nom is the nominal Ron value

$$MMPuPd = \frac{RONPu\text{-}RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax\text{-}RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax\text{-}RONPdMin}{RONNOM} * 100$$

5. This parameter of x16 device is specified for Upper byte and Lower byte.

2.2 Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$RON_{Pu} = \frac{VDDQ - Vout}{|Iout|}$$ under the condition that RONPd is off

$$RON_{Pd} = \frac{Vout}{|Iout|}$$ under the condition that RONPu is off

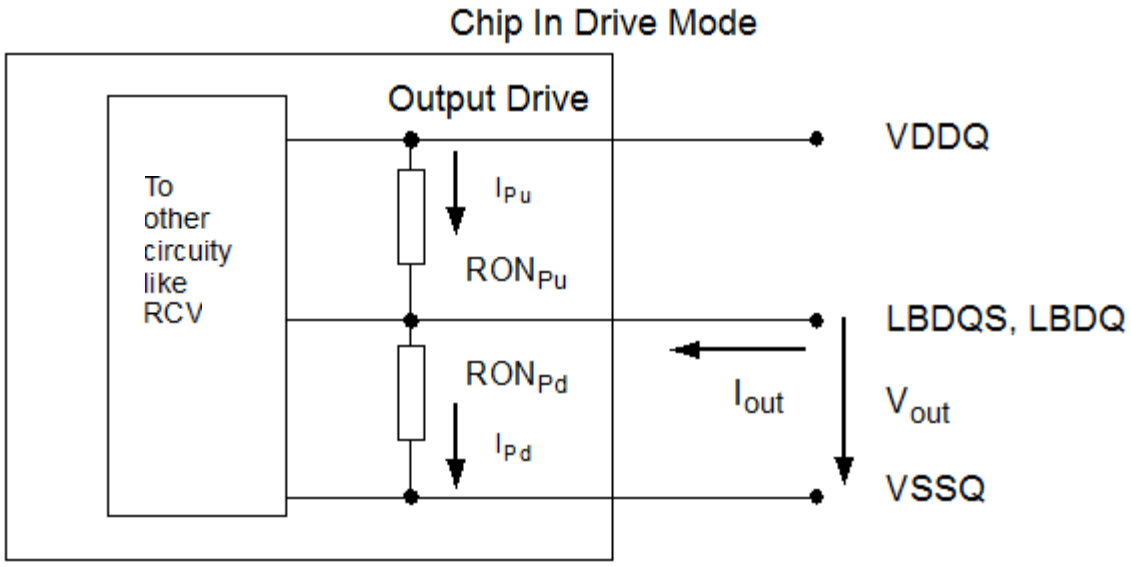


Figure 22 — Output Driver for Loopback Signals

Table 26 — Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.9	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,3,4
Mismatch LBDQS-LBDQ within device variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch LBDQS-LBDQ within device variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.

3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including LBDQS and LBDQ.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

2.3 Loopback Output Timing

Loopback strobe LBDQS to Loopback data LBDQ relationship is illustrated in **Figure 23**.

- tLBQSH describes the single-ended LBDQS strobe high pulse width
- tLBQSL describes the single-ended LBDQS strobe low pulse width
- tLBDQSQ describes the latest valid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBQH describes the earliest invalid transition of LBDQ measured at both rising and falling edges of LBDQS
- tLBDVW describes the data valid window per device per UI and is derived from (tLBQH-tLBDQSQ) of each UI on a given DRAM

Table 27 — Loopback Output Timing Parameters for DDR5-3200 to 4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Loopback Timing													
Loopback LBDQS Output Low Time	tLBQSL	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS Output High Time	tLBQSH	0.7	-	0.7	-	0.7	-	0.7	-	0.7	-	tCK	1
Loopback LBDQS to LBDQ Skew	tLBDQSQ	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK/2	1
Loopback LBDQ Output Time from LB-DQS	tLBQH	3.6	-	3.6	-	3.6	-	3.6	-	3.6	-	tCK/2	1
Loopback Data valid window (tLBQH-tLBDQSQ) of each UI per DRAM	tLBDVW	3.4	-	3.4	-	3.4	-	3.4	-	3.4	-	tCK/2	1

Note(s):

1: Based on Loopback 4-way interleave setting (see MR53)

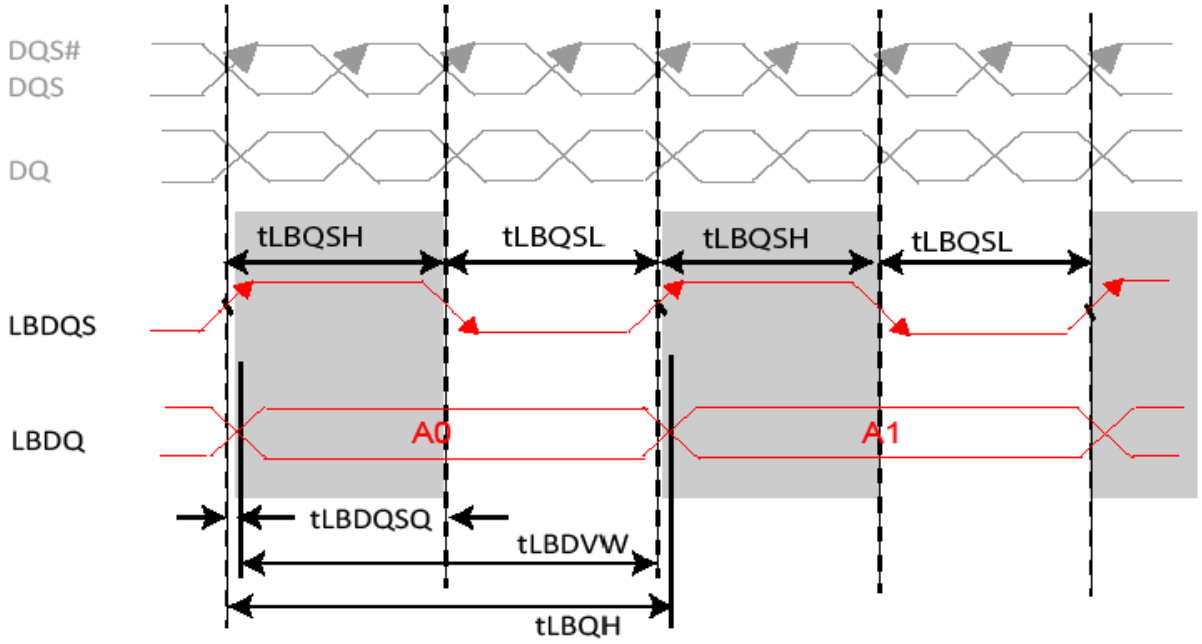
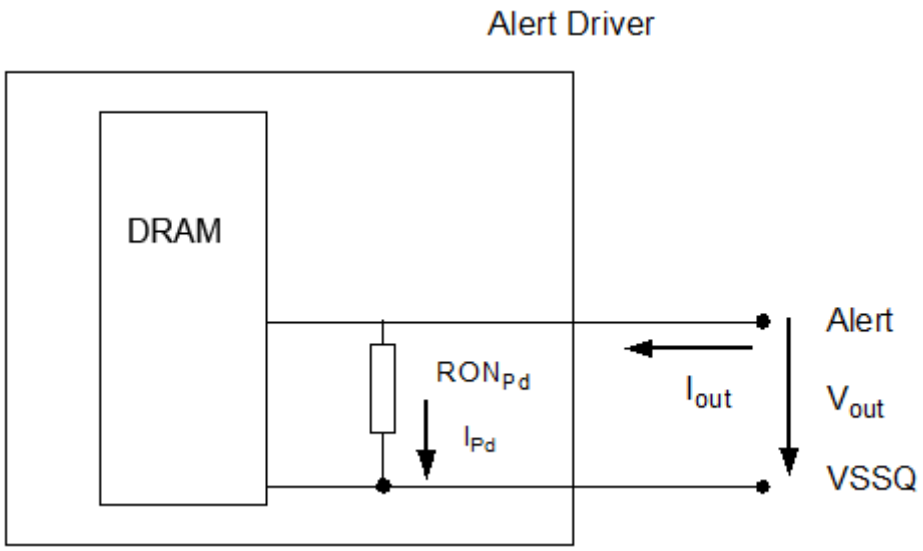


Figure 23 — Loopback Strobe to Data Relationship

2.3.1 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|Iout|} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$



Resistor	Vout	Min	Max	Unit	NOTE
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.1	$R_{ZQ}/7$	
	V_{OMdc} = 0.8* VDDQ	0.4	1.1	$R_{ZQ}/7$	
	V_{OHdc} = 0.95* VDDQ	0.4	1.25	$R_{ZQ}/7$	

Note(s):

2.3.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied to the Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

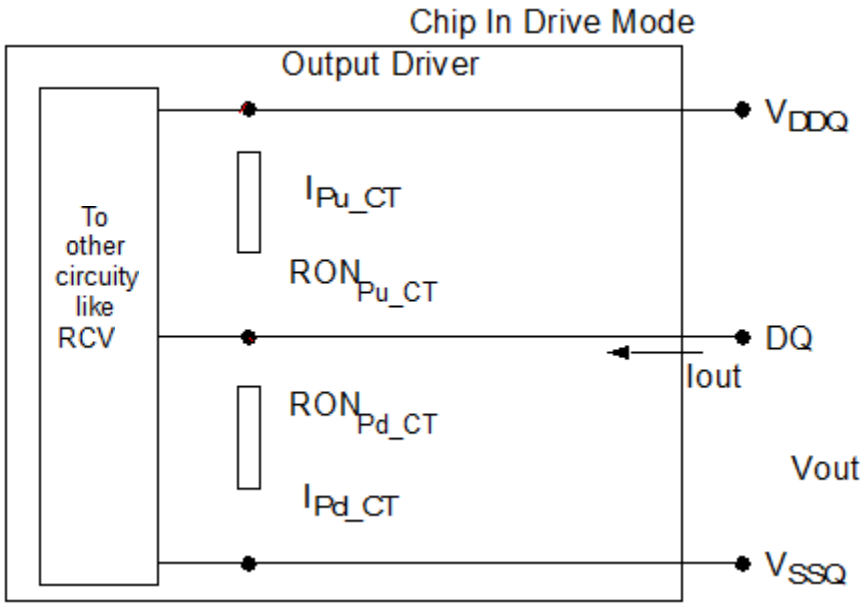


Figure 24 — Output Driver

RONNOM_CT	Resistor	Vout	Max	Units	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2
	RONPu_CT	VOBdc = 0.2 x VDDQ	1.9	$R_{ZQ}/7$	1,2
		VOLdc = 0.5 x VDDQ	2.0	$R_{ZQ}/7$	1,2
		VOMdc = 0.8 x VDDQ	2.2	$R_{ZQ}/7$	1,2
		VOHdc = 0.95 x VDDQ	2.5	$R_{ZQ}/7$	1,2

Note(s):
1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.
2. Uncalibrated drive strength tolerance is specified at +/- 30%

2.4 Single-ended Output Levels - VOL/VOH

Table 28 — Single-ended Output levels for DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

Note(s):
1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

2.5 Single-Ended Output Levels - VOL/VOH for Loopback Signals

Table 29 — Single-ended Output levels for Loopback Signals DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

Note(s):
1. V_{pk-pk} is the mean high voltage minus the mean low voltage over TBD samples.

2.6 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single ended signals as shown in Table 30 and Figure 25.

Table 30 — Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}	V_{OH}	$[V_{OH}-V_{OL}]$ / delta TRse
Single ended output slew rate for falling edge	V_{OH}	V_{OL}	$[V_{OH}-V_{OL}]$ / delta TFse

Note(s):
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

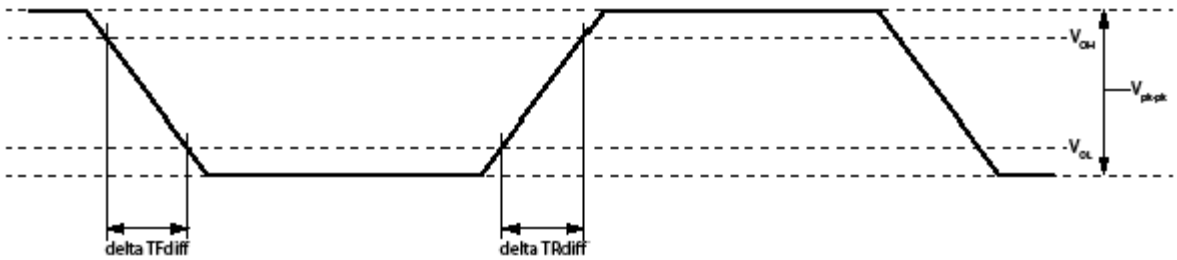


Figure 25 — Single-ended Output Slew Rate Definition

Table 31 — Single-ended Output Slew Rate for DDR5-3200 to DDR5-4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Single ended output slew rate	SRQse	8	18	8	18	8	18	8	18	8	18	V/ns	

Note(s):

2.7 Differential Output Levels

Table 32 — Differential Output levels for DDR5-3200 to DDR5-6400

Symbol	Parameter	DDR5-3200-6400	Units	Notes
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1

Note(s):
1. $V_{diffpk-pk}$is the mean high voltage minus the mean low voltage over TBD samples.

2.8 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL-diff}$ and V_{OHdiff} for differential signals as shown in Table 33 and Figure 26

Table 33 — Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}	V_{OHdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}	V_{OLdiff}	[V_{OHdiff}-V_{OLdiff}] / delta TFdiff

Note(s):
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure 26 — Differential Output Slew Rate Definition

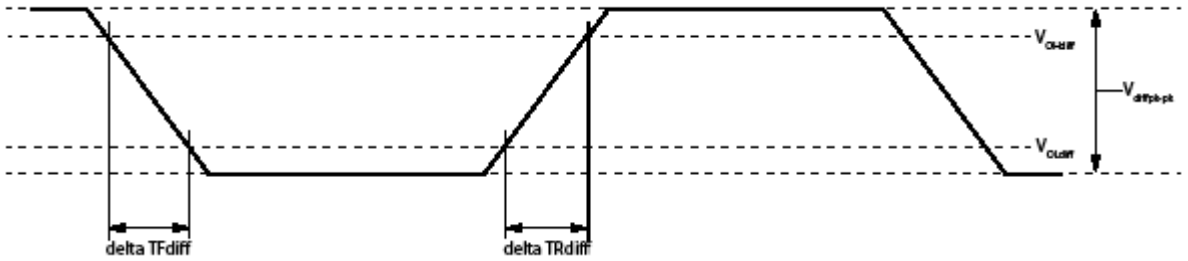


Table 34 — Differential Output Slew Rate for DDR5-3200 to DDR5-4800

Speed		DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Differential output slew rate	SRQdiff	16	36	16	36	16	36	16	36	16	36	V/ns	

Note(s):

2.9 Tx DQS Jitter

Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 35**.

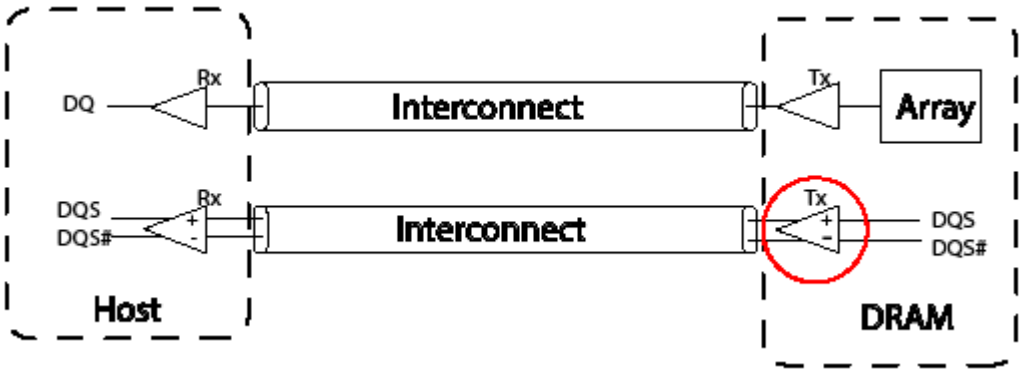


Table 35 — Tx DQS Jitter Parameters for DDR5-3200 to 4800

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,4, 5,6,7,8,9, 10,11,12
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1,2,3,5,6,7 ,8,9,10,11
Rj RMS Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	1,2,3,5,6,7 ,8,9,10,11, 12
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1,2,3,5,6,7 ,8,9,10,11

Note(s)

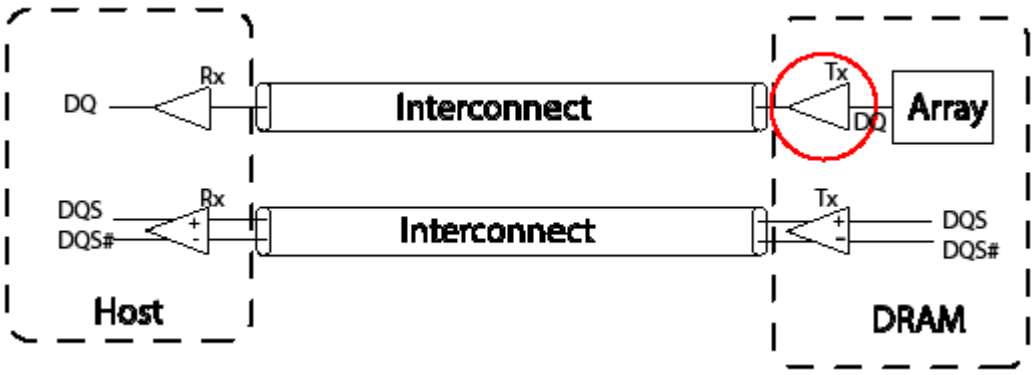
1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be signif-icant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. See Section 7.2 for details on the minimum BER requirements
6. See Section 7.3 for details on UI, NUI and Jitter definitions
7. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running the Tx DQ Jitter test
8. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44
9. Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test

10. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
11. Tested on the CTC2 card only
12. The max value of tTx_DQS_Rj_1UI_NoBUJ and tTx_DQS_Rj_NUI_NoBUJ can be 6mUI RMS

2.10 Tx DQ Jitter

2.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 36**.



2.10.2 Tx DQ Jitter Parameters

Table 36 — Tx DQ Jitter Parameters for DDR5-3200 to 4800

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rj RMS of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_NoBUJ	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	-	tCK_1UI_Rj_NoBUJ + 0.002	UI (RMS)	1,3,4,5,7, 8,9,10, 11, 12,13,14
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	3,5,7, 8,9,10, 11,12,13
Rj RMS of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_NoBUJ	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	-	tCK_NUI_Rj_NoBUJ + 0.002	UI (RMS)	3,5,7, 8,9,10, 11,12,13, 14
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_NoBUJ	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	3,6,7, 8,9,10, 11,12,13
Delay of any data lane relative to strobe lane	tTx_DQS2DQ	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	-0.100	0.100	UI	3,5,6,7,9, 10, 11,12,13

Note(s):

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
5. Delay of any data lane relative to strobe lane, as measured at Tx output
6. Vref noise level to DQ jitter should be adjusted to minimize DCD
7. See **Chapter 7** for details on the minimum BER requirements
8. See **Chapter 7** for details on UI, NUI and Jitter definitions
9. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
10. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
11. Spread Spectrum Clocking (SSC) must be disabled while running this test
12. These parameters are tested using the continuous clock pattern which are sent out from the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to “1” to enable this feature.
13. Tested on the CTC2 card only
14. The max value of tTx_DQ_Rj_1UI_NoBUJ and tTx_DQ_Rj_NUI_NoBUJ can be 6mUI RMS

2.11 Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E^{-9} and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40 OP[3:0]).

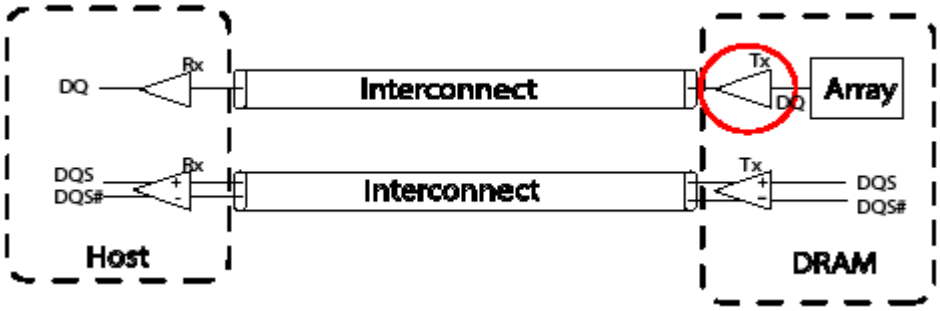


Figure 27 — Example of DDR5 Memory Interconnect

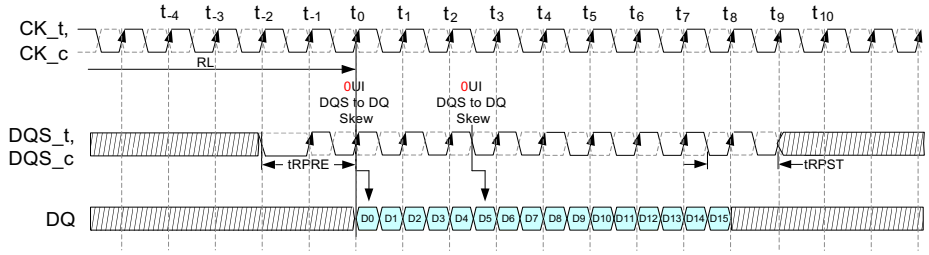


Figure 28 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 0 UI skew

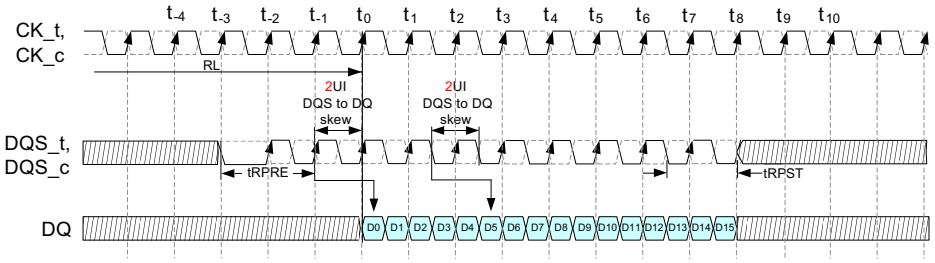


Figure 29 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 2 UI skew with Read DQS Offset Timing set to 1 Clock (2UI)

2.11.1 Tx DQ Stressed Eye Parameters

Table 37 — Tx DQ Stressed Eye Parameters for DDR5-3200 to 4800

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Eye Height specified at the transmitter with a skew between DQ and DQS of 1UI	TxEH_DQ_SES_1UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3, 4,6,7, 8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	TxEW_DQ_SES_1UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1,2,3, 4,6,7, 8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 2UI	TxEH_DQ_SES_2UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3, 4,6,7, 8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	TxEW_DQ_SES_2UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1,2,3, 4,6,7, 8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 3UI	TxEH_DQ_SES_3UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3, 4,6,7, 8,9,10
Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	TxEW_DQ_SES_3UI	0.72	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	1,2,3, 4,6,7, 8,9,10
Eye Height specified at the transmitter with a skew between DQ and DQS of 4UI	TxEH_DQ_SES_4UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3, 4,5,6, 7,8,9, 10
Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	TxEW_DQ_SES_4UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	UI	1,2,3, 4,5,6, 7,8,9, 10
Eye Height specified at the transmitter with a skew between DQ and DQS of 5UI	TxEH_DQ_SES_5UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	mV	1,2,3, 4,5,6, 7,8,9, 10
Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	TxEW_DQ_SES_5UI	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	UI	1,2,3, 4,5,6, 7,8,9, 10

Note(s):

1. Minimum BER E^{-9} and Confidence Level of 99.5% per pin
2. Refer to the minimum Bit Error Rate (BER) requirements for DDR5
3. The validation methodology for these parameters will be covered in future ballot(s)
4. Mismatch is defined as DQS to DQ mismatch, in UI increments
5. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable
6. Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster feature prior to running this test
7. The Mode Registers for the Duty Cycle Adjuster are MR43 and MR44. Also the Mode Registers for the Per Pin DCA of DQS are MR103-MR110, the Mode Registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \le x \le 7$, and the Mode Registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \le y \le 7$.
8. Spread Spectrum Clocking (SSC) must be disabled while running this test
9. These parameters are tested using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the dram device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to "1" to enable this feature.
10. Tested on the CTC2 card only
11. Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

3. IDD, IDDQ, IPP Specification Parameters and Test conditions

3.1 IDD, IPP and IDDQ Measurement Conditions

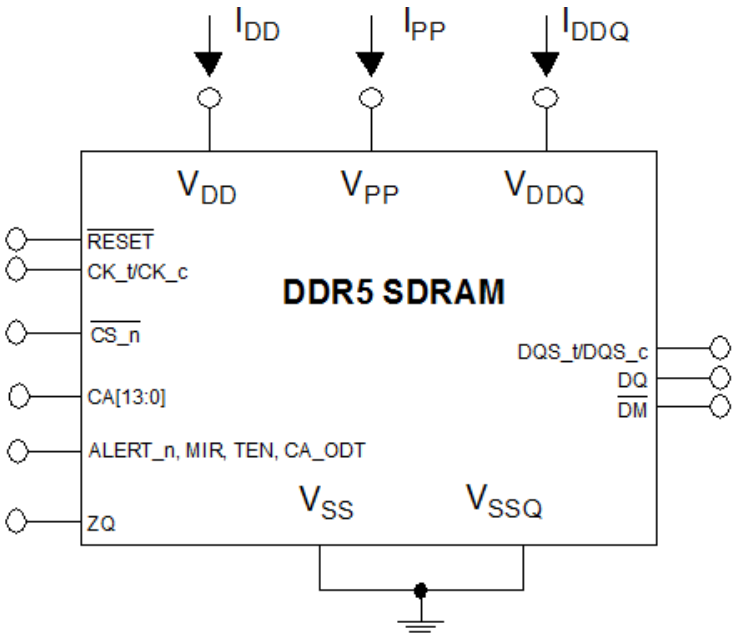
In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4W, IDDQ4W, IPP4W, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6, IDDQ6, IPP6 and IDD7, IDDQ7, IPP7) are measured as time-averaged currents with all VDD balls of the DDR5 SDRAM under test tied together. Any IDDQ or IPP current is not included in IDD currents.
- IDDQ currents are measured as time-averaged currents with all VDDQ balls of the DDR5 SDRAM under test tied together. Any IDD or IPP current is not included in IDDQ currents.
- IPP currents are measured as time-averaged currents with all VPP balls of the DDR5 SDRAM under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 31.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = VDDQ / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 189.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 190.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 191 through Table 200.
- IDD Measurements are done after properly initializing the DDR5 SDRAM. This includes but is not limited to setting
  TDQS_t disabled in MR5;
  CRC disabled in MR50;
  DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD, IDDQ or IPP measurement is started.



Note(s):
1. DIMM level Output test load condition may be different from above

Figure 30 — Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

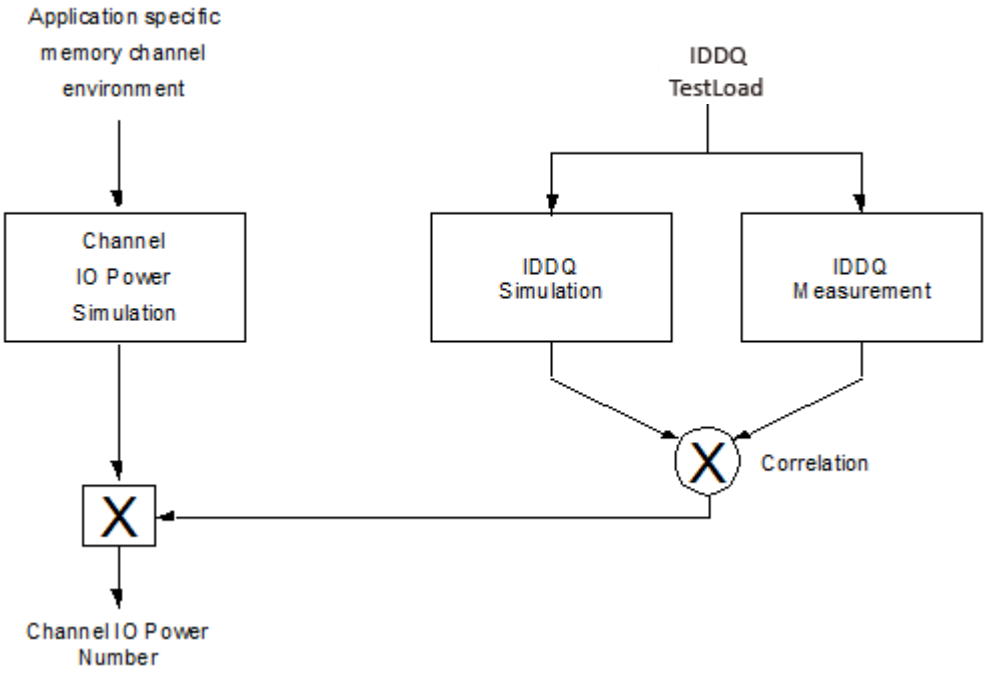


Figure 31 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

Table 38 — Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 288 on page 411; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 288 on page 411); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 288 on page 411
IDDQ0	**Operating One Bank Active-Precharge IDDQ Current** **Same condition with IDD0,** however measuring IDDQ current instead of IDD current
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0,** however measuring IPP current instead of IDD current
IDD0F	**Operating Four Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to Table 279 on page 418; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with four bank active at a time: (see Table 279 on page 418); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 279 on page 418
IDDQ0F	**Operating Four Bank Active-Precharge IDDQ Current** **Same condition with IDD0F,** however measuring IDDQ current instead of IDD current
IPP0F	**Operating Four Bank Active-Precharge IPP Current** **Same condition with IDD0F,** however measuring IPP current instead of IDD current
IDD2N	**Precharge Standby Current** **External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 280 on page 425; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 280 on page 425
IDDQ2N	**Precharge Standby IDDQ Current** **Same condition with IDD2N,** however measuring IDDQ current instead of IDD current
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N,** however measuring IPP current instead of IDD current
IDD2NT	**Precharge Standby Non-Target Command Current** **External clock:** On; **tCK**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between WRITE commands; **CS_n, CA Inputs:** partially toggling according to Table 281 on page 426; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 281 on page 426
IDDQ2NT (Optional)	**Precharge Standby Non-Target Command IDDQ Current** Same condition with IDD2NT, however measuring IDDQ current instead of IDD current
IPP2NT (Optional)	**Precharge Standby Non-Target Command IPP Current** Same condition with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	**Precharge Power-Down** **Device in Precharge Power-Down, External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IDDQ current instead of IDD current
IPP2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IPP current instead of IDD current
IDD3N	**Active Standby Current** **External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to Table 280 on page 425; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 280 on page 425
IDDQ3N	**Active Standby IDDQ Current** **Same condition with IDD3N,** however measuring IDDQ current instead of IDD current
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N,** however measuring IPP current instead of IDD current
IDD3P	**Active Power-Down Current** **Device in Active Power-Down, External clock:** On; **tCK**: see Table 266 on page 404; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2];

Table 38 — Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IDDQ3P	**Active Power-Down IDDQ Current** **Same condition with IDD3P,** however measuring IDDQ current instead of IDD current
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P,** however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** **External clock:** On; **tCK, nCCD, CL**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between RD; **CA Inputs:** partially toggling according to Table 282 on page 427; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 282 on page 427; **DM_n:** stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 282 on page 427); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 282 on page 427
IDD4RC	**Operating Burst Read Current with Read CRC** **Read CRC enabled[4]. Other conditions:** see IDD4R
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R,** however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** **External clock:** On; **tCK, nCCD, CL**: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** High between WR; **CA Inputs:** partially toggling according to Table 283 on page 432; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 283 on page 432; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 283 on page 432); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 283 on page 432
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** **Same condition with IDD4W,** however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W,** however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** **External clock:** On; **tCK, nRFC**1: see Table 266 on page 404; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 285 on page 441; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC1 (see Table 285 on page 441); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 285 on page 441
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IPP current instead of IDD current
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode)** **tRFC=tRFC2, Other conditions:** see IDD5B
IDDQ5F	**Burst Refresh IDDQPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IDDQ current instead of IDD current
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** **External clock:** On; **tCK, nRFCsb**: see Table 189 on page 404; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to Table 286 on page 446; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFCsb (see Table 286 on page 446); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 286 on page 446
IDDQ5C	**Burst Refresh IDDQPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh IPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IPP current instead of IDD current
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **External clock:** Off; CK_t and CK_c#: HIGH; tCK, nCPDED: see Table 266 on page 404; **BL:** 16[1]; **CS_n#:** low; **CA, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** All ODT disabled in MR32-MR35;
IDDQ6N	**Self Refresh IDDQ Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IDDQ current instead of IDD current

Table 38 — Basic IDD, IDDQ and IPP Measurement Conditions

Symbol	Description
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IPP current instead of IDD current
IDD6E	**SelfRefresh Current: Extended Temperature Range**) **T_{CASE}:** 85 - 95°C; Extended[4]; **External clock:** Off; CK_t and CK_c: HIGH; tCK, nCPDED: see Table 266 on page 404; **BL:** 16[1]; **CS_n:** low; **CA, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]
IDDQ6E	**Self Refresh IDDQ Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IDDQ current instead of IDD current
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IPP current instead of IDD current
IDD7	**Operating Bank Interleave Read Current** **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S CL**: see Table 266 on page 404; **BL:** 16[1]; **CS_n**: High between ACT and RDA; **CA Inputs:** partially toggling according to Table 288 on page 444; **Data IO:** read data bursts with different data between one burst and the next one according to Table 288 on page 444; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 288 on page 444; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see Table 288 on page 444
IDDQ7	**Operating Bank Interleave Read IDDQ Current** **Same condition with IDD7,** however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7,** however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** **External clock:** Off; CK_t and CK_c#: HIGH; tCK, nCPDED: see Table 266 on page 404; **BL:** 16[1]; **CS_n#:** low; **CA:**High**, DM_n:** stable at 1; **Bank Activity:** All banks closed and device in MPSM deep power down mode5; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Patterns Details**: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** **Same condition with IDD8,** however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Saving Deep Power Down IPP Current** **Same condition with IDD8,** however measuring IPP current instead of IDD current
IDD9 (Optional)	**MBIST Current** **Device in MBIST mode, External clock:** On; **CS_n**: Stable at 1 after MBIST entry; **CA Inputs:** stable at 1; **Data IO:** VDDQ; **Bank Activity:** MBIST operation; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ9 (Optional)	**MBIST IDDQ Current** **Same condition with IDD9,** however measuring IDDQ current instead of IDD current
IPP9 (Optional)	**MBIST IPP Current** **Same condition with IDD9,** however measuring IPP current instead of IDD current

Note(s):

1. Burst Length: BL16 fixed by MR0 OP[1:0]=00.

2. Output Buffer Enable
   - set MR5 OP[0] = 0] : Qoff = Output buffer enabled
   - set MR5 OP[2:1] = 00]: Pull-Up Output Driver Impedance Control = RZQ/7
   - set MR5 OP[7:6] = 00]: Pull-Down Output Driver Impedance Control = RZQ/7

   RTT_Nom enable
   - set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
   RTT_WR enable
   - set MR34 OP[5:3] = 010 RTT_WR = RZQ/2
     CA/CS/CK ODT, DQS_RTT_PART, and RTT_PARK disable
   - set MR32 OP[5:0] = 000000
   - set/MR33 OP[5:0] = 000000
   - set MR34 OP[2:0] = 000

3. WRITE CRC enabled
   - set MR50 OP[2:1] = 11

4. Read CRC enabled
   - set MR50:OP[0]=1

5. MPSM Deep Power Down Mode
   - set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
   - set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

3.2 IDD0, IDDQ0, IPP0 Pattern

Executes Active and PreCharge commands with tightest timing possible while exercising all Bank and Bank Group addresses. Note 2 applies to the entire table.

Table 39 — IDD0, IDDQ0, IPP0

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H	-	0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
	4	ACT	L H	-	0x03FFF	0x0	0x00	0x0	
	5	DES	H	Toggling1					Repeat sequence to satisfy tRAS(min), truncate if required
	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling1					Repeat sequence to satisfy tRP(min), truncate if required
1	8-15	Repeat sub-loop 0, use BG[2:0]=0x1 instead							
2	16-23	Repeat sub-loop 0, use BG[2:0]=0x2 instead							
3	24-31	Repeat sub-loop 0, use BG[2:0]=0x3 instead							
4	32-39	Repeat sub-loop 0, use BG[2:0]=0x4 instead							skip for x16
5	40-47	Repeat sub-loop 0, use BG[2:0]=0x5 instead							skip for x16
6	48-55	Repeat sub-loop 0, use BG[2:0]=0x6 instead							skip for x16
7	56-63	Repeat sub-loop 0, use BG[2:0]=0x7 instead							skip for x16
8-15	64-127	Repeat sub loops 0-7, use BA[1:0]=0x1 instead							
16-23	128-191	Repeat sub loops 0-7, use BA[1:0]=0x2 instead							
24-31	192-255	Repeat sub loops 0-7, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Note(s):

1. Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

3.3 IDD0F, IDDQ0F, IPP0F Pattern

Executes a rolling four bank group Active and PreCharge commands per tRC time while exercising all Bank, Bank, Group and CID addresses. Note 2 applies to the entire table.

Table 40 — IDD0F, IDDQ0F, IPP0F

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L H		0x00000	0x0	0x00	0x0	
	1	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	2	ACT	L H		0x00000	0x0	0x01	0x0	
	3	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	4	ACT	L H		0x00000	0x0	0x02	0x0	
	5	DES	H	Toggling1					Repeat to satisfy tRRD(min) (6 DES to meet 8nCK)
	6	ACT	L H		0x00000	0x0	0x03	0x0	
	7	DES	H	Toggling1					Repeat to satisfy tRAS(min) from Sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	14	PREpb	L			0x0	0x03	0x0	
	15	DES	H	Toggling1					Repeat for tRRD(min) (7 DES to meet 8nCK) This allows for next PRE to meet tRAS(min)
	16	DES	H	Toggling1					Repeat for tRC(min) from Sequence 0 first ACTIVATE. This will be zero DESELECTS for speed 4000Mbps and slower.
1	17-33	Repeat sub-loop 0, use Row Address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat sub-loop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							skip for x16
4-7	68-101	Repeat sub-loops 0-3, use BA[1:0]=0x1 instead							
8-11	102-135	Repeat sub-loops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat sub-loops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat sub loops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Note(s):

1. Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition.

3.4 IDD2N, IDD3N Pattern

Executes DESELECT commands while exercising all command/address pins in a predefined pattern. All notes apply to entire table.

Table 41 — IDD2N, IDDQ2N, IPP2N, IDD3N, IDDQ3N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

Note(s):
1. Data is pulled to VDDQ
2. DQS_t and DQS_c are pulled to VDDQ
3. Command / Address ODT is disabled
4. Repeat sequence 0 through 3.
5. All banks of all logical ranks mimic the same test condition.

3.5 IDD2NT, IDDQ2NT, IPP2NT Pattern

Executes Non-Target WRITE commands simulating Rank to Rank timing while exercising all C/A bits. Notes 3-6 apply to entire table.

Table 42 — IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE1	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling2	Repeat sequence to meet 1*tCCD_S(min), truncate if required
2	WRITE1	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling2	Repeat sequence to meet 1*tCCD(min), truncate if required

Note(s):
1. WRITE with CS_n=L on both cycles indicated a non-target WRITE.
2. Utilize DESELECTs between commands while toggling C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
3. Time between Non-Target WRITEs reflect tCCD_S (min) for ~~two~~ one rank~~s~~.
4. DQ signals are VDDQ.
5. DQS_t, DQS_c are VDDQ.
6. Repeat 0 through 3.

3.6 IDD4R, IDDQ4R, IPP4R Pattern

Executes READ commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses.
Notes 2-9 apply to entire table

Table 43 — IDD4R, IDDQ4R, IPP4R

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	READ	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	READ	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	READ	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands while toggling all C/A bits per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with Auto Precharge = H, Burst Chop = H.
3. Row address is set to 0x0000
4. Data reflects burst length of 16.
5. Data Pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF.
6. Data Pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0x~~0~~F, 0x0, 0xF, 0x~~F~~0, 0x~~F~~0, 0xF, 0x~~0~~F, 0x0, 0xF, 0x0, 0xF, 0x0.
7 Data Pattern for x8 each beat will reflect two like nibbles (Data Pattern A = 0x00, 0xFF, 0xFF...).
8. Data Pattern for x16 each beat will reflect two like bytes (Data Pattern A = 0x0000, 0xFFFF, 0xFFFF...).
9. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state

3.7 IDD4W, IDDQ4W, IPP4W Pattern

Executes WRITE commands with tightest timing possible while exercising all Bank, Bank Group and ~~CDI~~ CID addresses. Notes 2-6 apply to entire table.

Table 44 — IDD4W, IDDQ4W, IPP4W

Sub-Loop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [3:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L H	-	0x000	0x00	0x0	0x0	Pattern A	All “Valid” inputs = VDDQ
	1	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
1	2	WRITE	L H	-	0x3F0	0x00	0x1	0x0	Pattern B	All “Valid” inputs = VDDQ
	3	DES	H	Toggling1	-					Repeat sequence to satisfy tCCD_S(min), truncate if required
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead								skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead								skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead								skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead								skip for x16
8	16	WRITE	L H	-	0x3F0	0x00	0x0	0x0	Pattern B	All “Valid” inputs = VDDQ
	17	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
9	18	WRITE	L H	-	0x000	0x00	0x1	0x0	Pattern A	All “Valid” inputs = VDDQ
	19	DES	H	Toggling1						Repeat sequence to satisfy tCCD_S(min), truncate if required
10	20-21	Repeat sub-loop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat sub-loop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat sub-loop 8, use BG[2:0]=0x4 instead								skip for x16
13	26-27	Repeat sub-loop 9, use BG[2:0]=0x5 instead								skip for x16
14	28-29	Repeat sub-loop 8, use BG[2:0]=0x6 instead								skip for x16
15	30-31	Repeat sub-loop 9, use BG[2:0]=0x7 instead								skip for x16
16-31	32-33	Repeat sub-loops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat sub-loops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat sub-loops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat sub-loops 0-63 for each 3DS logical rank, if applicable								CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands ~~as specified~~ per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. WRITEs performed with Auto Precharge = H, Burst Chop = H.
3. Row address is set to 0x0000.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition.
6. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.

3.8 IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F Pattern

Executes Refresh (all Banks) command at minimum tRFC. Notes 3-6 apply to entire table.

Table 45 — IDD5B, IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sequence	Command	CS	C/A [13:0]	CA[9:8]	CID [2:0]	Special Instructions
0	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
1	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
2	REFab	L	-	H	0x0	All “valid” inputs = VDDQ
3	DES	H	Toggling1	-	-	Repeat sequence to satisfy tRFC(min)2, truncate if required
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For IDD5B, use tRFC1(min). For IDD5F, use tRFC2(min).
3. DQ signals are VDDQ.
4. All banks of all “non-target” logical ranks are Idd2N condition.
5. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
6. Must set CA8=H on REFab commands to indicate 1X refresh rate on devices that support RIR.

3.9 IDD5C, IDDQ5C and IPP5C Patterns

Executes Refresh (Same Bank) command at minimum tRFCsb. Notes 2-5 apply to entire table.

Table 46 — IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS	C/A [13:0]	CA[9:8]	BA [1:0]	CID [2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling1	-			Repeat sequence to satisfy tRFCsb(min), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable						CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. DQ signals are VDDQ.
3. All banks of all “non-target” logical ranks are Idd2N condition.
4. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
5. All banks of all “non-target” logical ranks are Idd2N condition.

3.10 IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R Pattern

All notes apply to entire table.

Table 47 — IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

Sequence	Command	Clock	CS	C/A [13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid tCKLCS(min) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy tCPDED(min), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A = H	CK_t = CK_c = H	L	0x3FFF	Repeat sequence indefinitely

Note(s):
1. Data is pulled to VDDQ
2. DQS_t and DQS_c are pulled to VDDQ
3. For 3DS, all banks of all logical ranks mimic the same test condition.

3.11 IDD7, IDDQ7 and IPP7 Patterns

Executes ACTVATE, READ/A commands with tightest timing possible while exercising all Bank, Bank Group and CID addresses. Notes 2-6 apply to entire table.

Table 48 — IDD7, IDD7Q, IPP7

Sub-Loop	Sequence	Command	CS	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L H	-	0x00000	-	0x0	0x0	0x0	-	
	1	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
1	2	ACT	L H	-	0x03FFF	-	0x0	0x1	0x0	-	
	3	DES	H	Toggling1							Repeat sequence to satisfy tRRD_S(min)
2	4-5	Repeat sub-loop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat sub-loop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat sub-loop 0, use BG[2:0]=0x4 instead									skip for x16
5	10-11	Repeat sub-loop 1, use BG[2:0]=0x5 instead									skip for x16
6	12-13	Repeat sub-loop 0, use BG[2:0]=0x6 instead									skip for x16
7	14-15	Repeat sub-loop 1, use BG[2:0]=0x7 instead									skip for x16
8	16	RDA	L H	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
	17	ACT	L H	-	0x00000	-	0x1	0x0	0x0	-	
	18	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
9	19	RDA	L H	-	-	0x000	0x0	0x1	0x0	Pattern B	
	20	ACT	L H	-	0x03FFF	-	0x1	0x1	0x0	-	
	21	DES	H	Toggling1							Repeat sequence to satisfy tCCD_S(min)
10	22-24	Repeat sub-loop 8, use BG[2:0]=0x2 instead									
11	25-27	Repeat sub-loop 9, use BG[2:0]=0x3 instead									
12	28-30	Repeat sub-loop 8, use BG[2:0]=0x4 instead									skip for x16
13	31-33	Repeat sub-loop 9, use BG[2:0]=0x5 instead									skip for x16
14	34-36	Repeat sub-loop 8, use BG[2:0]=0x6 instead									skip for x16
15	37-39	Repeat sub-loop 9, use BG[2:0]=0x7 instead									skip for x16
16-23	40-64	Repeat sub-loops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT									
24-31	65-89	Repeat sub-loops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT									
32-39	90-114	Repeat sub-loops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT									
...	...	Repeat sub-loops 0-18 for each 3DS logical rank, if applicable									CID[2:0]=0x1-0x7

Note(s):
1. Utilize DESELECTs between commands per the 4-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with Auto Precharge = L, Burst Chop = H.
3. x8 or x16 may have different Bank or Bank Group Address.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition
6. For 3DS, all banks of all “non-target” logical ranks are Idd2N condition

Standard Speed Bins

3DS DDR5-4400 Speed Bins and Operations

Table 1 — 3DS DDR5-4400 Speed Bins and Operations

Speed Bin					DDR5-4400B 3DS		Unit	NOTE
CL-nRCD-nRP					42-36-36			
Parameter				Symbol	min	max		
Read command to first data				tAA	18.750	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL	CL-2		nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Down Bins	Supported Frequency Down Bins			
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED		ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	ns	
3600AN	16.666	14.444	30	tCK(AVG)	RESERVED		ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED		ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED		ns	
Supported CL					22,30,32,34,36,38,40,42,44		nCK	

3DS DDR5-4800 Speed Bins and Operations

Table 2 — 3DS DDR5-4800 Speed Bins and Operations

Speed Bin					DDR5-4800B 3DS		Unit	NOTE
CL-nRCD-nRP					46-39-39			
Parameter				Symbol	min	max		
Read command to first data				tAA	18.750	22.222	ns	12
Activate to Read or Write command delay time				tRCD	16.000	-	ns	7
Row Precharge Time				tRP	16.000	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	48.000	-	ns	7,8
CAS Write Latency				CWL	CL-2		nCK	
Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRP-min (ns)[5]	Read CL[12]	Supported Frequency Down Bins	Supported Frequency Down Bins			
-	20.952	-	22	tCK(AVG)	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	tCK(AVG)	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	tCK(AVG)	0.625	0.681	ns	
3200AN	16.250	15.000	26	tCK(AVG)	RESERVED		ns	
3600C	20.000	17.777	36	tCK(AVG)	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	tCK(AVG)	0.555	<0.625	ns	
3600AN	16.666	14.444	30	tCK(AVG)	RESERVED		ns	
4000C	20.000	17.500	40	tCK(AVG)	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	tCK(AVG)	0.500	<0.555	ns	
4000AN	16.000	14.000	32	tCK(AVG)	RESERVED		ns	
4400C	20.000	17.727	44	tCK(AVG)	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	tCK(AVG)	0.454	<0.500	ns	
4400AN	16.363	14.545	36	tCK(AVG)	RESERVED		ns	
4800C	20.000	17.500	48	tCK(AVG)	0.416	<0.454	ns	
4800BN	19.166	16.666	46	tCK(AVG)	0.416	<0.454	ns	
4800B	19.166	16.250	46	tCK(AVG)	0.416	<0.454	ns	
4800AN	16.666	14.166	40	tCK(AVG)	RESERVED		ns	
Supported CL					22,30,32,34,36,38,40,42,44,46, 48		nCK	

DDR5 Speed Bin Table Note(s)

1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
2. The translation of all timing parameters from ns values to nCK values shall follow the Rounding Algorithm. The translation of tAA to CL shall follow the explicit combinations listed in the Speed Bin Tables.
3. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When selecting tCK(avg), requirements from the CL setting as well as requirements from the CWL setting shall be fulfilled.
4. 'Reserved' settings are not allowed. The user shall program a different value.
5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm, depending on the specific speed bin and down clock frequency combination.
6. DDR5-3200 AC timings apply if the DRAM operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
7. Parameters apply from tCK(avg)min to tCK(avg)max.
8. tRC(min) shall always be greater than or equal to tRAS(min) + tRP(min), and when using the appropriate rounding algorithms, nRC(min) shall always be greater than or equal to nRAS(min) + nRP(min).
9. tCK(avg).max of 1.010 ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000MT/s according to JESD404-1.
10. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC standard. The JEDEC standard does not require support for all speed bins within a given speed. The JEDEC standard requires meeting the parameters for a least one of the listed speed bins.
11. Any speed bin also supports functional operation at slower frequencies as shown in the table which are not subject to Production Tests but are verified by Design/Characterization.
12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the Speed Bin Tables. The CL Algorithm calculates supported CAS Latencies by rounding the operating frequency up to the next faster native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting tCK(AVG)min, and the bin target timings, the CL Algorithm then uses the Rounding Algorithm to calculate the valid CAS Latency. Because the DDR5 SDRAM specification only supports even CAS Latencies, odd CAS Latencies are rounded up to the next even CAS Latency. The 1980-2100 MT/s data rate always uses CL22. If tAA(corrected) or tRCDtRP(corrected) are violated, the CL Algorithm uses a slower combination of tAA(target) and tRCDtRP(target) to return slower valid CAS Latencies. The DDR5 SDRAM can support up to four valid CAS Latencies, CL(AN), CL(B), CL(BN), and CL(C), for a given frequency. tAA(corrected) and tRCDtRP(corrected) are calculated by reducing tAA(min), tRCD(min), and tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin Tables, or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information.

```
// Variables already defined in other areas of the DDR5 SDRAM specification
CorrFact       = 0.30                                          // (%)   Rounding Algorithm correction factor
ScaledCorrFact = 997                                           //       Scaled correction factor (1000*(1-0.30%))
tCKreal        =1011-952, 682-238                              // (ps)  Real application tCK(AVG) (1980-2100MT/s, 2933-8400MT/s)
tAAmin         MONO=14000-17500, 3DS=16000-20000               // (ps)  From Speed Bin Tables and DIMM SPD bytes 30-31
tRCDtRPmin     MONO=14000-17500, 3DS=14000-17500               // (ps)  From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
tAAcorr        = TRUNC(tAAmin*ScaledCorrFactor/1000)           // (ps)  Corrected tAA(min) per the Rounding Algorithm rules
tRCDtRPcorr    = TRUNC(tRCDtRPmin*ScaledCorrFactor/1000)       // (ps)  Corrected tRCD(min), tRP(min) per the Rounding Algorithm
FUNC[RA(targ)] = TRUNC((targ*ScaledCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
// Round tCKreal down to the next faster standard frequency (tCK in ps)
IF (TRUNC(2000000/(2000*99%))>=TRUNC(tCKreal)>=TRUNC(2000000/(2000*105%)))            // Check for  1980-2100 nominal data rates
   tCKstd=TRUNC(2000000/2000)                                                         // Assign standard 2000 tCK (ps)
ELSE IF (TRUNC(2000000/(2000+7*(133+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200))   // Check for  2933-3200 nominal data rates
   tCKstd=TRUNC(2000000/3200)                                                         // Assign standard 3200 tCK (ps)
ELSE
   FOR (DataRateNom=3200; DataRateNom<=8000; DataRateNom=DataRateNom+400)             // Check for >3200-8400 nominal data rates
      IF (TRUNC(2000000/DataRateNom)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
         tCKstd=TRUNC(2000000/(DataRateNom+400))                                      // Assign standard 3600-8400 tCK (ps)
      ELSE
         tCKstd=RESERVED                                                              // No valid data rate found

// Timing targets (ps) that have been used to define the Speed Bin Tables
// MONO targets            3DS targets
   BinAN_tAAtarg     = 14000 BinAN_tAAtarg     = 16000         // tAA target for AN bins
   BinB__tAAtarg     = 16000 BinB__tAAtarg     = 18500         // tAA target for AN, B bins
   BinBN_tAAtarg     = 16000 BinBN_tAAtarg     = 18500         // tAA target for AN, B, BN bins
   BinC__tAAtarg     = 17500 BinC__tAAtarg     = 20000         // tAA target for AN, B, BN, C bins
```

```
   BinAN_tRCDtRPtarg = 14000 BinAN_tRCDtRPtarg = 14000         // tRCD, tRP target for AN bins
   BinBN_tRCDtRPtarg = 16000 BinBN_tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B, BN bins
   BinC__tRCDtRPtarg = 17500 BinC__tRCDtRPtarg = 17500         // tRCD, tRP target for AN, B, BN, C bins
IF (TRUNC(2000000/3600)>tCKstd)                                // tRCD, tRP target for B bins is frequency dependent
   BinB__tRCDtRPtarg = 16000 BinB__tRCDtRPtarg = 16000         // tRCD, tRP target for AN, B bins data rates faster than 3600
ELSE
   // 16250=(2000000/3200)*EVEN(TRUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
   BinB__tRCDtRPtarg = 16250 BinB__tRCDtRPtarg = 16250         // tRCD, tRP target for AN, B bins for data rates 3600 and slower

// CL Algorithm using variables defined above
// Up to four valid CL's can be returned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
// The B and BN bins return the same CL
// Only even CL's (not odd CL's) are valid per the DDR5 SDRAM specification
// nRCD, nRP are only even at standard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
// nRCD, nRP may be even or odd at standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
IF (TRUNC(2000000/2000)=tCKstd)                                // CL22 is the only valid CL for 1980-2100 data rates
   CL(AN)=22                                                   // Valid even CL for AN bins
   CL(B )=22                                                   // Valid even CL for AN, B, bins
   CL(BN)=22                                                   // Valid even CL for AN, B, BN bins
   CL(C )=22                                                   // Valid even CL for AN, B, BN, C bins
ELSE IF (TRUNC(2000000/3200)>=tCKstd>=TRUNC(2000000/8400))     // Valid CL for 2933-8400 data rates
   IF      ((EVEN(RA(BinAN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinAN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=EVEN(RA(BinAN_tAAtarg))                           // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinB__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinB__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=EVEN(RA(BinB__tAAtarg))                           // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinBN_tAAtarg))*tCKstd>=tAAcorr)AND(EVEN(RA(BinBN_tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even only
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=EVEN(RA(BinBN_tAAtarg))                           // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE IF ((EVEN(RA(BinC__tAAtarg))*tCKstd>=tAAcorr)AND(    (RA(BinC__tRCDtRPtarg))*tCKstd>=tRCDtRPcorr)) // nRCD, nRP even, odd
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                          // Valid even CL for AN, B, BN bins
      CL(C )=EVEN(RA(BinC__tAAtarg))                           // Valid even CL for AN, B, BN, C bins
   ELSE                                                        // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
      CL(AN)=RESERVED                                          // Valid even CL for AN bins
      CL(B )=RESERVED                                          // Valid even CL for AN, B bins
      CL(BN)=RESERVED                                          // Valid even CL for AN, B, BN bins
      CL(C )=RESERVED                                          // Valid even CL for AN, B, BN, C bins
ELSE                                                           // No valid data rate found
   CL(AN)=RESERVED                                             // Valid even CL for AN bins
   CL(B )=RESERVED                                             // Valid even CL for AN, B bins
   CL(BN)=RESERVED                                             // Valid even CL for AN, B, BN bins
   CL(C )=RESERVED                                             // Valid even CL for AN, B, BN, C bins
```

Current Specification

128GB 16Gx80 Module (4Rank of x4) RDIMM

Module Current		unit	note
Symbol	4800		
IDD0	418.8	mA	
IDD0F	508.3	mA	
IDD2N	383.8	mA	
IDD2P	355.9	mA	
IDD3N	497.7	mA	
IDD3P	470.3	mA	
IDD4R	938.3	mA	
IDD4W	1060.7	mA	
IDD5	754.2	mA	
IDD5B	727.3	mA	
IDD5C	495.0	mA	
IDD6N	425.9	mA	
IDD7	1035.3	mA	
IDD8	204.6	mA	

Note(s):
Module IDD is based on PMIC 12V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

Current Specification

256GB 32Gx80 Module (8Rank of x4) RDIMM

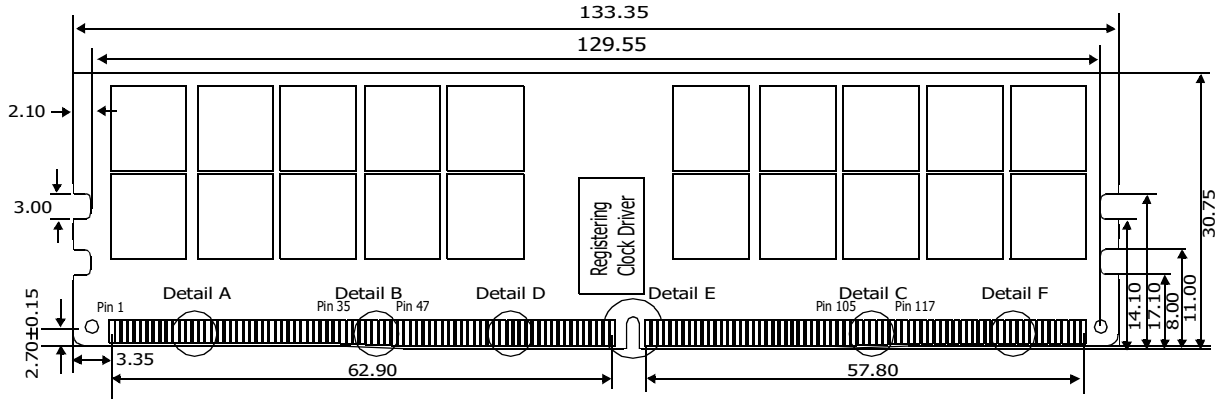
Module Current		unit	note
Symbol	4800		
IDD0	536.9	mA	
IDD0F	624.0	mA	
IDD2N	501.7	mA	
IDD2P	472.8	mA	
IDD3N	709.2	mA	
IDD3P	685.9	mA	
IDD4R	1174.3	mA	
IDD4W	1302.6	mA	
IDD5	867.6	mA	
IDD5B	840.6	mA	
IDD5C	610.0	mA	
IDD6N	773.1	mA	
IDD7	1202.9	mA	
IDD8	312.2	mA	

Note(s):
Module IDD is based on PMIC 12V input current, each IDD parameter includes all IDD/IDDQ/IPP of DRAM, RCD current and PMIC efficiency.

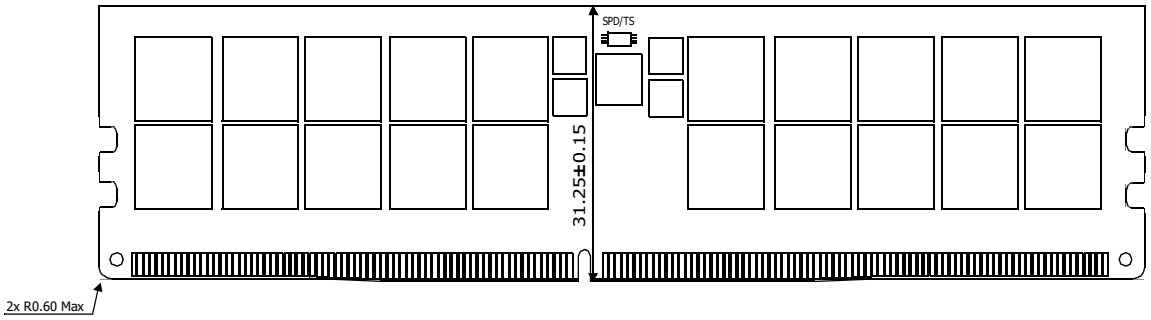
Module Dimensions

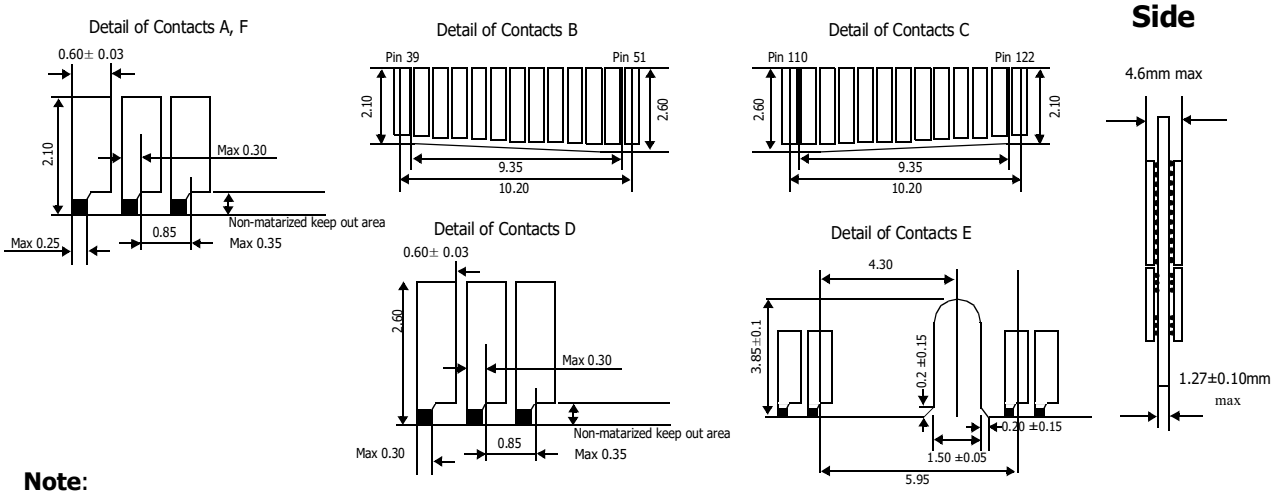
128GB 16Gx80 Module (4Rank of x4) RDIMM

Front



Back





Note:

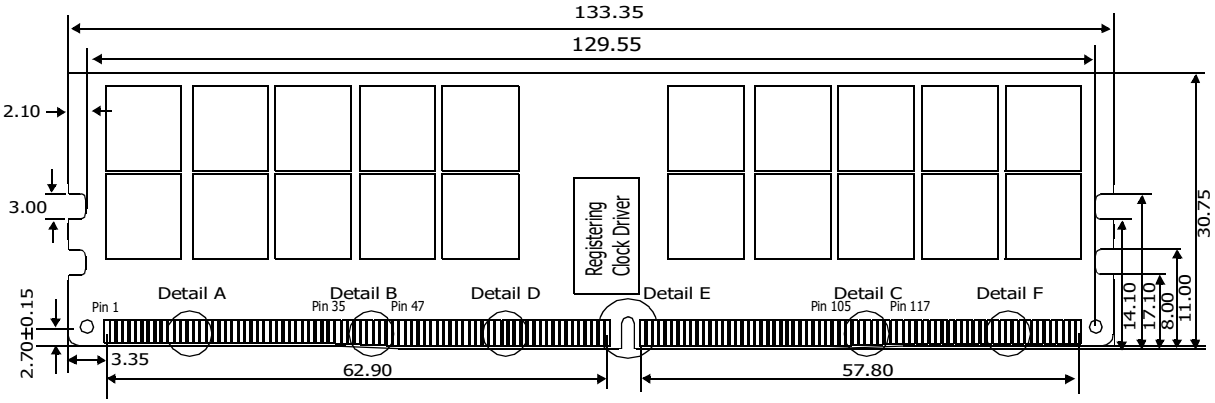
1. ±0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters

Module Dimensions

256GB 32Gx80 Module (8Rank of x4) RDIMM

Front



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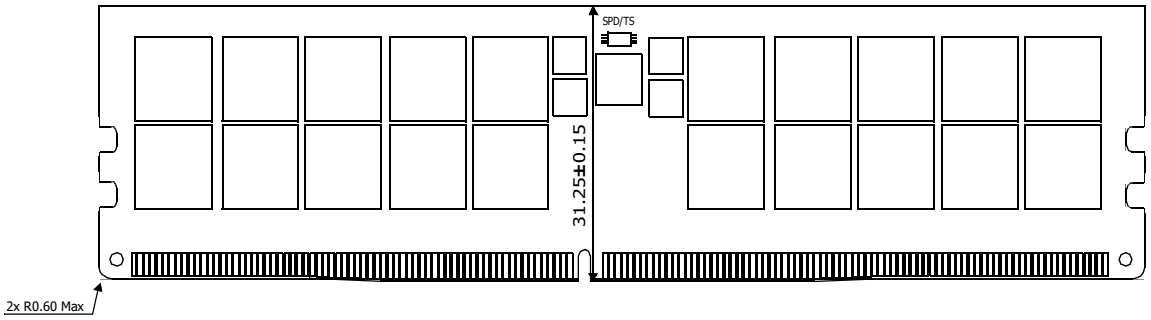

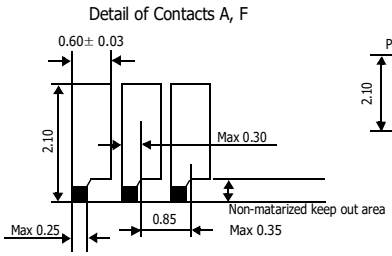

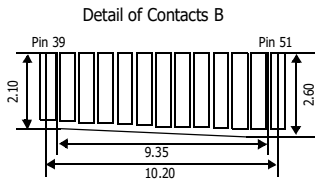

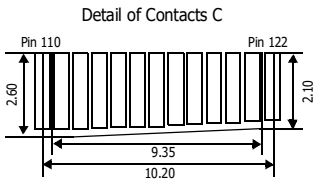

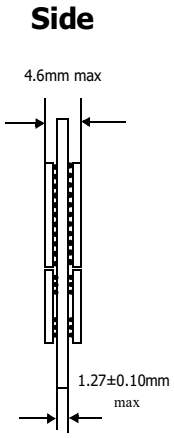

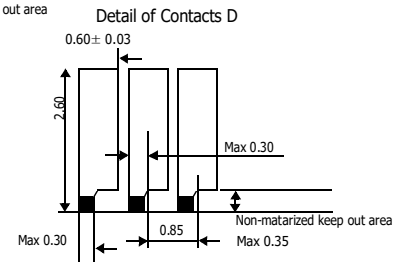

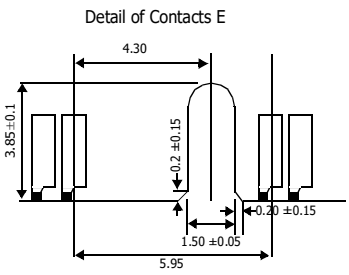

Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters