M74LS74AP

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS74AP is a semiconductor intergrated circuit containing 2 D-type positive edge-triggered flip-flop circuits with discrete terminals for clock input T, data input D and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Each flip-flop can be used independently.
- Direct set and reset inputs
- Positive edge-triggering
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20 ~ +75°C)

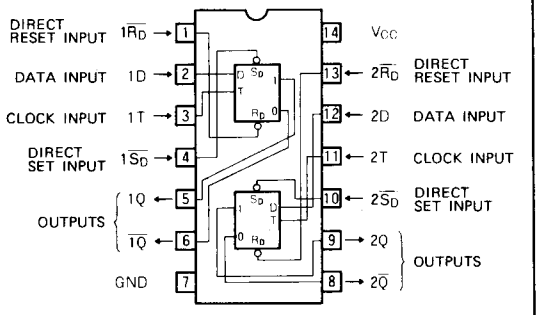
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

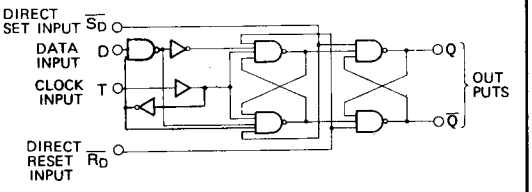
When T changes from low to high, the D signal immediately before the change emerges in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into a direct R-S flip-flop. When both S_D and R_D are low, Q = $\overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a D-type filip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH FLIP-FLOP)



FUNCTION TABLE

$\overline{S_D}$	$\overline{R_D}$	T	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H *	H *
H	H	L	X	Q^0	$\overline{Q}^0$
H	H	↑	H	H	L
H	H	↑	L	L	H

Note 1: ↑ : Transition from low to high-level

Q^0 : level of Q before the indicated steady-state input conditions were established.

$\overline{Q}^0$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.

X : Irrelevant

* : Nonstable; it will not persist when $\overline{R_D}$, $\overline{S_D}$ inputs return to their inactive (high) level.

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

MITSUBISHI ELECTRIC

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leq 0.4V$	0		4	mA
		$V_{OL} \leq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC} = 4.75V$, $I_{IC} = -18mA$				1.5	V
V_{OH}	High-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$	$I_{OL} = 4mA$		0.25	0.4	V
				$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	D, T	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$\overline{S}_D$, $\overline{R}_D$					40	μA
		D, T	$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
		$\overline{S}_D$, $\overline{R}_D$					0.2	mA
I_{IL}	Low-level input current	D, T	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
		$\overline{S}_D$, $\overline{R}_D$					−0.8	mA
I_{OS}	Short-circuit output current (Note 2)		$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC} = 5.25V$, (Note 3)			4	8	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.

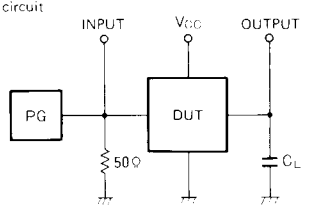
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: Measurement circuit

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 4)	25	50		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to Q, $\overline{Q}$			11	25	ns
t_{PHL}				11	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S}_D$, $\overline{R}_D$ to Q, $\overline{Q}$			8	25	ns
t_{PHL}				11	40	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$

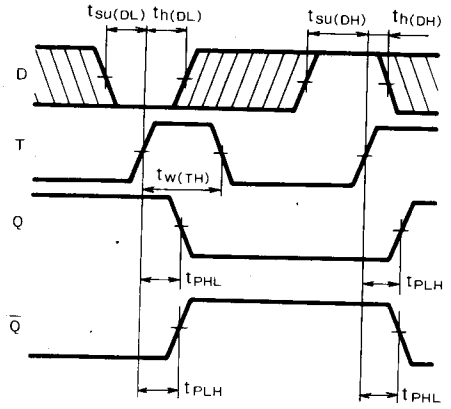
(2) C_L includes probe and jig capacitance.

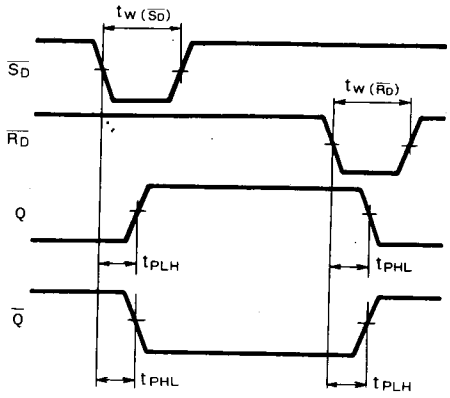
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(TH)}$	Clock input T high pulse width		25	4		ns
$t_{w(\overline{S_D}, \overline{R_D})}$	Direct set and reset inputs $\overline{S_D}$, $\overline{R_D}$ pulse width		25	4		ns
$t_{su(DH)}$	Setup time high D to T		20	10		ns
$t_{su(DL)}$	Setup time low D to T		20	8		ns
$t_{h(DH)}$	Hold time high D to T		5	− 5		ns
$t_{h(DL)}$	Hold time low D to T		5	− 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

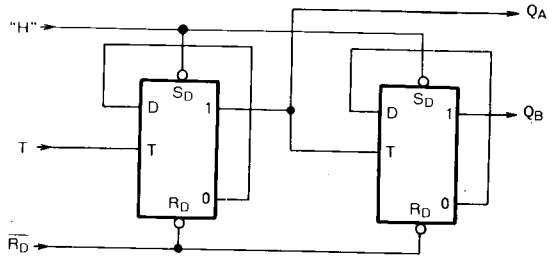


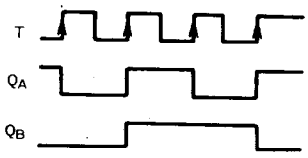


Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

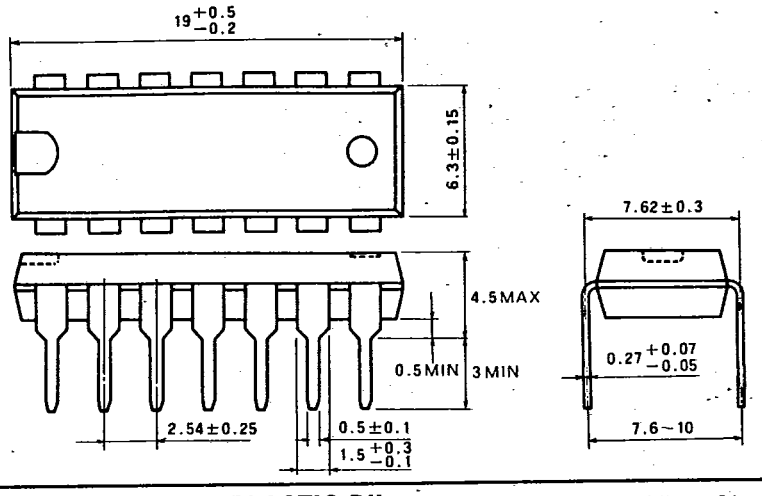
¼divider





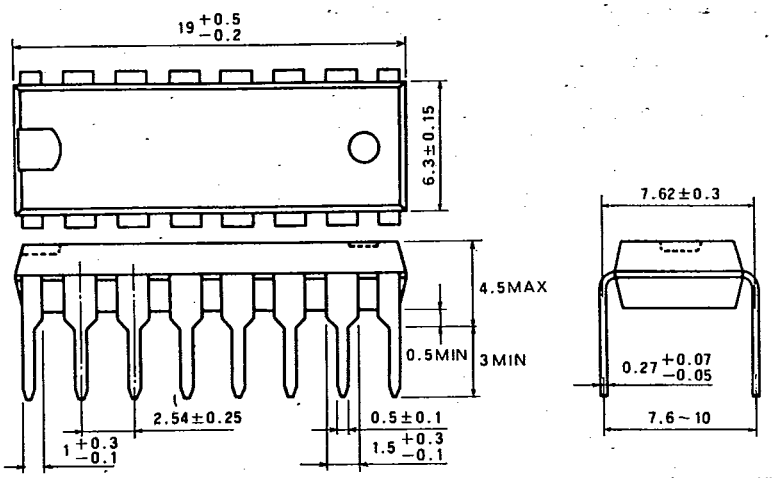
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm