Enhanced Memory Systems Inc.

SM2405 - Enhanced SDRAM

512Kx32 ESDRAM

Product Brief

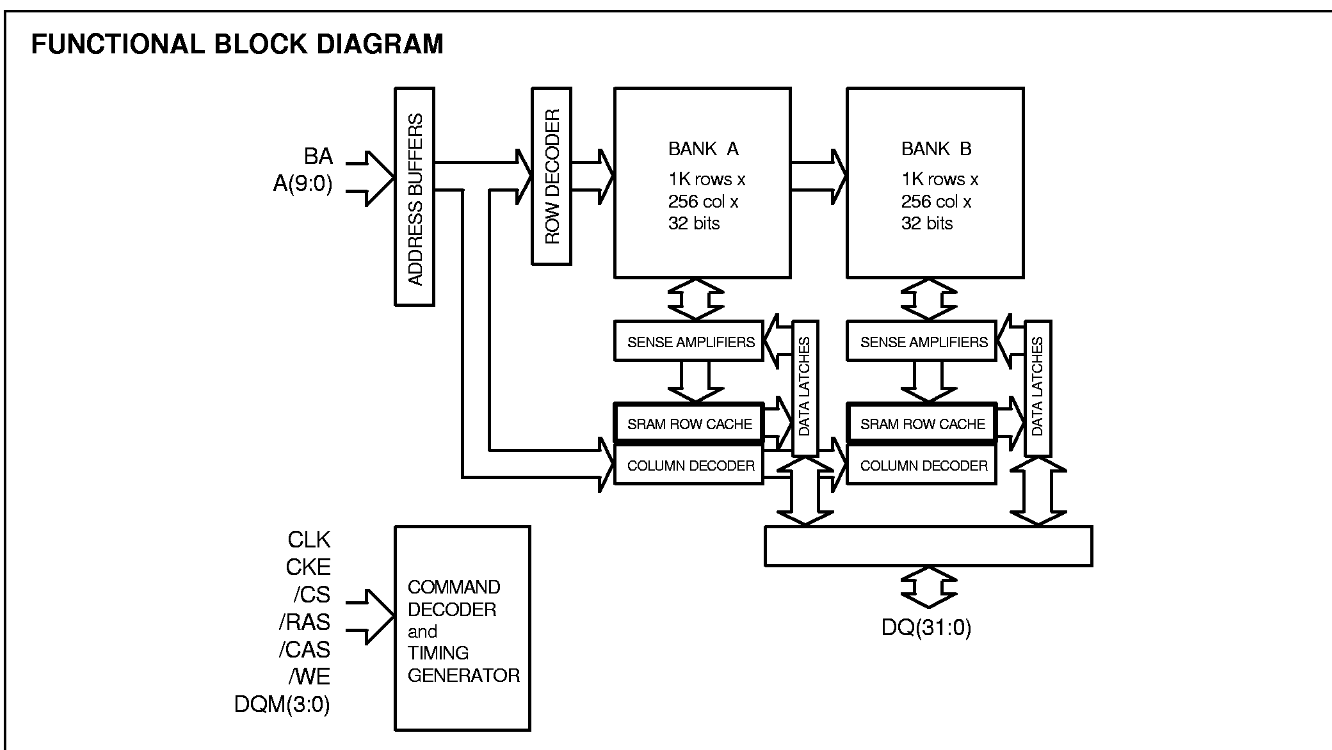
Features

- 100% Function and Timing Compatible with JEDEC standard SDRAM
- Pin Compatible with JEDEC Std. SGRAM
- Integrated 8Kbit SRAM Row Cache per Bank
- Synchronous Operation up to 150MHz
- 24ns Row Access Latency, 10ns Column Latency
- Two Bank Architecture
  - 1K rows x 256 column x 32 bits x 2 banks
- Early Auto-Precharge
- Programmable Burst Length (1, 2, 4, 8, full page)
- Programmable CAS Latency (1, 2, 3)
- Hidden Auto-Refresh without closing Read Pages
- Low Power Suspend, Self-Refresh, and Power Down Modes Supported
- Optional “No Write Transfer” Mode
- Optional Read DQM Latency = 1 for CL=1 (EMRS)
- Single 3.3V Power Supply
- Flexible V_{DDQ} Supports LVTTL and 2.5V I/O
- Programmable Output Impedance (EMRS)
- 2K / 32ms Refresh
- 100-pin LQFP (0.65mm pin pitch)

Description

The SM2405 Enhanced SDRAM (ESDRAM) is a single data rate I/O device which combines raw speed with innovative architecture to optimize system price/performance in high performance video graphics and embedded systems. The device is pin compatible with industry standard SGRAM. It is also function and timing compatible with JEDEC standard SDRAMs.

The two bank architecture combines 24ns DRAM arrays with a 10ns SRAM row cache per bank. The SM2405 is a superset technology of JEDEC standard SDRAM. Its two key functional features include early auto-precharge (close DRAM page while burst reads are performed) and an optional No Write Transfer mode. The ESDRAM is capable of maintaining two open read pages and two open write pages simultaneously via the No Write Transfer mode.



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Architecture

The ESDRAM architecture combines two banks of fast 24ns DRAM with two banks of 11ns SRAM row register cache on one chip to improve memory latency. On a page read miss, a DRAM bank is activated and data is developed by the DRAM sense amplifiers in 13.3ns. The sense amplifiers now hold an entire row of data (8K bits). On a read command, the entire row is latched into the SRAM row register and the specified starting address is output in 10ns (CAS Latency 1 at clock frequencies up to 83MHz, and CAS Latency 2 up to 150MHz). The architecture allows fast 11ns latency to any of the constantly open rows on page hits.

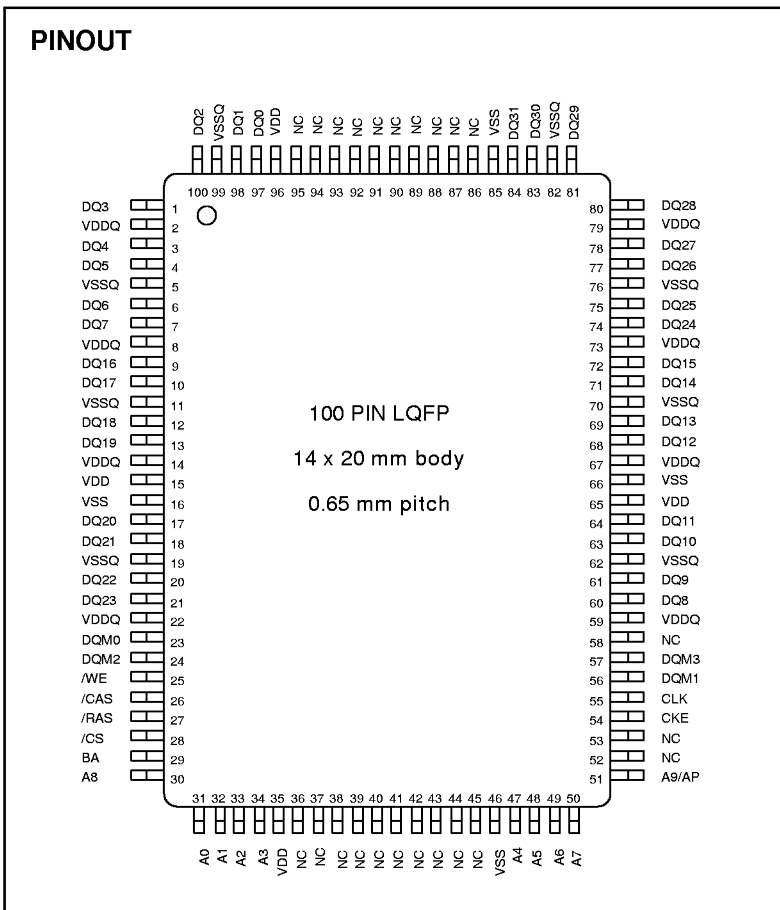
Early auto-precharge can be performed since row data is latched separately in the SRAM row cache from the DRAM sense amplifiers. The precharge time can be hidden behind a burst read from cache. This minimizes subsequent page miss latency. The auto-precharge begins one clock cycle after the Read-Autoprecharge command and completes early enough to allow the next pipelined random access to complete by the end of the current burst cycle.

At 150MHz, all but one cycle of the next random access to any location in the same bank can be hidden to increase sustained bandwidth by up to two times over standard SDRAM. For interleaved burst read accesses, the entire precharge time is hidden and output data can be driven without any wait states.

The ESDRAM architecture also offers the designer two different cache load strategies via the mode register set for write cycles. In Write Transfer mode, the row register cache is always loaded with the sense amplifier (DRAM data) contents on a write command. This ensures coherency between the row cache and the DRAM array. This allows read-modify-write cycles and simplified memory control logic.

In No Write Transfer mode, the row register cache is not loaded during writes. Data is written to the DRAM sense amplifiers and the prior row contents are maintained in the row cache (for write page misses). If the on-chip page hit/miss comparator determines that the write is to the same row latched in the SRAM row cache, the write updates the row cache as well as the DRAM sense amplifiers to maintain coherency. No Write Transfer mode allows immediate return to the prior cached read page without otherwise incurring a page miss penalty. Write page precharge and a bank activate times can be hidden during cache reads. The ESDRAM's fast precharge time minimizes latency between the end of a write and the next read or write miss cycle. If a cache read follows a write cycle, write precharge time can be hidden.

The synchronous interface of the ESDRAM allows operation at clock rates up to 150MHz with 2.5V I/O levels. Fast input set-up and clock-to-output times allow actual system operation at the specified clock rate.



Compatibility

By making the ESDRAM exactly pin-compatible with JEDEC standard SDRAM, it is possible for the memory controller to support both types of memory with a simple mode selection. Both SDRAM and ESDRAM use identical memory footprints on the planar and identical SO-DIMM module wiring. Systems designed to support both memory types can provide two distinct price/performance points and a simple field upgrade with the ESDRAM.

Basic Operating Modes

The ESDRAM operating modes are specified in the following text and in the table below.

Hit and Miss Terminology - "Hit" and "miss" refer to whether or not a new row address presented to the ESDRAM matches a row already activated in the device. There are up to two rows or "pages" that can be open at any given point in time. The row data or page contents consist of 8192 bits or 256 32-bit words and are held in each bank's sense amplifiers. Each page is selected by the bank select pin BA. Each bank's SRAM row cache is loaded only when a read command is issued. The ESDRAM's on-chip row address comparator is used only in No Write Transfer mode of operation.

The memory controller typically stores row or page address tags in order to determine which command to issue based on the tag compare result.

Mode Register Set - Two mode registers are loaded from pins BA and A9-A0 when /CS, /RAS, /CAS, and /WE are low. The standard mode register specifies the burst length, burst type, CAS latency, and write transfer mode. The standard mode register is set by issuing an MRS command while BA is low. Read DQM latency mode and output driver impedance are optionally set via the extended mode register (EMRS). The extended mode register is set by issuing an MRS command while BA is high.

Bank Activate - BA specifies one of the two banks and the row address A9-A0 specifies which of the 1024 rows to load into its sense amplifiers. In No Write Transfer mode, the ESDRAM compares the last row read address to the current row address. If the two row addresses match, a subsequent write updates the SRAM row cache in addition to the DRAM. Otherwise, only the DRAM is written.

Write - The ESDRAM performs a write or burst write to the bank specified by BA and begins writing at the start address specified by the column address A7-A0. If the A9/AP pin is high, the auto-precharge operation begins one cycle following the last write of the burst. Note: In No Write Transfer mode, if the on-chip hit/miss comparator result (from ACTV cycle) indicates a page hit, then the write is performed to both the row cache and the DRAM.

Read - The ESDRAM loads the row cache and performs a read or burst read from the cache to the bank specified by BA and begins reading at the start address specified by the column address A7-A0. If the A9/AP pin is high, the auto-precharge operation begins one cycle following this command. The first read data is output from the memory after the CAS latency (defined by the Mode Register Set) has been satisfied.

Burst Terminate - The ESDRAM terminates a burst read after a delay equal to the CAS latency. It will terminate a burst write and mask data in the current cycle.

Single Bank Precharge - The ESDRAM will perform a manual precharge of the bank specified by BA while A9/AP is low. Manual precharge terminates a burst read after a delay equal to the CAS latency. It will also terminate a burst write and mask data in the current cycle.

Precharge All Banks - The ESDRAM will precharge both open banks if A9/AP is high. It will terminate burst cycles exactly the same as the Single Bank Precharge command.

Auto Refresh (CBR) - The ESDRAM will perform an internal refresh cycle on both DRAM banks. Both banks must be closed before this command is executed. Unlike standard SDRAM, this command can be executed while performing cache burst reads. The contents of each row cache are not lost during Auto Refresh cycles.

Self Refresh Entry - The ESDRAM enters a self refresh mode with refresh cycles automatically generated by an internal clock. Self Refresh mode continues as long as CKE is low. All input buffers except CKE are disabled. The chip is in a low power standby mode.

Device Deselect - When /CS is high, the command decoder is disabled but the prior command will be completed (i.e. a burst will complete).

Clock Suspend/Standby Mode - When CKE is low, the internal execution of the current command is suspended until CKE returns high.

Power Down Entry/Exit - If both DRAM banks are precharged, CKE is low, and /CS is high, the chip will enter its power down mode. Once the chip is in power down mode, the chip will exit power down mode one clock after CKE is returned high.

Data Write/Output Enable - When DQM is low, write data is written to the chip during a write command and the output buffers are enabled during read commands. In standard mode, DQM latency is two cycles for reads and zero cycles for writes. In the optional mode (see EMRS), DQM latency is one cycle for reads only when CAS latency is set to 1.

Data Mask/Output Disable - When DQM is high, write data is masked during a write command and the output buffers are disabled during read commands. In standard mode, DQM latency is two cycles for reads and zero cycles for writes. In the optional mode (see EMRS), DQM latency is one cycle for reads only when CAS latency is set to 1.

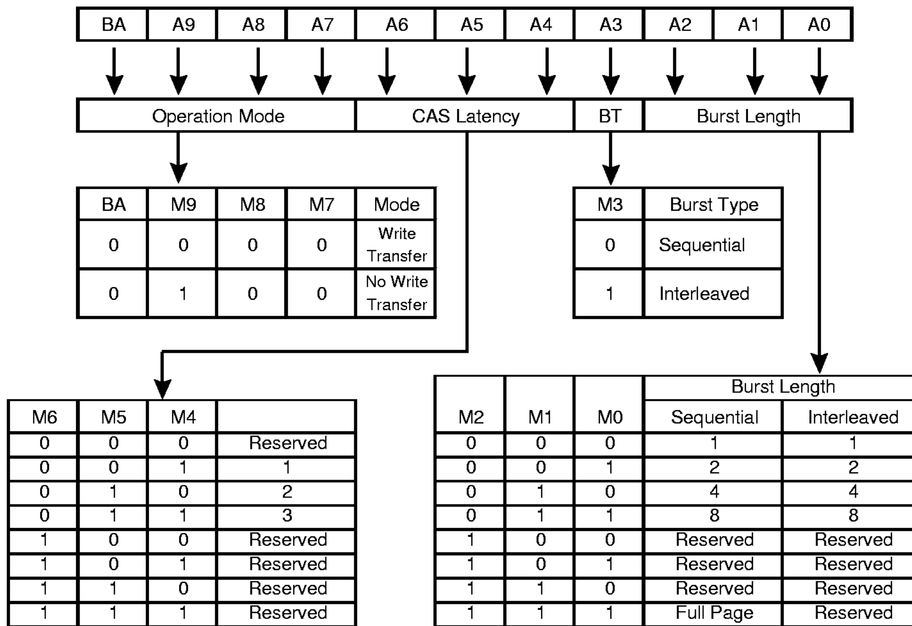
ESDRAM Command Truth Table

Function	CKE		/CS	/RAS	/CAS	/WE	DQM	BA	A9/AP	A8	A7-A0
	Previous Cycle	Current Cycle									
Mode Register Set	H	X	L	L	L	L	X	L	Op Code		
Extended Mode Register Set	H	X	L	L	L	L	X	H	Op Code		
Bank Activate	H	X	L	L	H	H	X	BS	Row Address		
Write with Auto-Precharge	H	X	L	H	L	L	X	BS	H	X	Column
Write	H	X	L	H	L	L	X	BS	L	X	Column
Read with Auto-Precharge	H	X	L	H	L	H	X	BS	H	X	Column
Read	H	X	L	H	L	H	X	BS	L	X	Column
Burst Termination	H	X	L	H	H	L	X	X	X	X	X
Single Bank Precharge	H	X	L	L	H	L	X	BS	L	X	X
Precharge All Banks	H	X	L	L	H	L	X	X	H	X	X
Auto-Refresh (CBR)	H	H	L	L	L	H	X	X	X	X	X
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	X
Self Refresh Exit	L	H	NOP or DESEL				X	X	X	X	X
No Operation	H	X	L	H	H	H	X	X	X	X	X
Device Deselect	H	X	H	X	X	X	X	X	X	X	X
Clock Suspend/Standby	L	X	X	X	X	X	X	X	X	X	X
Power Down Mode Entry	H	L	NOP or DESEL				X	X	X	X	X
Power Down Mode Exit	L	H	NOP or DESEL				X	X	X	X	X
Data Write/Output Enable	H	X	X	X	X	X	L	X	X	X	X
Data Mask/Output Disable	H	X	X	X	X	X	H	X	X	X	X

Pin Description

Symbol	Type	Function
CLK	Input	Clock: All ESDRAM input signals are sampled on the positive edge of CLK.
CKE	Input	Clock Enable: Activates the CLK signal when high and deactivates CLK internally. CKE low initiates the Power Down, Suspend, and Self-Refresh modes.
/CS	Input	Chip Select: Active low /CS enables the command decoder and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
/RAS, /CAS, /WE	Input	Command Inputs: Sampled on the rising edge of CLK, these inputs define the command to be executed.
BA	Input	Bank Address: This input defines to which of the 2 banks a given command is being applied. This address input is also used to program the Mode Registers.
A9-A0	Input	Address Inputs: A9-A0 defines the row address for the Bank Activate command. A7-A0 defines the column address for Read and Write commands. A9/AP invokes the Auto-Precharge operation. During manual Precharge commands, A9/AP low specifies a single bank precharge while A9/AP high precharges all banks. The address inputs are also used to program the Mode Registers.
DQ31-DQ0	Input/ Output	Data I/O: Data bus inputs and outputs. For Write cycles, input data is applied to these pins and must be set-up and held relative to the rising edge of clock. For Read cycles, the device drives output data on these pins after the CAS latency is satisfied.
DQM3-DQM0	Input	Data I/O Mask Inputs: DQM inputs mask write data (zero latency) and acts as a synchronous output enable (2 cycle latency) for read data. In the optional mode set via the Extended Mode Register, output enable latency is one when CAS latency is one.
V_{DD}, V_{SS}	Supply	Power (+3.3V) and ground for the input buffers and core logic.
V_{DDQ}, V_{SSQ}	Supply	Isolated power supply and ground for output buffers. V_{DDQ} may be connected to either 3.3V or 2.5V power.

Mode Register Set (Address Input for Mode Set)



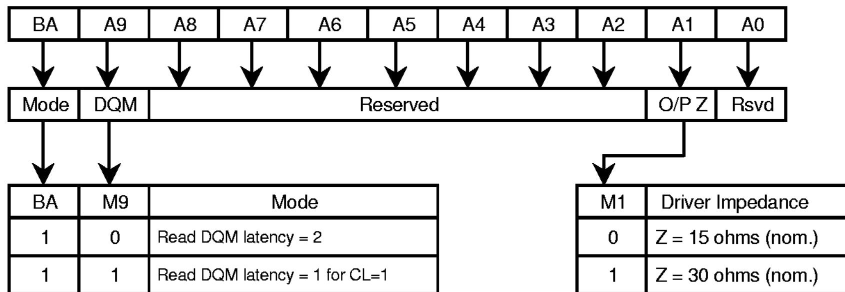
BA	M9	M8	M7	Mode
0	0	0	0	Write Transfer
0	1	0	0	No Write Transfer

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

			Burst Length	
M2	M1	M0	Sequential	Interleaved
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Extended Mode Register Set (Address Input for Mode Set)



BA	M9	Mode
1	0	Read DQM latency = 2
1	1	Read DQM latency = 1 for CL=1

M1	Driver Impedance
0	Z = 15 ohms (nom.)
1	Z = 30 ohms (nom.)

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Value
Power Supply Voltage	V_{DD}	-1V to +4.6V
I/O Power Supply Voltage	V_{DDQ}	-1V to +4.6V, where $V_{DDQ} \leq V_{DD}+1V$
Voltage on any pin with respect to ground	V_{IN}, V_{OUT}	-0.5V to +4.6V
Operating Temperature (ambient)	T_A	0° C to + 70° C
Storage Temperature	T_{stg}	-55° C to + 150° C
Power Dissipation	P_D	1.2W
DC Output Current (I/O pins)	I_{OUT}	50 mA

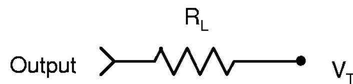
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS (T_A = 0°C to + 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Supply Voltage	3.15	3.3	3.6	V	
V_{DDQ}	I/O Supply Voltage	2.3	-	3.6	V	1
V_{IH1}	Input High Voltage	2.0	3.3	V_{DD} + 0.3	V	2, 3
V_{IL1}	Input Low Voltage	-0.3	0.0	0.8	V	2, 3
V_{IH2}	Input High Voltage	1.7	2.5	V_{DDQ} + 0.3	V	4
V_{IL2}	Input Low Voltage	-0.3	0.0	0.7	V	4
$I_{I(L)}$	Input Leakage Current	-	-	±1	µA	
$I_{O(L)}$	Output Leakage Current	-	-	±1	µA	
V_{OH1}	Output High Voltage (I_{OUT} = -4mA)	2.4	-	-	V	3
V_{OL1}	Output Low Voltage (I_{OUT} = +4mA)	-	-	0.4	V	3
V_{OH2}	Output High Voltage (I_{OUT} = -2mA)	2.0	-	-	V	4
V_{OL2}	Output Low Voltage (I_{OUT} = +2mA)	-	-	0.4	V	4

1. V_{DDQ} must be no more than 0.3V higher than V_{DD}.
2. Applies to all input-only pins regardless of V_{DDQ} voltage.
3. Applies to DQ pins when V_{DDQ}=3.3V.
4. Applies to DQ pins when V_{DDQ}=2.5V.

DC OUTPUT LOAD CIRCUIT



For VDDQ = 3.3V
V_{OH} (DC) =2.4V, I_{OH} = -4mA
V_{OL} (DC) = 0.4V, I_{OL} = 4mA
V_T = 1.4V, R_L = 250Ω

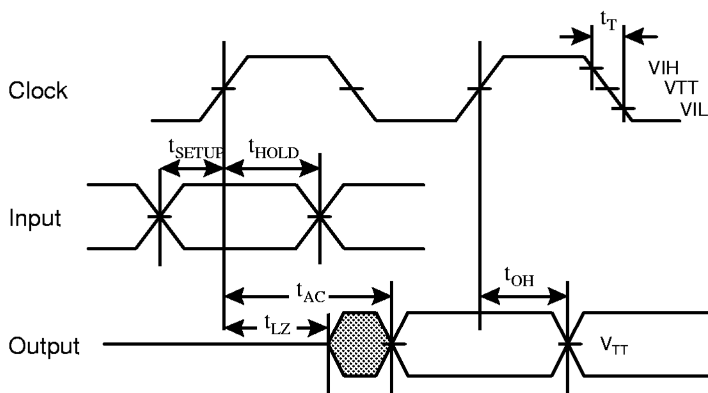
For VDDQ = 2.5V
V_{OH} (DC) =2.0V, I_{OH} = -2mA
V_{OL} (DC) = 0.4V, I_{OL} = 2mA
V_T = 1.2V, R_L = 400Ω

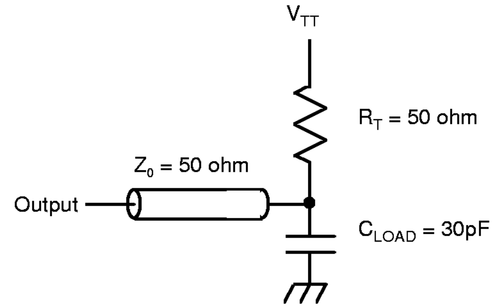
CAPACITANCE (T_A = 25°C, f=1MHz, VDD = 3.3V ±0.3V)

Symbol	Parameter	Min	Typ	Max	Units	Notes
C_{I1}	Input Capacitance (BA, A9-A0)	2.0	2.7	4.0	pF	
C_{I2}	Input Capacitance (All control inputs)	2.0	2.7	4.0	pF	
C_O	Output Capacitance (DQ31-DQ0)	3.0	4.5	5.5	pF	

AC CHARACTERISTICS (T_A = 0°C to + 70°C)

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. For VDDQ = 3.3V, AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the V_{TT} = 1.4V crossover point. For VDDQ = 2.5V, AC timing tests have V_{IL} = 0.7V and V_{IH} = 1.7V with the timing referenced to the V_{TT} = 1.25V crossover point.





AC Output Load Circuit

3. The transition time is measured between V_{IH} and V_{IL} (or between) V_{IL} and V_{IH}).
4. AC measurements assume t_T = 1ns.
5. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

AC OPERATING CONDITIONS (T_A = 0°C to + 70°C)

Symbol	Parameter	-6.6 Min	-6.6 Max	-7.5 Min	-7.5 Max	-10 Min	-10 Max	Units	Notes
Clock and Clock Enable Parameters									
t_{CK2}	Clock Cycle Time, CL = 2, 3	6.6	150MHz	7.5	133MHz	10	100MHz	ns	
t_{CK1}	Clock Cycle Time, CL = 1	13.3	75MHz	15	66MHz	15	66MHz	ns	
t_{AC2}	Clock Access Time, CL = 2, 3	-	4.3	-	4.5	-	5	ns	1, 2
t_{AC1}	Clock Access Time, CL = 1	-	10.5	-	11.0	-	11.5	ns	1,2
t_{CKH2}, t_{CKL2}	Clock High & Low Time (CL=2,3)	2.6	-	2.8	-	3.5	-	ns	3
t_{CKH1}, t_{CKL1}	Clock High & Low Time (CL=1)	4	-	5	-	5	-	ns	3
t_{CKES}	Clock Enable Set-Up Time	2.2	-	2.2	-	2.5	-	ns	
t_{CKEH}	Clock Enable Hold Time	1.0	-	1.0	-	1.0	-	ns	
t_{CKSP}	CKE Set-Up Time (Power down mode)	2.2	-	2.2	-	2.5	-	ns	
t_T	Transition Time (Rise and Fall)	-	4	-	4	-	4	ns	
Common Parameters									
t_{CS}	Command and Address Set-Up Time	2.2	-	2.2	-	2.5	-	ns	
t_{CH}	Command and Address Hold Time	1.0	-	1.0	-	1.0	-	ns	
t_{RCD}	RAS to CAS Delay Time	13.3	-	15	-	15	-	ns	
t_{RC}	Bank Cycle Time	33.3	120K	37.5	120K	45	120K	ns	
t_{RAS}	Bank Active Time	20	120K	22.5	120K	30	120K	ns	
t_{RP}	Precharge Time	13.3	-	15	-	15	-	ns	
t_{RRD}	Bank to Bank Delay Time (Alt. Bank)	13.3	-	15	-	15	-	ns	
t_{CCD}	CAS to CAS Delay Time (Same Bank)	6.6	-	7.5	-	10	-	ns	
Read and Write Parameters									
t_{OH1}	Data Output Hold Time (CL=1)	3.0	-	3.0	-	3.0	-	ns	
t_{OH2}	Data Output Hold Time (CL=2,3)	2.0	-	2.0	-	2.0	-	ns	
t_{LZ}	Data Output to Low-Z Time	0	-	0	-	0	-	ns	
t_{HZ1}	Data Output to High-Z Time (CL=1)	-	7.0	-	7.5	-	8.0	ns	4
t_{HZ2}	Data Output to High-Z Time (CL=2,3)	-	4.3	-	4.5	-	5.0	ns	4
t_{DQZ}	DQM Data Output Disable Time	2	-	2	-	2	-	CLK	
t_{DS}	Data Input Set-Up Time	2.0	-	2.2	-	2.5	-	ns	
t_{DH}	Data Input Hold Time	1.0	-	1.0	-	1.0	-	ns	
t_{DPL}	Data Input to Precharge	6.6	-	7.5	-	10	-	ns	
t_{DAL}	Data Input to ACTV/Refresh	20	-	22.5	-	30	-	ns	5
t_{DQW}	Data Write Mask Latency	0	-	0	-	0	-	CLK	
Refresh Parameters									
t_{REF}	Refresh Period	-	32	-	32	-	32	ms	6, 7
t_{SREX}	Self Refresh Exit Time	2CLK $+t_{RC}$	-	2CLK $+t_{RC}$	-	2CLK $+t_{RC}$	-	ns	8

Notes:

1. Access time is measured at 1.4V (LVTTL) and 1.25V (V_{DDQ}=2.5V). See AC Test Load.
2. Access time is based on a clock rise time of 1ns. If clock rise time is longer than 1ns, then (t_{rise}/2-0.5)ns must be added to the access time.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, other AC timing parameters must be compensated by an additional [(t_{rise}+t_{fall})/2-1]ns.
4. Referenced to the time at which the output achieves an open circuit condition.
5. t_{DAL} is equal to t_{DPL} + t_{RP}.
6. 2048 cycles.
7. Any time that the refresh period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to "wake up" the device.
8. Self Refresh exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not completed until t_{RC} is satisfied once the Self Refresh Exit command is registered.

ORDERING INFORMATION

Part Number	CAS Latencies	I/O Width	I/O Type	Package	Power Supply	Maximum Operating Frequency (MHz)
SM2405Q-6.6	1, 2, 3	x32	LVTTL, 2.5V	100 pin LQFP	3.3V	150
SM2405Q-7.5	1, 2, 3	x32	LVTTL, 2.5V	100 pin LQFP	3.3V	133
SM2405Q-10	1, 2, 3	x32	LVTTL, 2.5V	100 pin LQFP	3.3V	100

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