HM11S220

240-Output LCD Segment/Common Driver IC

AUGUST. 2000.

VER 0.0

Hynix Semiconductor, Inc.

HM11S220 Specification revision history		
Version	Content	Date
0.0	1. New documentation	Aug. 2000

CONTENTS

1. INTRODUCTION

The HM11S220 is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels. Through the use of SST(Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The HM11S220 is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

2. FEATURES

-Number of LCD drive outputs : 240
-Supply voltage for LCD drive : +15.0 to +40.0V
-Supply voltage for the logic system : +2.4 to +5.5V
-Low power consumption
-Low output impedance
-Package : Super slim TCP (Tape Carrier Package)/Au Bumped chip

[Segment mode]

-. Shift clock frequency : 20MHz(V_{DD} = +5.0V ~ +5.5V)
15MHz(V_{DD} = +3.0V ~ +4.5V)
12MHz(V_{DD} = +2.4V ~ +3.0V)
-. Adopts a data bus system
-. 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
-. Automatic transfer function of an enable signal
-. Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
-. Line latch circuits are reset when DISPOFFB active

[Common mode]

-. Shift clock frequency : 4 MHz(MAX, V_{DD} = +2.4V ~ +5.5V)
-. Built-in 240-bit bi-directional shift register
-. Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register X 2)
① $Y_1 \rightarrow Y_{240}$ Single mode
② $Y_{240} \rightarrow Y_1$ Single mode
③ $Y_1 \rightarrow Y_{120}$, $Y_{121} \rightarrow Y_{240}$ Dual mode
④ $Y_{240} \rightarrow Y_{121}$, $Y_{120} \rightarrow Y_1$ Dual mode
The above 4 shift directions are pin-selectable
-. Shift register circuits are reset when DISPOFFB active

3. BLOCK DIAGRAM

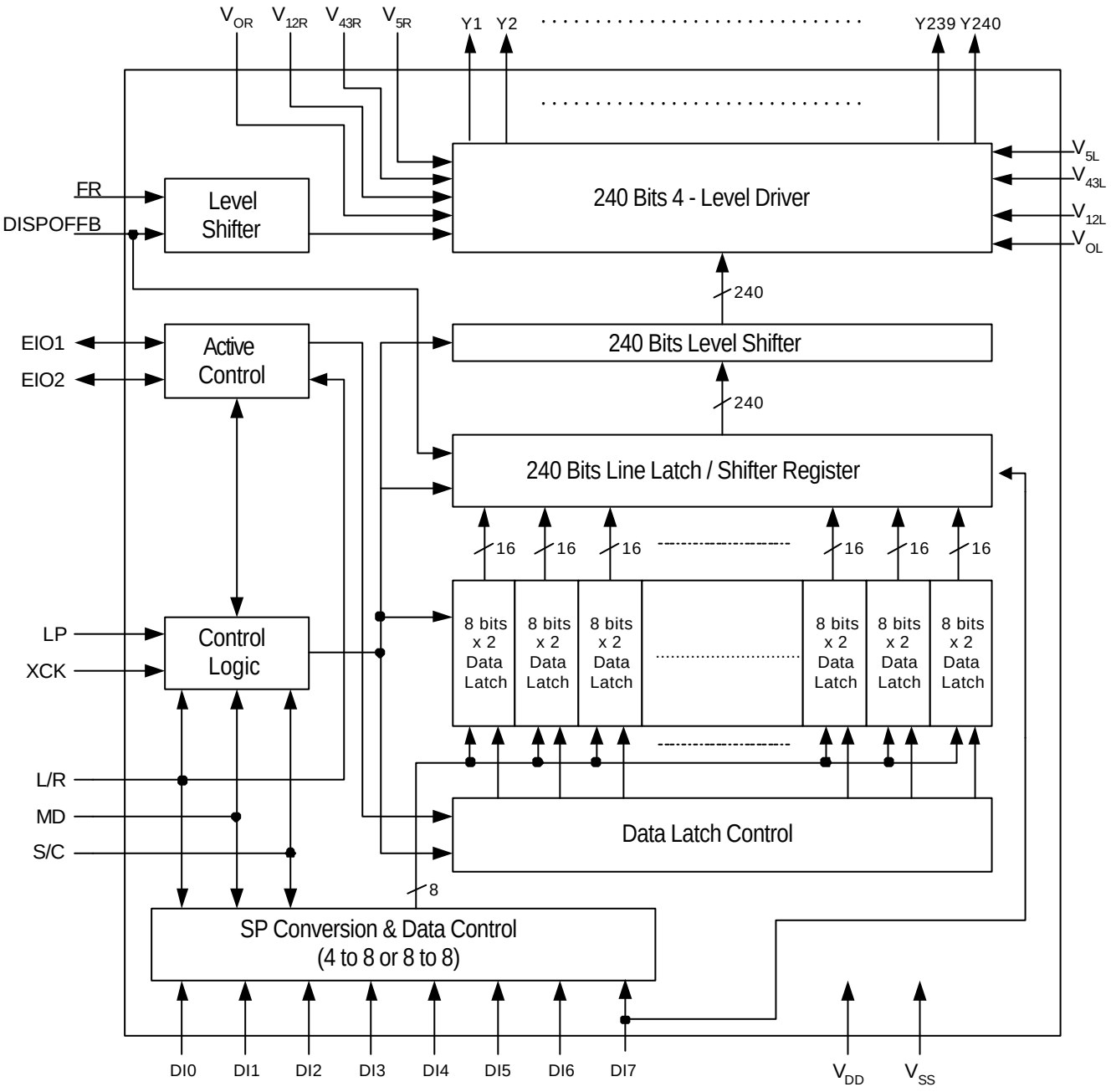


Figure 3-1. block diagram

4. PIN DESCRIPTION

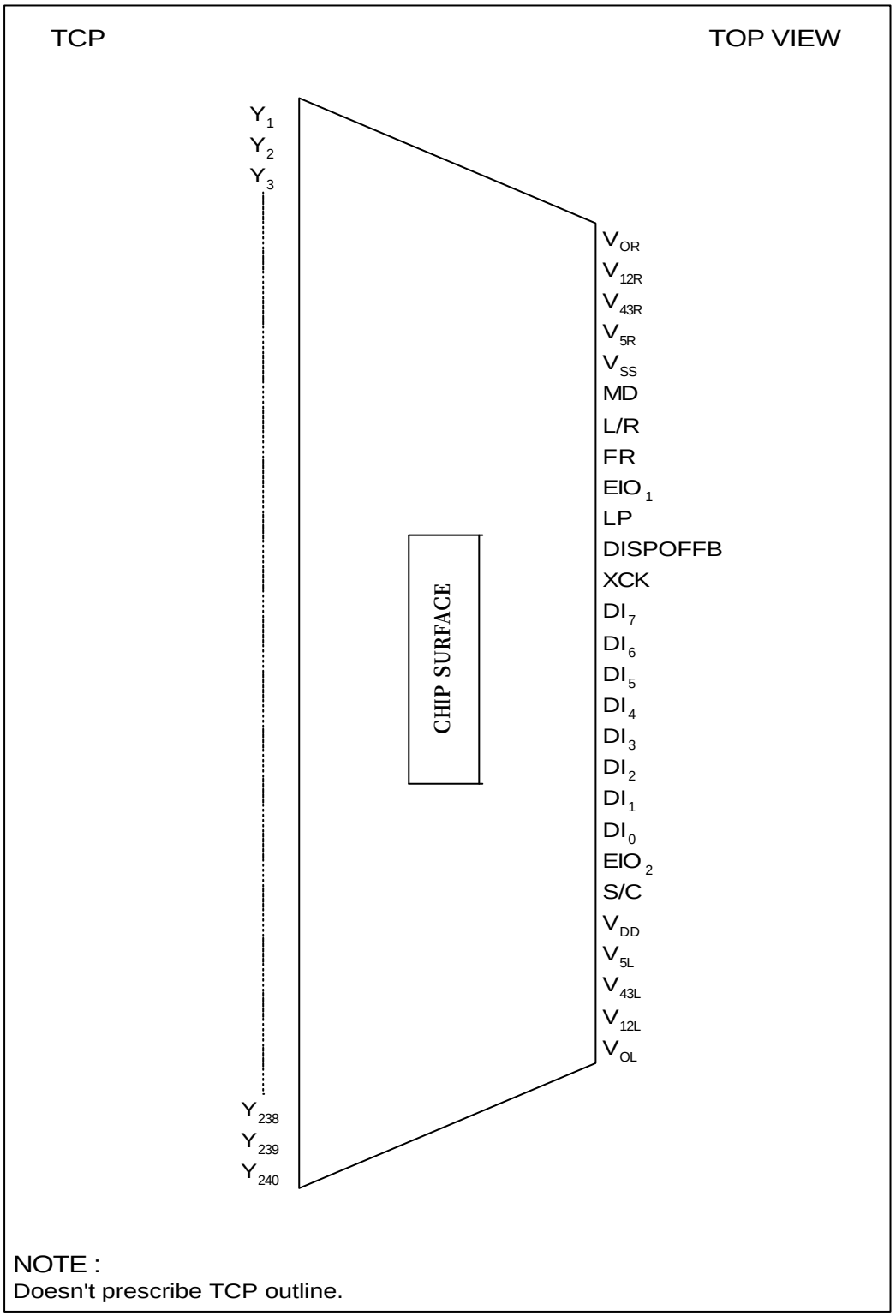
4-1. Pin Description

Table 4-1. Pin description

SYMBOL	I/O	DESCRIPTION
Y1 – Y240	O	LCD drive output
V0L, V0R	-	Power supply for LCD drive
V12L, V12R	-	Power supply for LCD drive
V43L, V43R	-	Power supply for LCD drive
V5L, V5R	-	Power supply for LCD drive
L/R	I	Input for selecting the reading direction of display data at segment mode/ Input for selecting the shift direction of shift register at common mode
VDD	-	Power supply for logic system (+2.4 to +5.5V)
S/C	I	Segment mode/common mode selection
EIO2, EIO1	I/O	Input/output for chip selection at segment mode/ Shift data input/output for shift register at common mode
DI0-DI6	I	Display data input at segment mode
DI7	I	Display data input at segment mode/Dual mode data input at common mode
XCK	I	Clock input for taking display data at segment mode
DISPOFFB	I	Control input for output of non-select level
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
FR	I	AC-converting signal input for LCD drive waveform
MD	I	Mode selection input
VSS	-	Ground(0 V)

4-2. Pin Connections

****Not fixed**



5. FUNCTIONAL DESCRIPTION

5-1. Pin Functions

Table 5-1. Pin Functions(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin. (+2.4V to +5.5V)
V_{SS}	Ground pin. (0V)
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage. -Normally use the bias voltages set by a resistor divider. -Ensure that voltages are set such that Vss $\leq$ V_5 < V_{43} < V_{12} < V_0 -$V_{0L(R)}$, $V_{12L(R)}$, $V_{43L(R)}$, $V_{5L(R)}$ must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
DI_7-DI_0	Input pins for display data. -In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0. Connect DI_7-DI_4 to Vss or V_{DD}. -In 8-bit parallel input mode, input data into the 8 pins, DI_7-DI_0.
XCK	Clock input pin for taking display data. -Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data. -Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data. -When set to Vss level "L", data is read sequentially from Y_{240} to Y_1. -When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{240}.
DISPOFFB	Control input pin for output of non-select level. -The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. -When set to Vss level "L", the LCD drive output pins(Y_1-Y_{240})are set to level V_5. -When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of DISPOFFB. When the DISPOFFB function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if DISPOFFB removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly.
FR	AC signal input pin for LCD drive waveform. -The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. -Normally it inputs a frame inversion signal. -The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal.
MD	Mode selection pin. -When set to V_{SS} level "L", 8-bit parallel input mode is set. -When set to V_{DD} level "H", 4-bit parallel input mode is set.
S/C	Segment mode/common mode selection pin. -When set to V_{DD} level "H", segment mode is set.
EIO_1, EIO_2	Input/output pins for chip selection. -When L/R input is at Vss level "L", EIO_1 is set for output, and EIO_2 is set for input. -When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. -During output, set to "H" while LP XCK is "H" and after 240 bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". -During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 240 bits of data have been read.

Table 5-2. Pin Functions (Common mode)

SYMBOL	FUNCTION
Y_1-Y_{240}	LCD drive output pins. -Corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output.
V_{DD}	Logic system power supply pin.(+2.4 to +5.5V)
V_{SS}	Ground pin. (0V)
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage. -Normally use the bias voltages set by a resistor divider. -Ensure that voltages are set such that Vss $\leq$ V_5 < V_{43} < V_{12} < V_0. -$V_{0L(R)}$, $V_{12L(R)}$, $V_{43L(R)}$, $V_{5L(R)}$ must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
EIO_1	Shift data input/output pin for bi-directional shift register. -Output pin when L/R is at Vss level "L", input pin when L/R is at V_{DD} level "H". -When L/R = H, EIO_1 is used as input pin, it will be pulled down. -When L/R = L, EIO_1 is used as output pin, it won't be pulled down.
EIO_2	Shift data input/output pin for bi-directional shift register. -Input pin when L/R is at Vss level "L", output pin when L/R is at V_{DD} level "H". -When L/R = L, EIO_2 is used as input pin, it will be pulled down. -When L/R = H, EIO_2 is used as output pin, it won't be pulled down.
LP	Shift clock pulse input pin for bi-directional shift register. -Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register. -Data is shifted from Y_{240} to Y_1 when set to Vss level "L", and data is shifted from Y_1 to Y_{240} when set to V_{DD} level "H".
DISPOFFB	Control input pin for output of non-select level. -The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. -When set to Vss level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level V_5. -When set to "L", the contents of the shift register are reset to not reading data. When the DISPOFFB function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if DISPOFFB removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly.
FR	AC signal input pin for LCD drive waveform. -The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. -Normally it inputs a frame inversion signal. -The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal.
MD	Mode selection pin -When set to Vss level "L", single mode is selected, when set to V_{DD} level "H", dual mode is selected.

SYMBOL	FUNCTION
DI_7	Dual mode data input pin. -According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down.
S/C	Segment mode/common mode selection pin. -When set to Vss level "L", common mode is set.
DI_6-DI_0	Not used. -Connect DI_6-DI_0 to Vss or V_{DD}, avoiding floating.
XCK	Not used. -XCK is pulled down in common mode, so connect to Vss or open.
Y_1-Y_{240}	LCD drive output pins. -Corresponding directly to each bit of the shift register, one level(V_0, V_{12}, V_{43}, or V_5) is selected and output.

5-2. Functional Operations of each block

Table 5-3. Functional operations of each block

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit, after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control, 240 bits of data are read in 30 sets of 8 bits
Line Latch/ Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V_0, V_{12}, V_{43}, or V_5) based on the S/C, FR and DISPOFFB signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

5-3. Functional Operations

a. LCD drive output voltage level

(Segment Mode)

FR	LATCH DATA	DISPOFFB	LCD DRIVE OUTPUT VOLTAGE LEVEL(Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

(Common Mode)

FR	LATCH DATA	DISPOFFB	LCD DRIVE OUTPUT VOLTAGE LEVEL(Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Notes : - Vss $\leq$ V5 < V43 < V12 < V0, L : Vss(0 V), H : VDD(+2.4 to +5,5V), X : Don't care
-"Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
Supply regular voltage which is assigned by specification for each power pin.

b. Relationship between the display data and LCD drive output pins

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
					1st	2nd	3rd	..	58th	59th	60th
H	L	Output	Input	DI0	Y237	Y233	Y229	..	Y9	Y5	Y1
				DI1	Y238	Y234	Y230	..	Y10	Y6	Y2
				DI2	Y239	Y235	Y231	..	Y11	Y7	Y3
				DI3	Y240	Y236	Y232	..	Y12	Y8	Y4
H	H	Input	Output	DI0	Y4	Y8	Y12	..	Y232	Y236	Y240
				DI1	Y3	Y7	Y11	..	Y231	Y235	Y239
				DI2	Y2	Y6	Y10	..	Y230	Y234	Y238
				DI3	Y1	Y5	Y9	..	Y229	Y233	Y237

(b) 8-bit Parallel Input Mode

MD	L/R	EIO1	EIO2	DATA INPUT	NUMBER OF CLOCKS						
					1st	2nd	3rd	..	28th	29th	30th
L	L	Output	Input	DI0	Y233	Y225	Y217	..	Y17	Y9	Y1
				DI1	Y234	Y226	Y218	..	Y18	Y10	Y2
				DI2	Y235	Y227	Y219	..	Y19	Y11	Y3
				DI3	Y236	Y228	Y220	..	Y20	Y12	Y4
				DI4	Y237	Y229	Y221	..	Y21	Y13	Y5
				DI5	Y238	Y230	Y222	..	Y22	Y14	Y6
				DI6	Y239	Y231	Y223	..	Y23	Y15	Y7
				DI7	Y240	Y232	Y224	..	Y24	Y16	Y8
L	H	Input	Output	DI0	Y8	Y16	Y24	..	Y224	Y232	Y240
				DI1	Y7	Y15	Y23	..	Y223	Y231	Y239
				DI2	Y6	Y14	Y22	..	Y222	Y230	Y238
				DI3	Y5	Y13	Y21	..	Y221	Y229	Y237
				DI4	Y4	Y12	Y20	..	Y220	Y228	Y236
				DI5	Y3	Y11	Y19	..	Y219	Y227	Y235
				DI6	Y2	Y10	Y18	..	Y218	Y226	Y234
				DI7	Y1	Y9	Y17	..	Y217	Y225	Y233

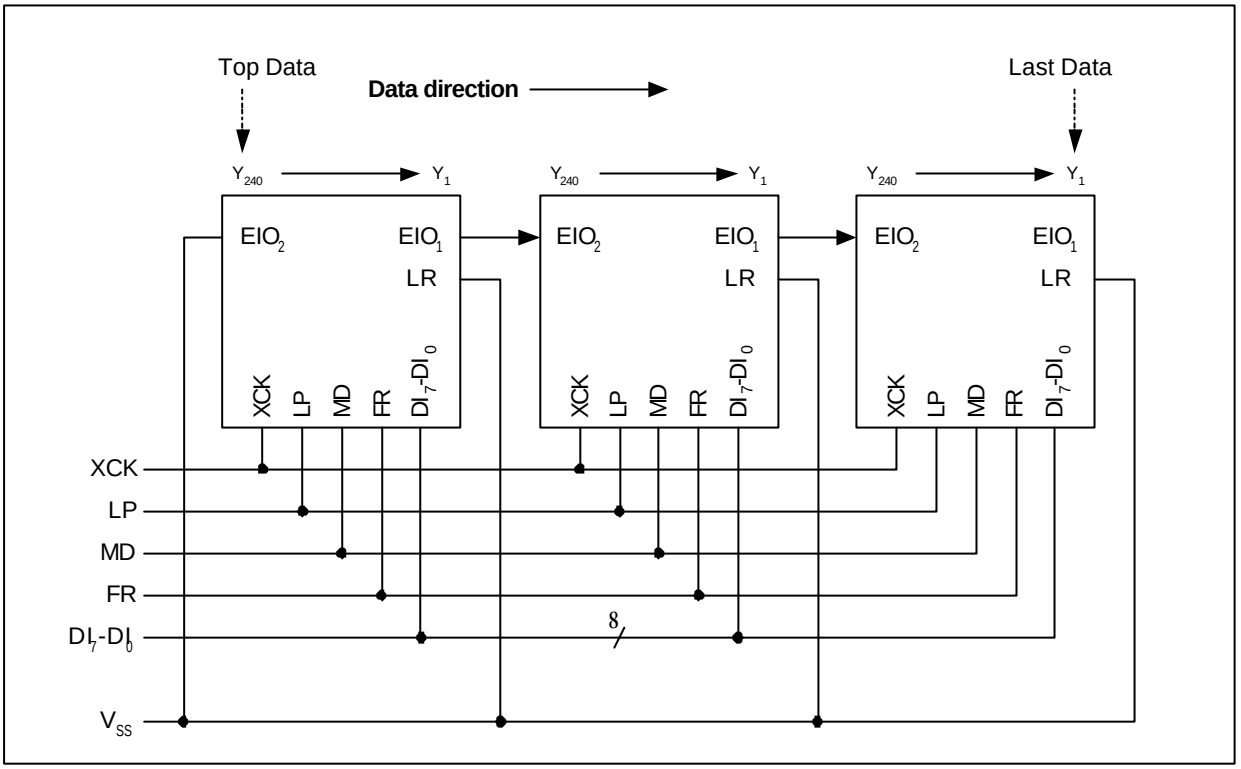
(Common Mode)

MD	L/R	DATA TRANSFER DIRECTION	EIO1	EIO2	DI7
L (Single)	L	Y240 → Y1	Output	Input	X
	H	Y1 → Y240	Input	Output	X
H (Dual)	L	Y240 → Y121 Y120 → Y1	Output	Input	Input
	H	Y1 → Y120 Y121 → Y240	Input	Output	Input

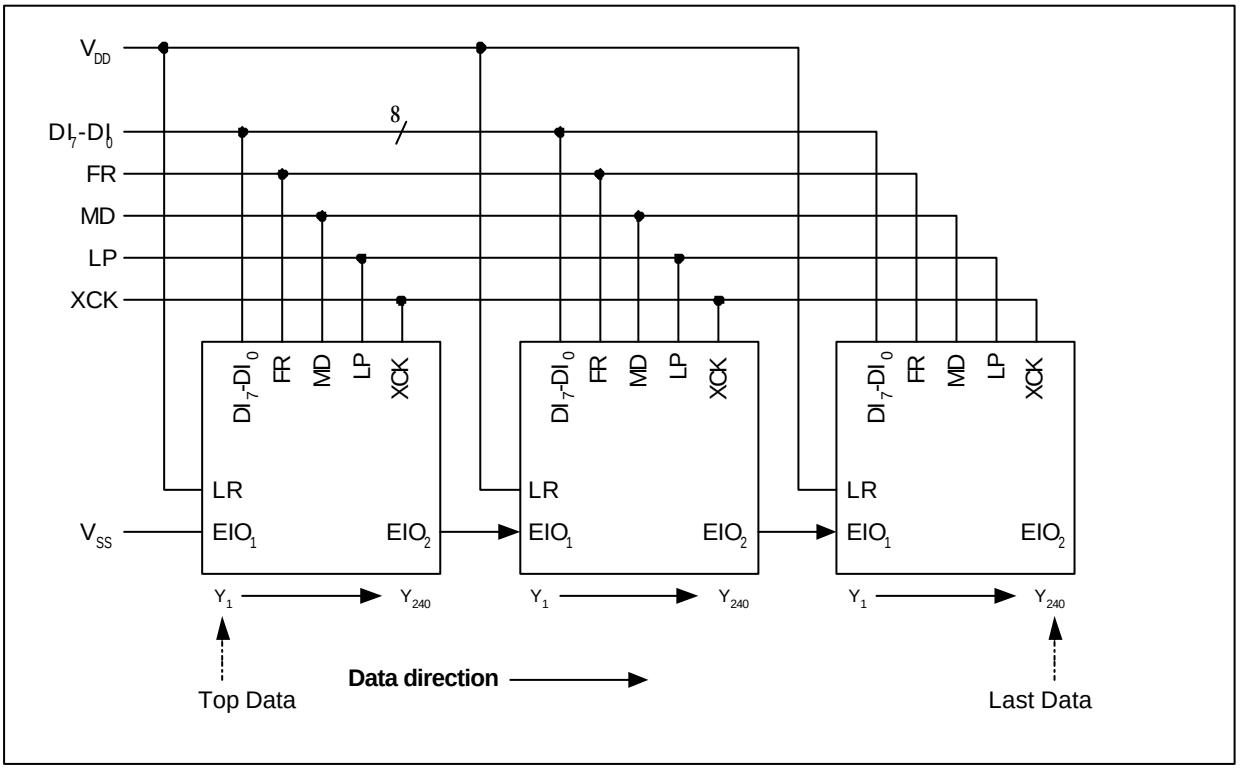
Notes : - L : Vss(0 V), H : VDD (+2.4 to +5.5V), X : Don't care.
- "Don't care" should be fixed to "H" or "L", avoiding floating.

c. Connection examples of cascade segment drivers

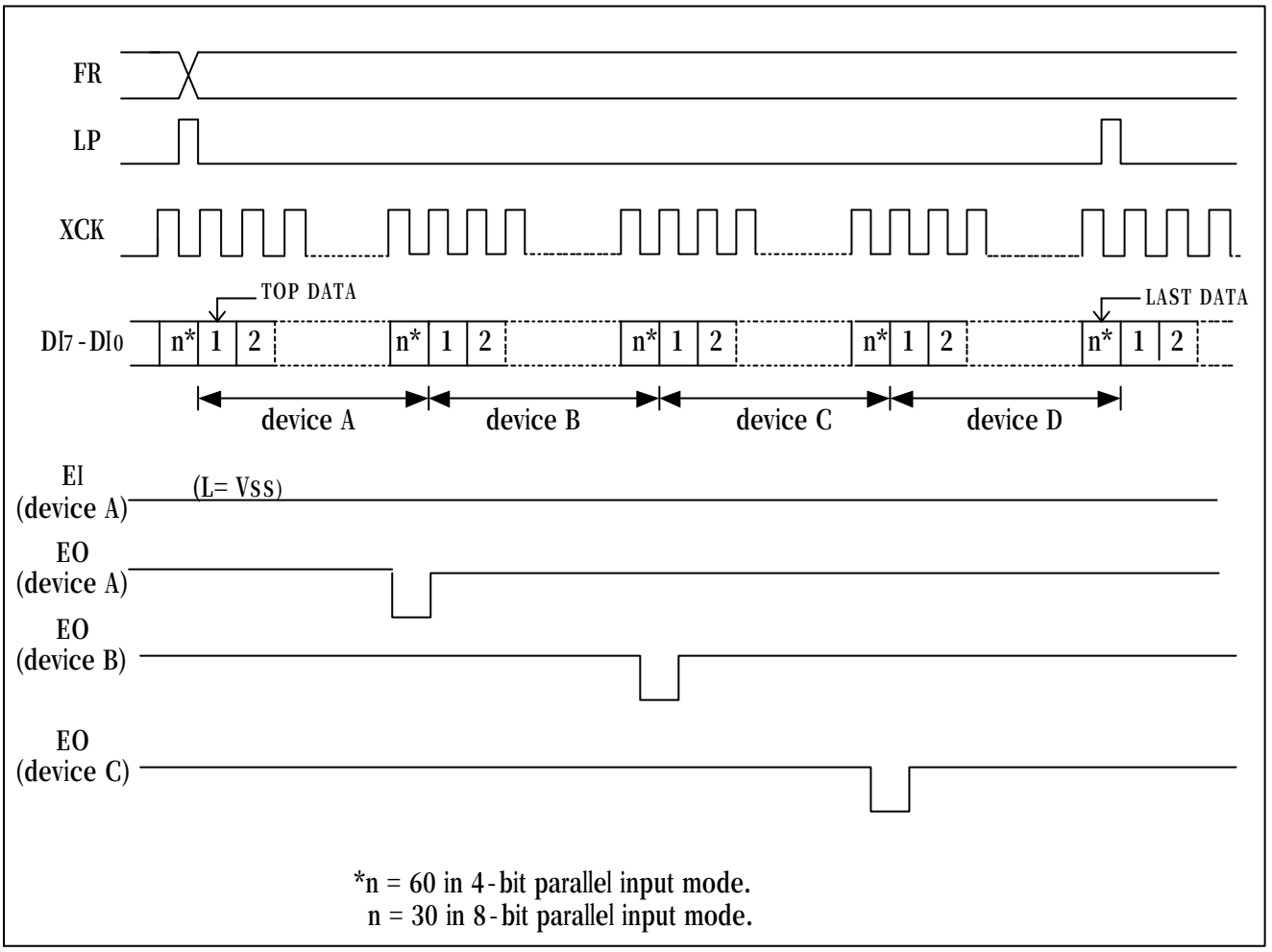
(a) When L/R ="L"



(b) When L/R ="H"



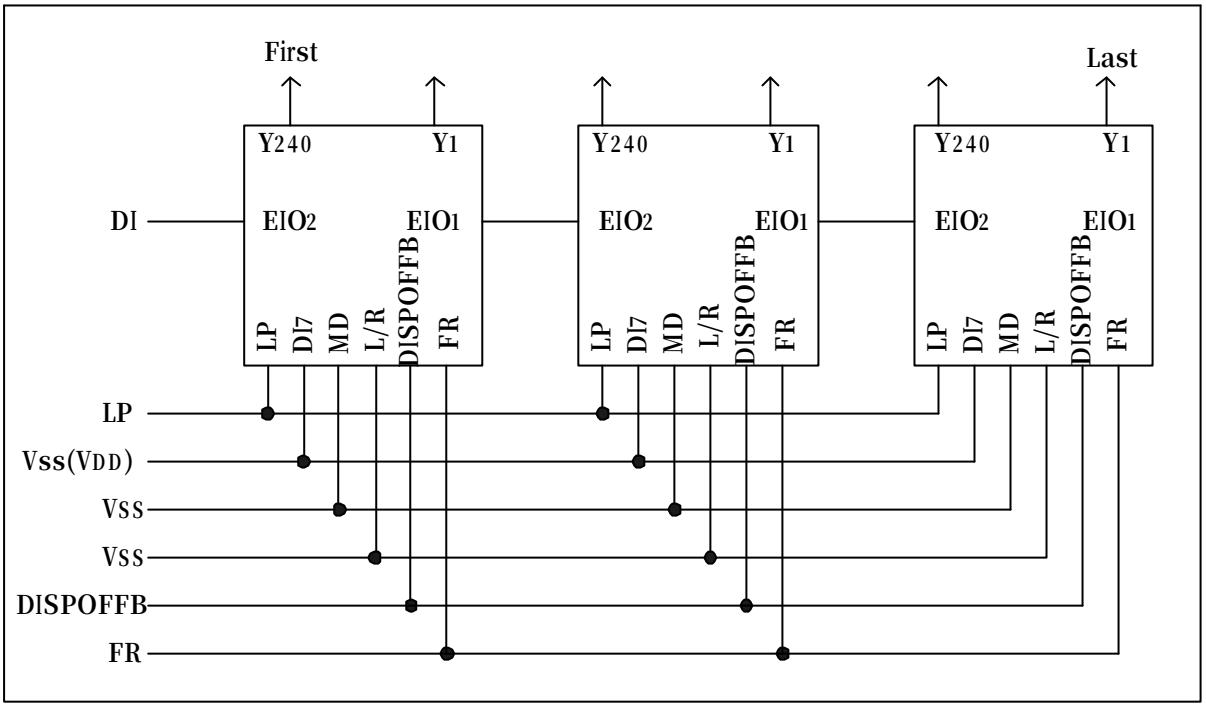
d. Timing chart of 4-device cascade connection of segment drivers



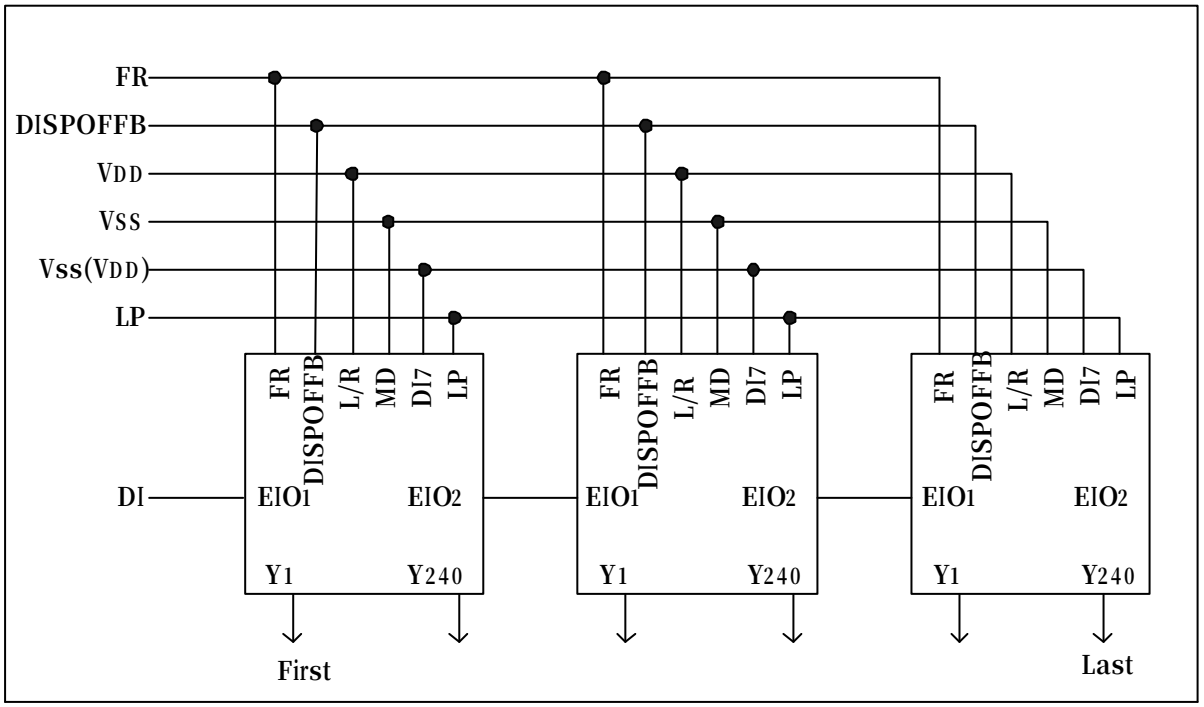
*n = 60 in 4-bit parallel input mode.
n = 30 in 8-bit parallel input mode.

e. Connection examples of cascade common drivers

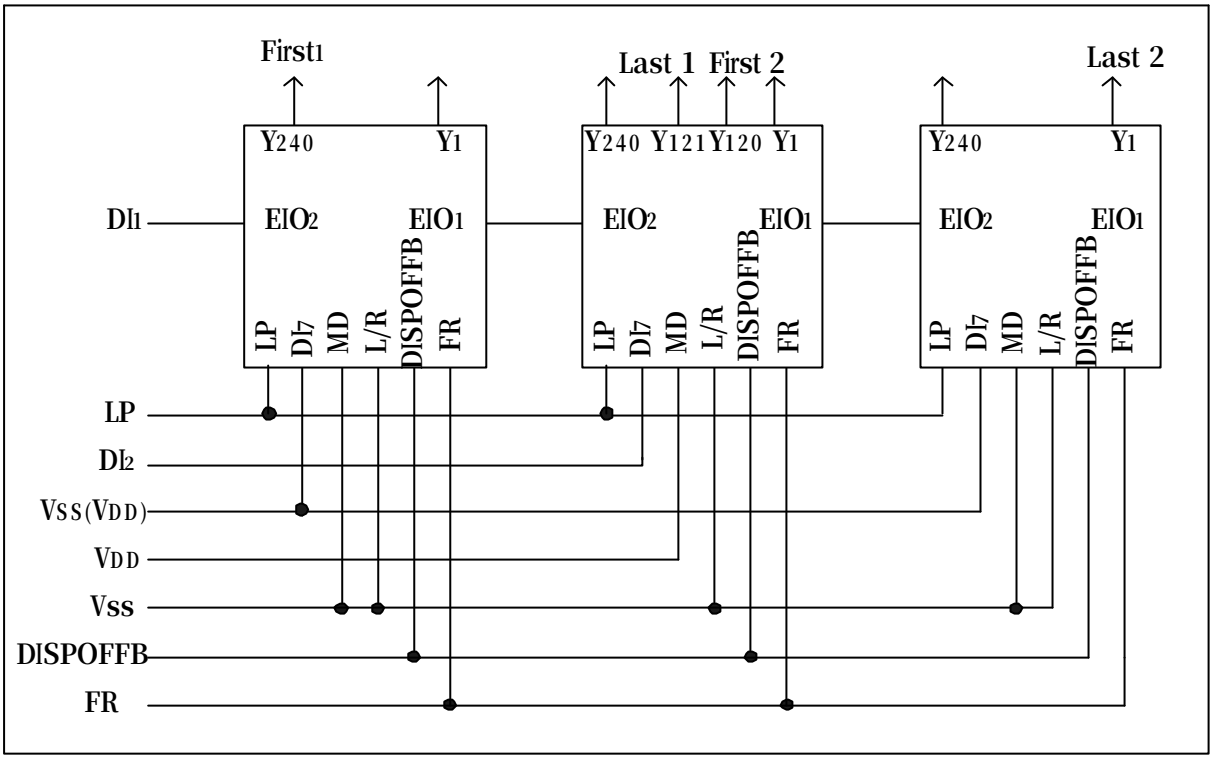
(a) Single Mode (L/R = " L")



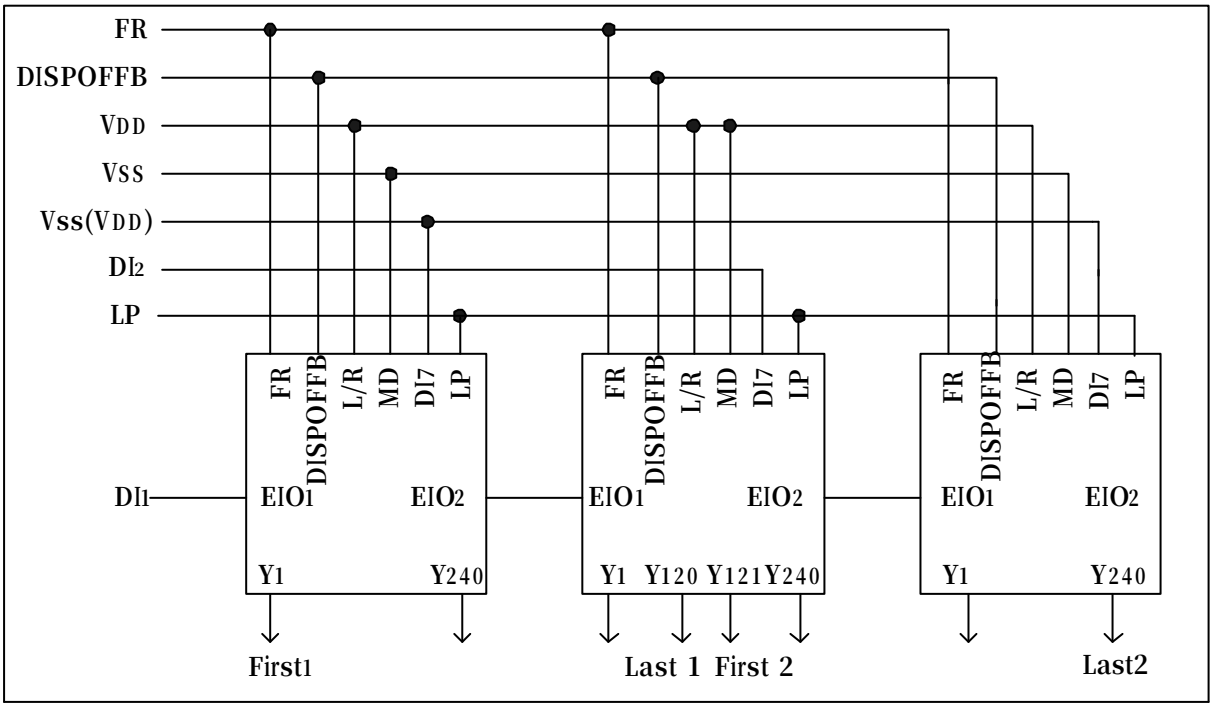
(b) Single Mode(L/R = " H")



(c) Dual Mode (L/R = "L")



(d)Dual Mode(L/R = "H")



5-4. Precautions

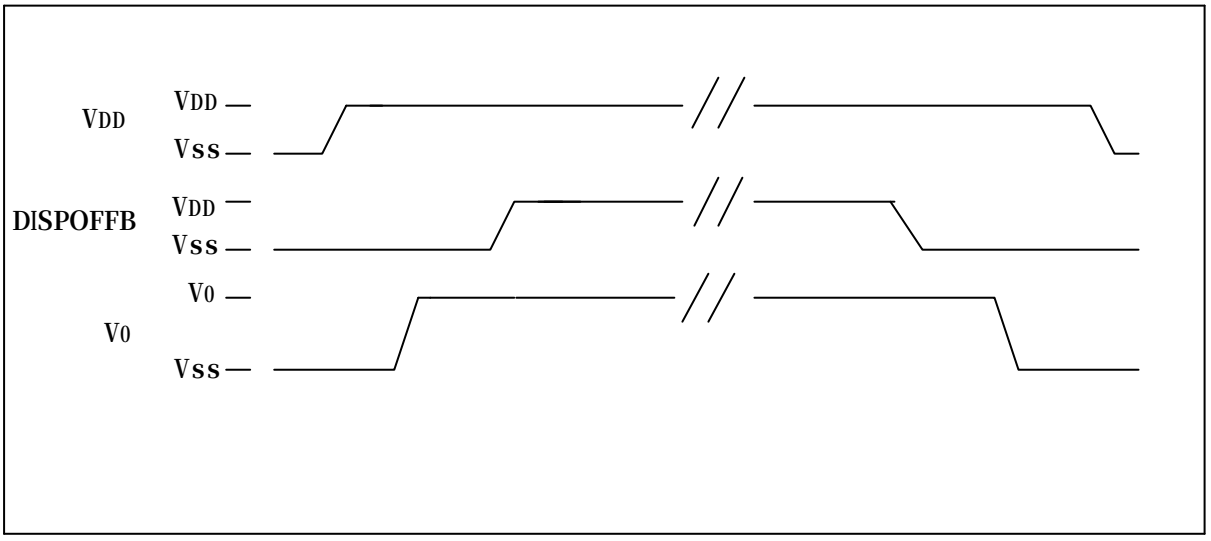
-Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

-When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.

-It is advisable to connect the serial resistor (50 to 100Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on DISPOFFB function. After that, cancel the DISPOFFB function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_5 on DISPOFFB function. Then, disconnect the logic system power after disconnecting the LCD drive power. When connecting the power supply, follow the recommended sequence shown here.



6. SPECIFICATIONS

6-1. Absolute Maximum Ratings

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage(1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 to +45.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to V_0 + 0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to V_0 + 0.3	V	
	V_5	V_{5L}, V_{5R}	-0.3 to V_0 + 0.3	V	
Input voltage	V_I	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1 EIO_2, DISPOFFB	-0.3 to V_{DD}+ 0.3	V	
Storage temperature	T_{STG}		-45 to +125	℃	

Notes : 1. T_a = +25℃
2. The maximum applicable voltage on any pin with respect to Vss(0 V)

6-2. Recommended Operating Conditions

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.4		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+42.0	V	
Operating temperature	T_a		-30		+85	℃	

Notes : 1. The applicable voltage on any pin with respect to Vss (0 V)
2. Ensure that voltage are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$

6-3. Electrical Characteristics

a. DC Characteristics

(Segment Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.4 to +5.5V, V_0 = +15.0 to +42.0 V, T_a = -30 to +85℃)

PARAMETER	SYMBOL	CONDITIONS		APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input " LOW" voltage	V_{IL}			DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, DISPOFFB,			0.2V_{DD}	V	
Input " HIGH" voltage	V_{IH}				0.8V_{DD}			V	
Output " LOW" voltage	V_{OL}	I_{OL}=+0.4mA		EIO_1, EIO_2			+0.4	V	
Output " HIGH" voltage	V_{OH}	I_{OH}=-0.4mA			V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = Vss		DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, DISPOFFB			-10.0	μA	
	I_{LIH}	V_I = V_{DD}					+10.0	μA	
Output resistance	R_{ON}	$\lvert\triangle V_{ON}\rvert$ =0.5V	V0=40V	Y1-Y240		1.0	1.5	kΩ	
			V0=30V			1.5	2.0		
			V0=20V			2.0	2.5		
Standby current	I_{STB}			Vss			75.0	μA	1
Supply current(1) (Non-selection)	I_{DD1}			V_{DD}			2.0	mA	2
Supply current(2) (Selection)	I_{DD2}			V_{DD}			12.0	mA	3
Supply current(3)	I_0			V_{0L}, V_{0R}			1.5	mA	4

Notes : 1. V_{DD} = +5.0 V, V_0 = +40.0 V, V_I = Vss.
2. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 20MHz, no-load, E_I = V_{DD}.
The input data is turned over by data taking clock(4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK}= 20MHz, no-load, E_I = Vss.
The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 20MHz, f_{LP} = 41.6kHz, f_{FR} = 80Hz, no-load.
The input data is turned over by data taking clock(4-bit parallel input mode).

(Common Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.4 to +5.5V, V_0 = +15.0 to +42.0 V, T_a = -30 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "LOW" voltage	V_{IL}			DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, DISPOFFB,			0.2V_{DD}	V	
Input "HIGH" voltage	V_{IH}				0.8V_{DD}			V	
Output "LOW" voltage	V_{OL}	I_{OL}=+0.4mA		EIO_1, EIO_2			+0.4	V	
Output "HIGH" voltage	V_{OH}	I_{OH}=-0.4mA			V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = V_{SS}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, DISPOFFB			-10.0	µA	
	I_{LIH}	V_I = V_{DD}					+10.0	µA	
Input pull-down current	I_{PD}	V_I = V_{DD}		DI_7,XCK,EIO_1,EIO_2			100.0	µA	
Output resistance	R_{ON}	$I\triangle V_{ON}$ =0.5V	V0=40V	Y_1-Y_{240}		1.0	1.5	kΩ	
			V0=30V			1.5	2.0		
			V0=20V			2.0	2.5		
Standby current	I_{STB}			V_{SS}			75.0	µA	1
Supply current(1)	I_{DD}			V_{DD}			120.0	µA	2
Supply current(2)	I_0			V_{0L}, V_{0R}			240.0	µA	2

Notes : 1. V_{DD} = +5.0 V, V_0 = +40.0 V, V_I = V_{SS}.
2. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{LP} = 41.6 kHz, f_{FR}= 80Hz, 1/480 duty operation, no-load.

b. AC Characteristics

(Segment Mode 1) (Vss = V_5 = 0 V, V_{DD} = +5.0 to +5.5 V, V_0 = +15.0 to +40.0V, Ta= -30 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	twck	t_R, t_F ≤ 10ns	50			ns	1
Shift clock "H" pulse width	tWCKH		15			ns	
Shift clock "L" pulse width	tWCKL		15			ns	
Data setup time	tDS		10			ns	
Data hold time	tDH		12			ns	
Latch pulse "H" pulse width	tWLPH		15			ns	
Shift clock rise to latch pulse rise time	tLD		0			ns	
Shift clock fall to latch pulse fall time	tSL		30			ns	
Latch pulse rise to shift clock rise time	tLS		25			ns	
Latch pulse fall to shift clock fall time	tLH		25			ns	
Enable setup time	ts		10			ns	
Input signal rise time	tR				50	ns	2
Input signal fall time	tF				50	ns	2
DISPOFFB removal time	tSD		100			ns	
DISPOFFB "L" pulse width	tWDL		1.2			µs	
Output delay time(1)	tD	C_L = 15 pF			30	ns	
Output delay time(2)	tPD1, tPD2	C_L = 15 pF			1.2	µs	
Output delay time(3)	tPD3	C_L = 15 pF			1.2	µs	

Notes : 1. Takes the cascade connection into consideration
2. (twCK - twCKH – twCKL)/2 is maximum in the case of high speed operation.

(Segment Mode 2) (Vss = V_5 = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = +15.0 to +40.0V, T_a= -30 to +85℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	Twck	t_R, t_F ≤ 10ns	66			ns	1
Shift clock "H" pulse width	T_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	ts		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFFB removal time	t_{SD}		100			ns	
DISPOFFB "L" pulse width	t_{WDL}		1.2			µs	
Output delay time(1)	t_D	C_L = 15 pF			41	ns	
Output delay time(2)	t_{PD1}, t_{PD2}	C_L = 15 pF			1.2	µs	
Output delay time(3)	t_{PD3}	C_L = 15 pF			1.2	µs	

Notes : 1. Takes the cascade connection into consideration
2. (t_{WCK} - t_{WCKH} – t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (Vss = V_5 = 0 V, V_{DD} = +2.4 to +3.0 V, V_0 = +15.0 to +40.0V, Ta= -30 to +85℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, $t_F \leq$ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		65			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFFB removal time	t_{SD}		100			ns	
DISPOFFB "L" pulse width	t_{WDL}		1.2			µs	
Output delay time(1)	t_D	C_L = 15 pF			57	ns	
Output delay time(2)	t_{PD1}, t_{PD2}	C_L = 15 pF			1.2	µs	
Output delay time(3)	t_{PD3}	C_L = 15 pF			1.2	µs	

Notes : 1. Takes the cascade connection into consideration
2. (t_{WCK} - t_{WCKH} – t_{WCKL})/2 is maximum in the case of high speed operation.

6-4. Timing Chart of Segment Mode

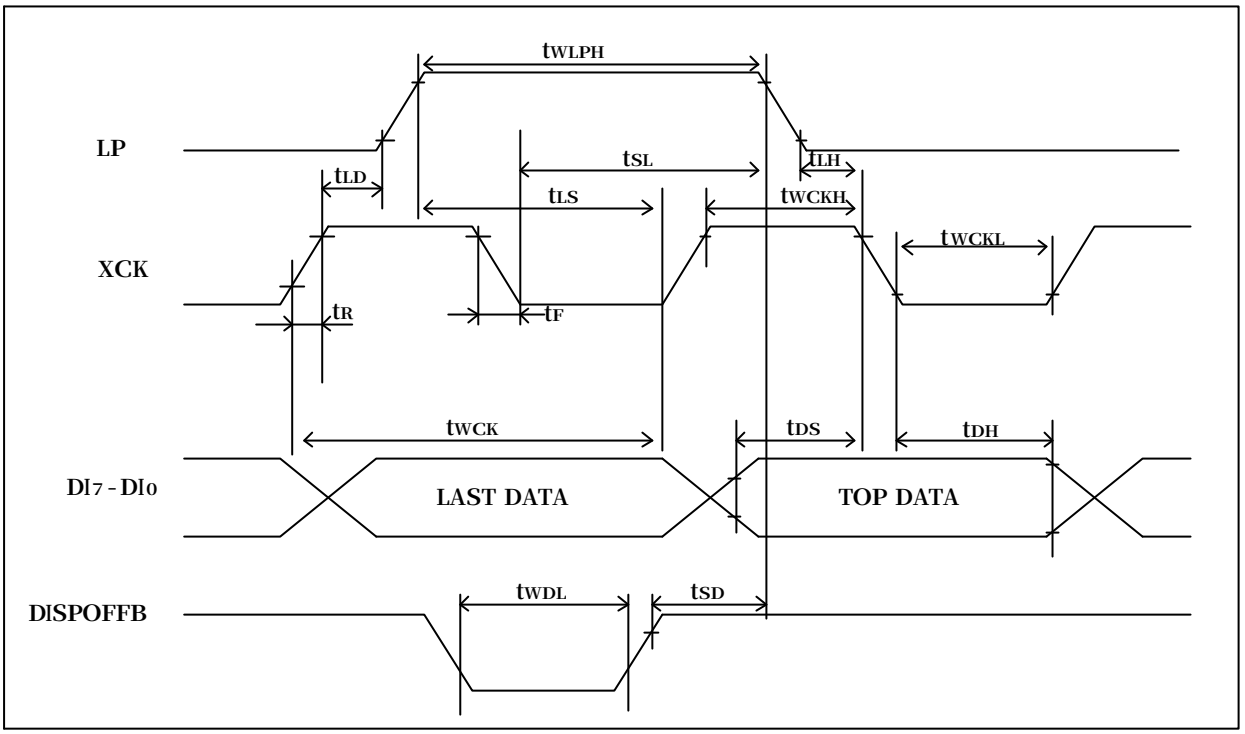


Fig. 6 Timing Characteristics (1)

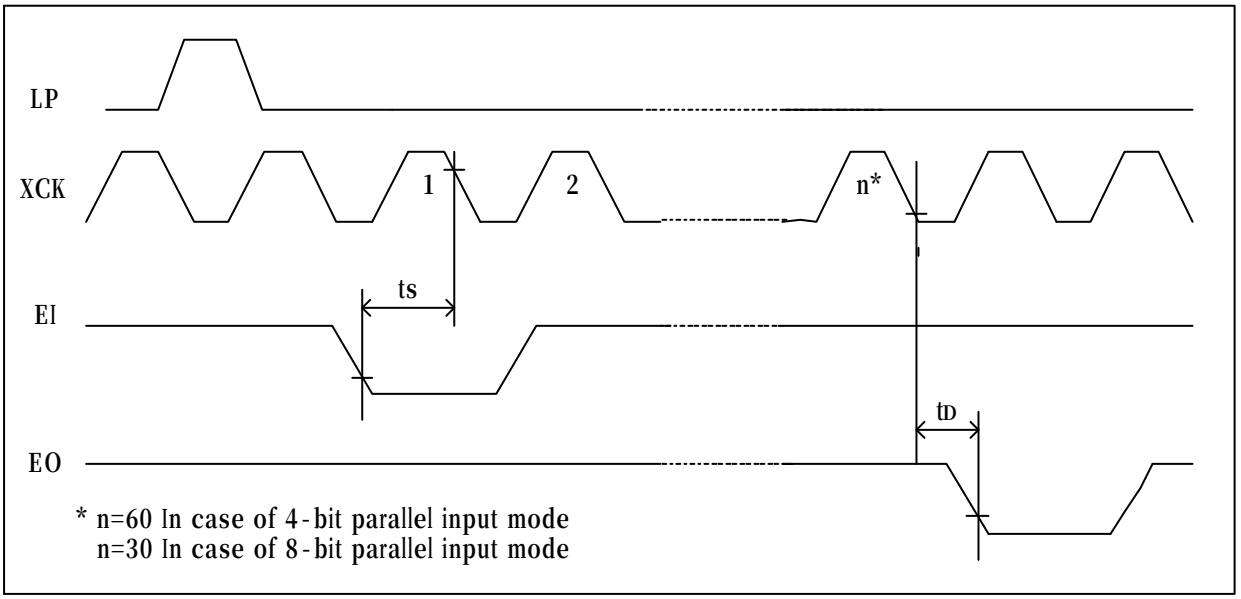


Fig. 7 Timing Characteristics (2)

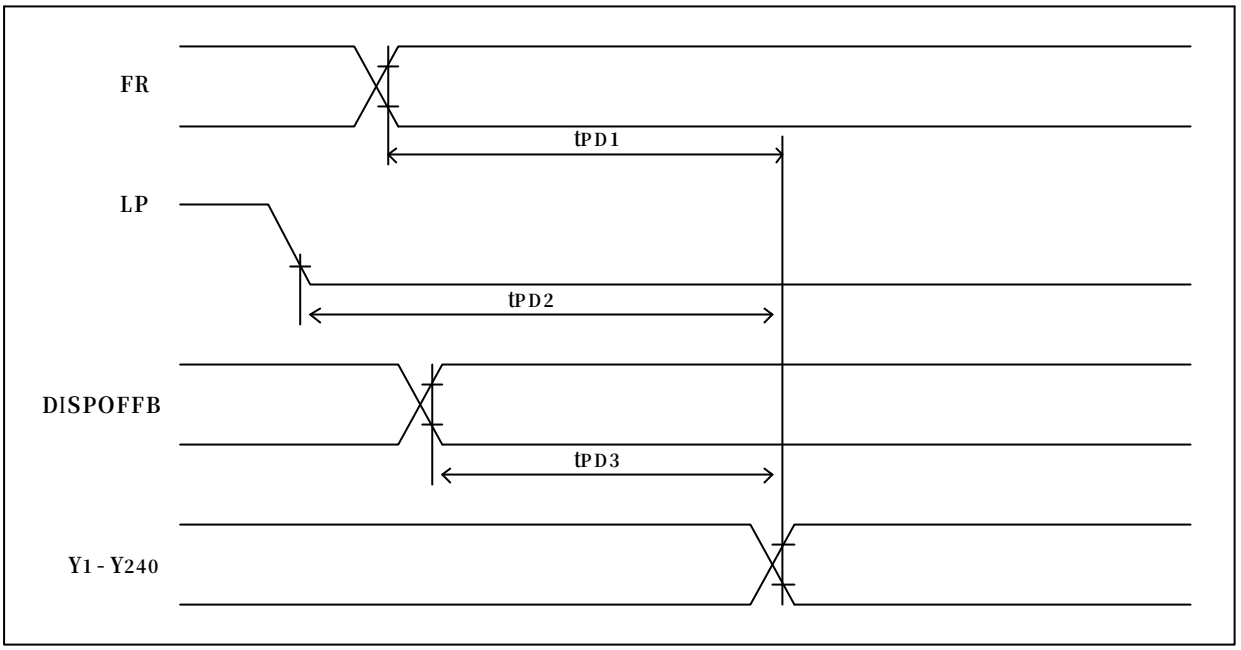
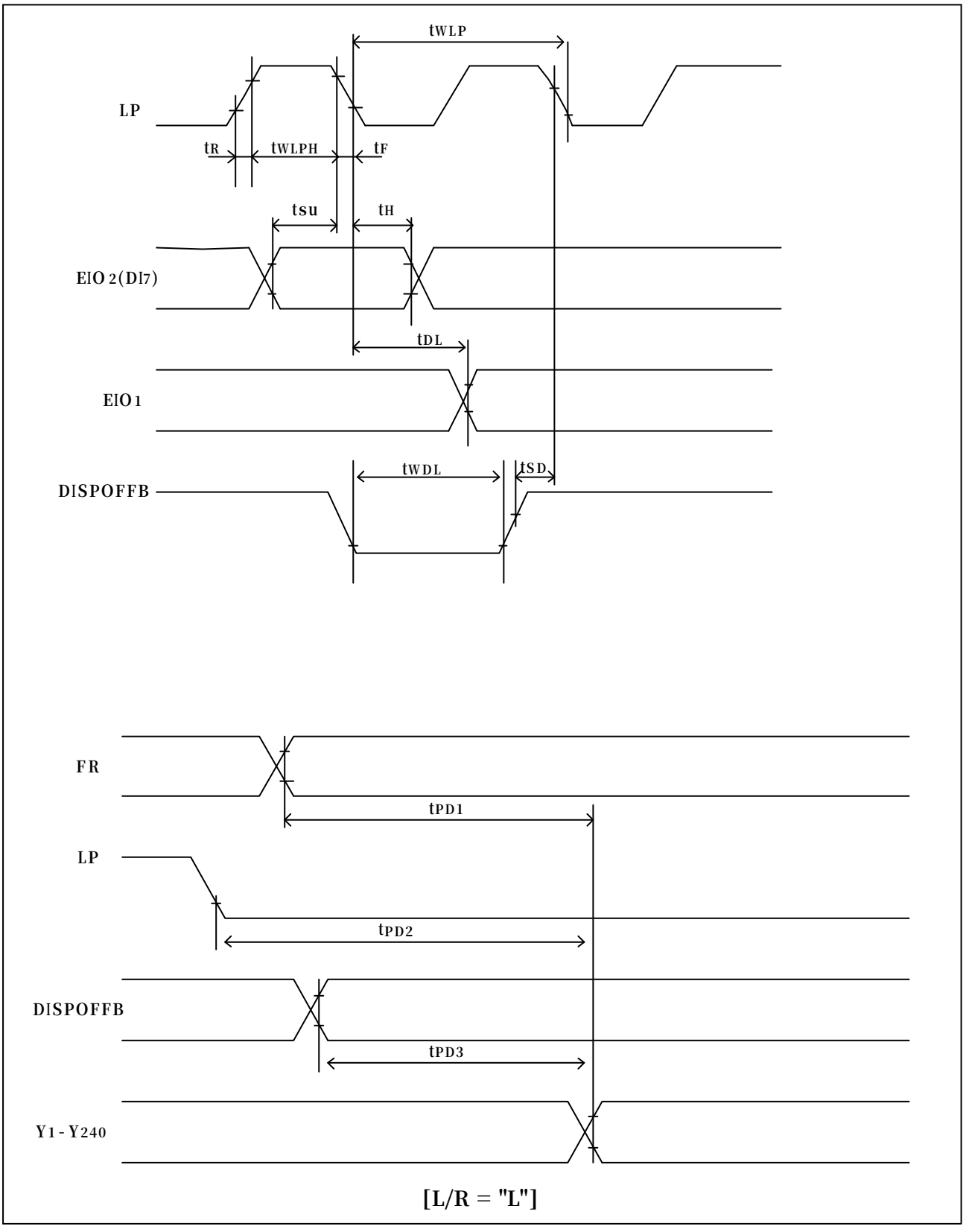


Fig. 8 Timing Characteristics (3)

(Common Mode) (Vss = V5 = 0V, V_{DD} = +2.4 to +5.5V, V_0 = +15.0 to +40.0V, Ta= -30 to +85℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R, $t_F \leq$ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0±0.5V	15			ns
		V_{DD} = +2.5 to +4.5V	30			ns
Data setup time	t_{su}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFFB removal time	t_{SD}		100			ns
DISPOFFB "L" pulse width	t_{WDL}		1.2			µs
Output delay time(1)	t_{DL}	C_L = 15 pF			200	ns
Output delay time(2)	t_{PD1}, t_{PD2}	C_L = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	C_L = 15 pF			1.2	µs

6-5. Timing Chart of Common Mode



[L/R = "L"]

6-6. System Configuration Example