

HD74AC280/HD74ACT280

9-bit Parity Generator/Checker

HITACHI

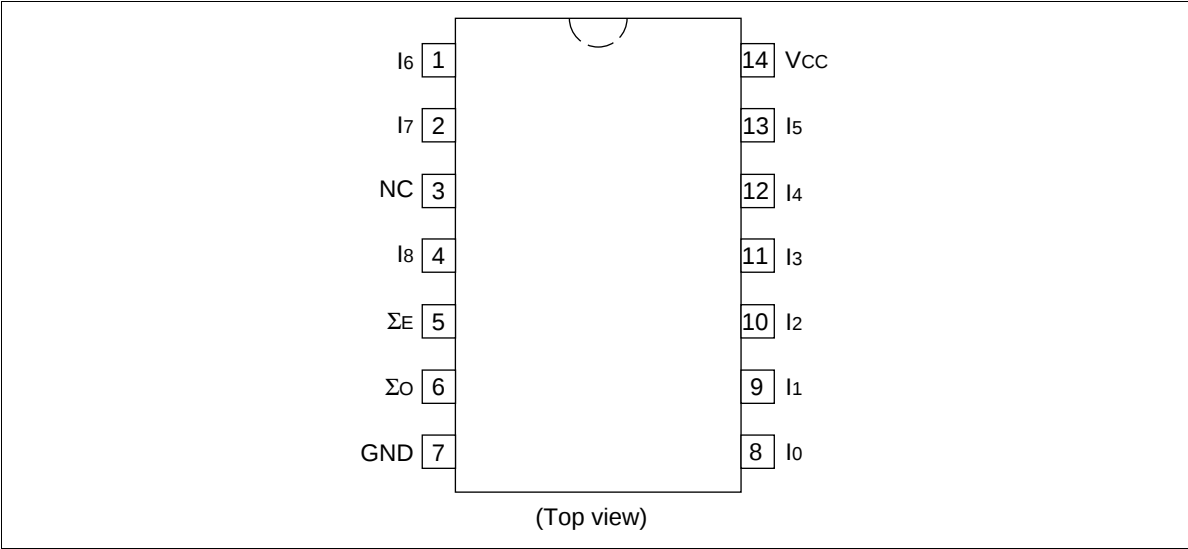
Description

The HD74AC280/HD74ACT280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is High. If an even number of inputs is High, the Sum Even output is High. If an odd number is High, the Sum Even output is Low. The Sum Odd output is the complement of the Sum Even output.

Features

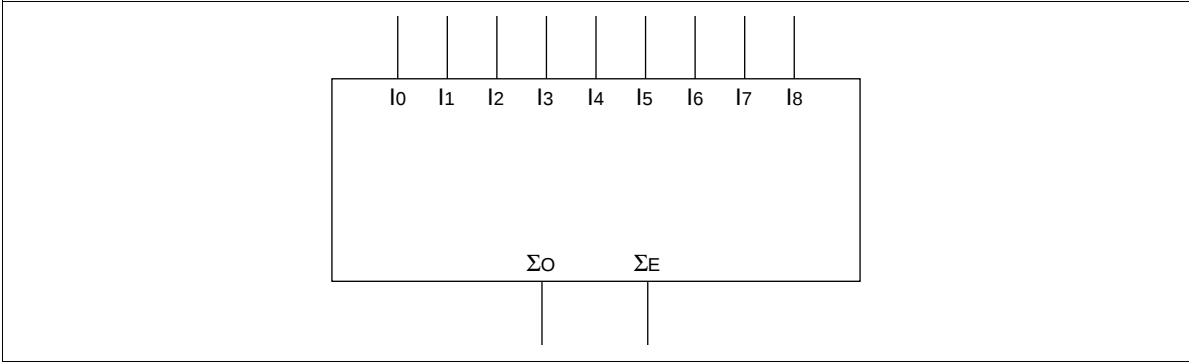
- Outputs Source/Sink 24 mA
- HD74ACT280 has TTL-Cmpatible Inputs

Pin Arrangement



HD74AC280/HD74ACT280

Logic Symbol



Pin Names

- I₀ – I₈

Data Inputs
- O

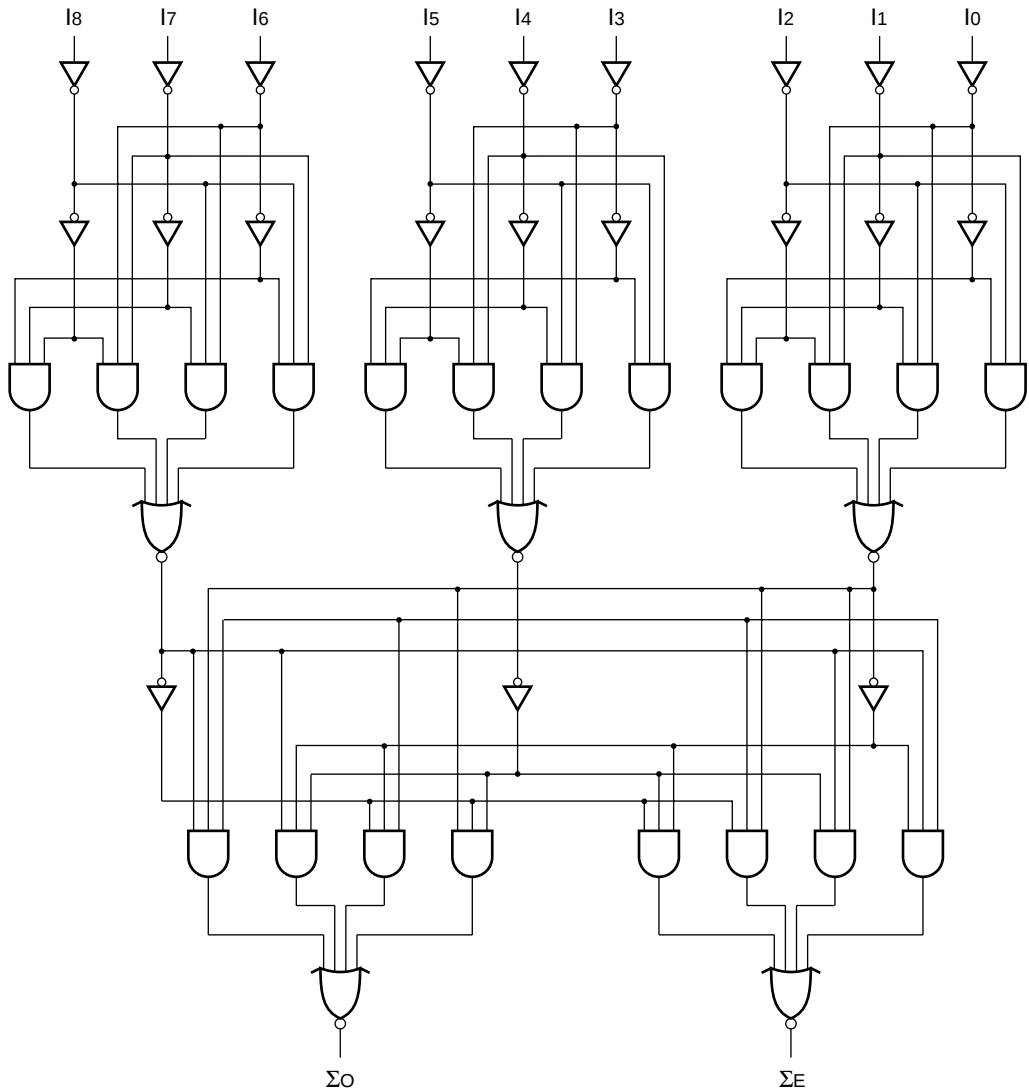
Odd Parity Output
- E

Even Parity Output

Truth Table

Number of High Inputs I ₀ – I ₈	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

- H : High Voltage Level
- L : Low Voltage Level

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

HD74AC280/HD74ACT280

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^{\circ}C$
Maximum I_{CC}/input (HD74ACT280)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$

AC Characteristics: HD74AC280

Item	Symbol	$V_{CC} (V)^{*1}$	$T_a = +25^{\circ}C$ $C_L = 50 pF$			$T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50 pF$		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t_{PLH}	3.3	1.0	14.5	17.0	1.0	18.5	ns
		5.0	1.0	11.0	13.0	1.0	14.5	
Propagation delay	t_{PHL}	3.3	1.0	14.5	17.0	1.0	18.5	ns
		5.0	1.0	11.0	13.0	1.0	14.5	

Note: 1. Voltage Range 3.3 is $3.3 V \pm 0.3 V$
Voltage Range 5.0 is $5.0 V \pm 0.5 V$

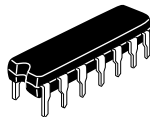
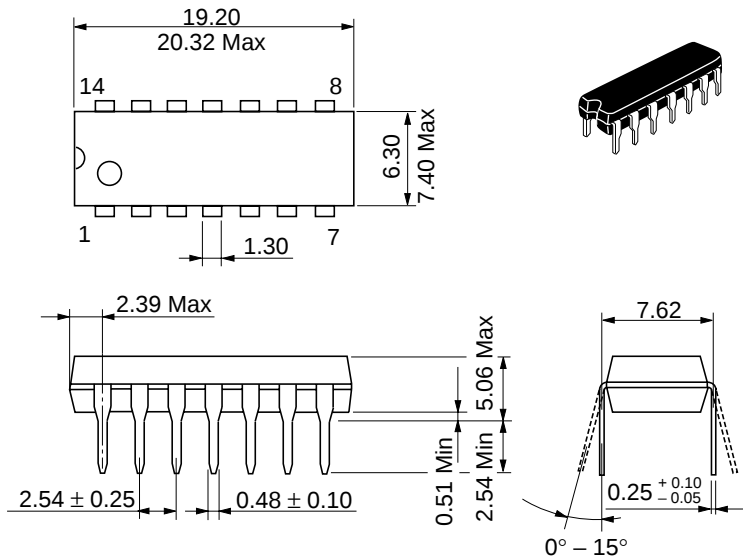
AC Characteristics: HD74ACT280

Item	Symbol	$V_{CC} (V)^{*1}$	$T_a = +25^{\circ}C$ $C_L = 50 pF$			$T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50 pF$		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t_{PLH}	5.0	1.0	12.5	15.0	1.0	16.5	ns
Propagation delay	t_{PHL}	5.0	1.0	12.5	15.0	1.0	16.5	ns

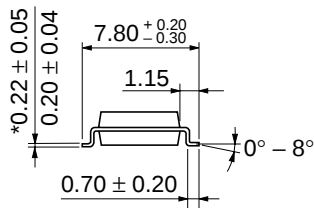
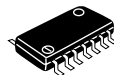
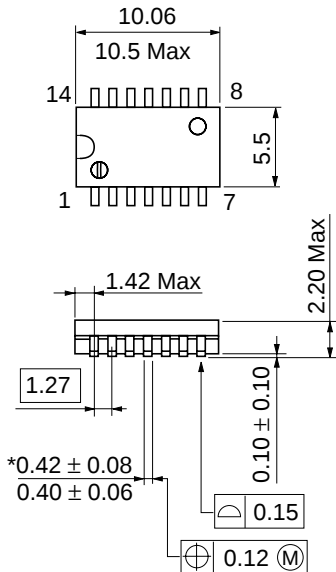
Note: 1. Voltage Range 5.0 is $5.0 V \pm 0.5 V$

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 V$
Power dissipation capacitance	C_{PD}	60.0	pF	$V_{CC} = 5.0 V$

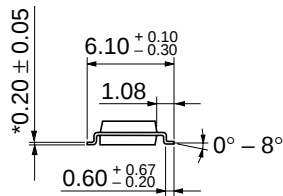
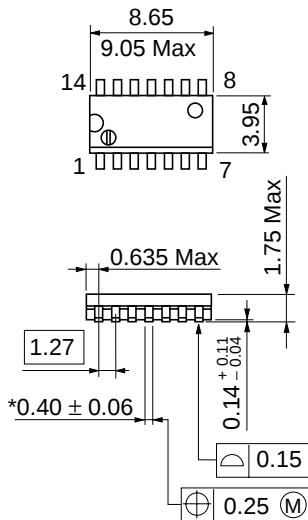


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

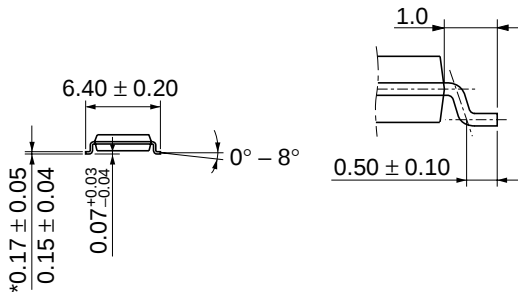
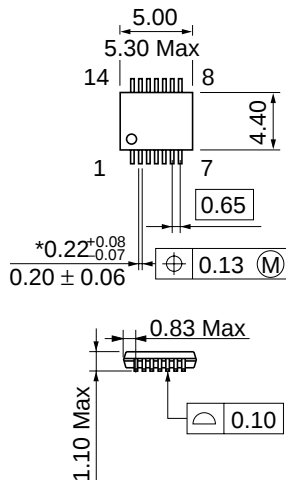


Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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