82750PD VIDEO PROCESSOR

- **High Performance Video Processor Based on the 82750PB**
- **Supports the Shared Frame Buffer Architecture**
  - **Integration of Graphics and Video into a Single Subsystem**
  - **Simple, Low Cost, High Performance Solution**
- **High Speed Shared Frame Buffer Interconnect (SFBI)**
  - **32/64-bit Memory Interface**
  - **Supports up to 8 MB of VRAM and DRAM**
- **Event Synchronization via the SynchroLink* Bus**
- **Universal Host Bus Interface**
  - **ISA, EISA, Micro Channel, PCI, VL-bus**
- **82750PD Core Features Include:**
  - **25 MHz Operation with Single Cycle Execution**
  - **Programmable 512 x 48 Instruction RAM**
  - **Flexible 16-Bit ALU**
  - **Two Internal 16-Bit Buses Providing Parallel Transfers**
  - **Pixel Interpolator**
  - **Variable Length Sequence Decoder**

The 82750PD is a programmable video processor that supports a wide range of video compression algorithms. The 82750PD operates in conjunction with a graphics processor and an optional capture processor to bring real-time video compression and decompression acceleration to the graphics subsystem. The shared frame buffer architecture is enabled through the implementation of the Shared Frame Buffer Interconnect (SFBI). This allows the integration of the video and graphics subsystem and results in a simple, low cost, and high performance solution. Event synchronization is achieved through the SynchroLink* serial bus, providing the synchronization of graphics, video, and audio events without the use of host interrupts. The 82750PD supports a Universal Host Bus Interface, which includes ISA, EISA, Micro Channel, PCI, and VL-bus.

The 82750PD is implemented using Intel's low power CHMOS IV technology and is packaged in either a 196-pin Plastic Quad Flat Package (PQFP) or a 208-pin ceramic Pin Grid Array (PGA).

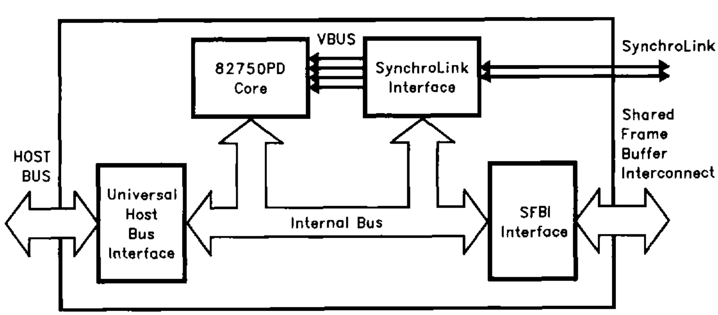

Figure 1. 82750PD Block Diagram

*SynchroLink is a trademark of ATI Technologies, Inc.

82750PD Video Processor

CONTENTS PAGE

CONTENTS PAGE

1.0 PURPOSE

This document provides electrical characteristics for the 82750PD. For a detailed description of any 82750PD functional topic, other than parametric performance, consult the 82750PD Programmer's Reference Manual (Order No. 272352) and the 82750PD Video Processor Universal Host Bus Interface Application Note (Order No. 272378).

2.0 82750PD OVERVIEW

The 82750PD is an i750® Video Processor that operates in conjunction with a graphics processor and a video capture processor to bring real-time video compression and decompression to the graphics subsystem. The 82750PD has been designed to operate in a shared frame buffer architecture where it provides video compression/decompression. The shared frame buffer system is shown in Figure 2.

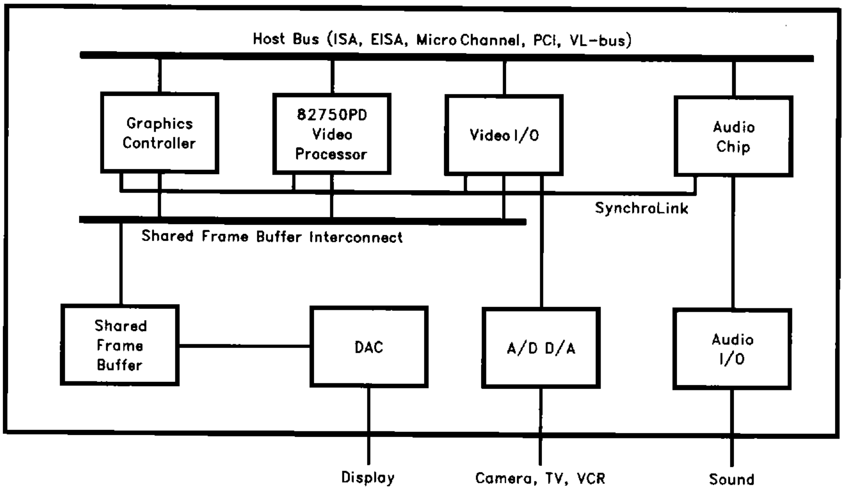

Figure 2. Shared Frame Buffer System

The 82750PD core is a microcode compatible derivative of the 82750PB and executes instructions stored in the on-chip microcode RAM. The 82750PD adds a flexible host interface, Shared Frame Buffer Interconnect support, and SynchroLink interface to provide a highly integrated solution. The 82750PD block diagram is shown in Figure 1 on page 1.

2.1 82750PD Core

The 82750PD core includes a wide instruction processor that is optimized for implementing algorithms such as compression/decompression of video frames. The core is comprised of a number of processing, storage, and input/output elements as shown in Figure 3.

The various elements are connected via the two 16-bit buses, the A bus and the B bus. During each instruction execution cycle, data can be transferred from a bus source to a bus destination on both buses.

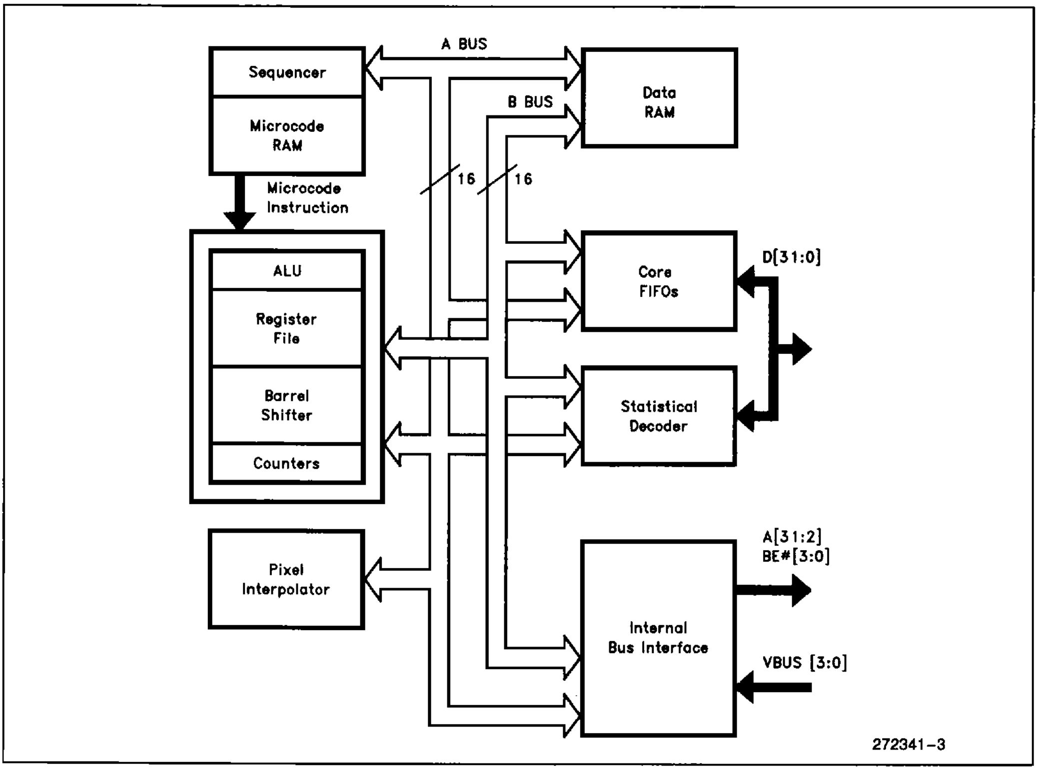

Figure 3. 82750PD Core Diagram

2.2 Universal Host Bus Interface

The 82750PD has a Universal Host Bus Interface (UHBI) that supports ISA, PCI, VL-bus, EISA, and MicroChannel system buses. The bus is selected through hardwiring the BUSTYP[2:0] pins in the proper configuration upon the rising edge of RESET. For configuration details, see Section 5.0, Reset Configuration. The pin assignments for each of the host interfaces can be found in Section 3.2.1, Universal Host Bus Interface. Detailed bus timings for each of the host interfaces can be found in Section 4.5.1.

2.3 Shared Frame Buffer Interconnect (SFBI)

The Shared Frame Buffer Interconnect (SFBI) is a multi-master interface to the shared frame buffer. The SFBI provides a high performance solution by freeing the host bus of large video and graphics-related data transfers. The SFBI is a 32/64-bit wide memory bus that can support up to 200 MByte/sec peak throughput to VRAM and DRAM. The pin assignments for the SFBI can be found in Section 3.2.2, Shared Frame Buffer Interconnect. Detailed bus timings can be found in Section 4.5.2.

2.4 SynchroLink Interface

The SynchroLink interface provides a local method of synchronizing graphic, video, and audio events without relying on the use of host interrupts. The SynchroLink interface connects components to a time multiplexed serial bus where each device on the bus has an opportunity to transmit messages to other devices. The pin assignments for the SynchroLink interface can be found in Section 3.2.3, Event Interfaces. Detailed bus timings can be found in Section 4.5.3.

3.0 PACKAGE

3.1 Package Introduction

This section describes the pins, pinouts and thermal characteristics for the 82750PD in the 208-pin Ceramic Pin Grid Array (PGA) package and the 196-pin Plastic Quad Flat Package (PQFP). For complete package specifications and information, see the *Packaging Handbook* (Order No. 240800).

3.2 Pin Descriptions

The 82750PD pins are described in this section. Descriptions of host interface bus cycles refer to data transferred into the 82750PD as write cycles and data transfered out of the 82750PD as read cycles. Table 1 presents the legend for interpreting the pin type descriptions in the following tables. The numeric pin type is preceded by an alpha designator of I for input, O for output, I/O for input/output, or OC for open-collector.

Table 1 presents the legend for interpreting the pin type descriptions in the following tables. The "Type" column identifies the general electrical characteristics of the pin. Each type is composed of two components: a function and an electrical description. The function abbreviations are given in Table 1. A brief electrical desciption of the pin type is given in Table 2. See Section 4 for complete electrical characteristics of the pins.

Table 1. Pin Type Descriptions

Pin Type	Function
I	Input Only
O	Output Only
I/O	Both Input and Output
OC	Open Collector Output

The pins associated with the Host Interface are described in Tables 3–7. Pins associated with the Shared Frame Buffer Interconnect are described in Table 8. Pins associated with the Event Interfaces are described in Table 9. Power, Ground, and Reserved Pins are described in Table 10.

Table 2. Pin Type Description

Type	Description
1	TTL Input Buffer
2	TTL Input Buffer, Schmitt Triggered
3	TTL Bi-Directional Buffer, $I_{OL} = I_{OH} = 4$ mA
4	TTL Bi-Directional Buffer, $I_{OL} = I_{OH} = 6$ mA
5	TTL Bi-Directional Buffer, $I_{OL} = I_{OH} = 18$ mA
6	TTL Bi-Directional Buffer, $I_{OL} = I_{OH} = 24$ mA
7	TTL Bi-Directional Buffer, Schmitt Triggered, $I_{OL} = 24$ mA
8	TTL Bi-Directional, $I_{OL} = 6$ mA, $I_{OH} = 2$ mA, PCI Class II
9*	TTL Three-State Output Buffer, $I_{OL} = I_{OH} = 4$ mA
10*	TTL Three-State Output Buffer, $I_{OL} = I_{OH} = 6$ mA
11*	TTL Three-State Output Buffer, $I_{OL} = I_{OH} = 12$ mA
12*	TTL Three-State Output Buffer, $I_{OL} = I_{OH} = 18$ mA
13*	TTL Three-State Output Buffer, $I_{OL} = I_{OH} = 24$ mA
14*	TTL Three-State Output Buffer, $I_{OL} = 6$ mA, $I_{OH} = 2$ mA, PCI Class II

NOTES:
For complete electrical characteristics of the pins, see Section 4.
*Some of these pins may be internally configured to function as open-collector outputs.

3.2.1 UNIVERSAL HOST BUS INTERFACE

Table 3. ISA Bus Interface

Name	PGA-Pin	PQFP-Pin	Type	Description
A[23:16]	P04, R04, S03, N04, P03, R03, S02, M04	101, 102, 104–109	I-8	**ADDRESS [23:16]:** Non-multiplexed address lines.
AD[15:0]	R02, N03, L04, Q02, R01, M03, L03, P02, K04, N02, Q01, K03, J04, E01, F02, J03	110, 111, 113–120, 122–127	I/O-8	**ADDRESS-DATA [15:0]:** Multiplexed between System Address [15 to 0] and Data [15 to 0]
AEN	A02	156	I-1	**ADDRESS ENABLE:** This active high signal is used to degate I/O devices from the ISA bus to allow DMA transfers to take place.
BALE	C04	147	I-6	**BUFFERED ADDRESS LATCH ENABLE:** Active high signal indicating a valid address on the ISA bus LA[23:17] lines. Addresses are latched on falling edge of this signal.
DIR	C01	138	OC-3	**DATA DIRECTION:** Direction control line for data transceivers. Low = Read bus cycles. High = Write bus cycles.
EN#[1:0]	H04, H03	130, 129	OC-14	**DATA OUTPUT ENABLE [1:0]:** Active low signal for the output enable of the external transceiver. (EN#[0] controls the low byte.)
IOCHRDY	C06	155	OC-7	**I/O CHANNEL READY:** This signal is pulled low (not ready) by the device to lengthen ISA bus cycles.

Table 3. ISA Bus Interface (Continued)

Name	PGA-Pin	PQFP-Pin	Type	Description
IOCSI6#	B03	151	OC-6	**I/O 16-BIT CHIP SELECT:** Active low signal indicating the present data transfer is a 16-bit, 1 wait-state, I/O cycle.
IOR#	A01	143	I-1	**I/O READ:** Active low input indicating the present bus cycle is an I/O read data transfer.
LOW#	C03	144	I-1	**I/O WRITE:** Active low input indicating the present bus cycle is an I/O write data transfer.
IRQ	A17	13	O-13	**INTERRUPT REQUEST:** This output is used to indicate that the 82750PD needs attention.
MEMCS16#	D06	152	OC-I3	**MEMORY 16-BIT CHIP SELECT:** Active low output indicating the present data transfer is a 1 wait-state, 16-bit, memory cycle.
MEMR#	D04	146	I-1	**MEMORY READ:** Active low input indicating the present bus cycle is a memory read data transfer.
MEMW#	B02	145	I-1	**MEMORY WRITE:** Active low input indicating the present bus cycle is a memory write data transfer.
NOWS#	D07	153	OC-6	**NO (ZERO) WAIT STATE REQUEST:** This active low signal indicates the device can complete the present bus cycle without inserting any additional wait cycles.
REFRESH#	C05	157	I-2	**REFRESH:** Active low input used to indicate a refresh cycle.
RENA	C02	139	OC-3	**RECEIVER ADDRESS ENABLE:** Active high output is used to enable external receiver to gate address bits 15:0 onto AD[15:0].
RESET	B05	159	I-2	**RESET DRIVE:** The Reset Drive is an active high input used to reset or initialize the 82750PD.
SBHE#	E04	142	I-3	**SYSTEM BUS HIGH BYTE ENABLE:** An active low input signifying data transfer on the upper byte of the data bus (AD[15:8]).

Table 4. EISA Bus Interface

Name	PGA-Pin	PQFP-Pin	Type	Description
AD[31:0]	See Table 12 for Pin Numbers	See Table 16 for Pin Numbers	I/O-8	**ADDRESS-DATA [31:0]:** Multiplexed between System Address [31:2] and Data [31:0]
AENx	A02	156	I-1	**ADDRESS ENABLE:** Slot-specific Address Enable where x identifies the slot number
BCLK	F14	11	I-1	**BUS CLOCK:** EISA system clock
BE#[3] BE#[2:0]	B01 D03, C02, C01	141 140-138	I-1 I-3	**BYTE ENABLE [3:0]:** These active low inputs define which byte of the data bus is used for the bus cycle.
CMD#	D04	146	I-1	**COMMAND:** Command is an active low input indicating that a channel cycle is in progress.

Table 4. EISA Bus Interface (Continued)

Name	PGA-Pin	PQFP-Pin	Type	Description
DIR	H03	129	OC-14	**DATA DIRECTION:** Direction control for data transceivers; Low = Read, High = Write.
EN# [23]	E02	133	OC-3	**DATA LATCH ENABLE [23]:** A single active low output to contol the data transceivers for the high two bytes AD[32:16].
EN# [1,0]	F03, G03	132, 131	OC-14	**DATA LATCH ENABLE [1,0]:** Active low signal for the output enable of the external transceiver. (EN# [0] controls the low byte.)
EX32#	D06	152	OC-12	**MEMORY 32-BIT CHIP SELECT:** Active low signal indicating the present data transfer is a 32-bit memory cycle.
EXRDY	C06	155	I/O-7	**CHANNEL READY:** This signal is pulled low (not ready) by the device to lengthen the bus cycle.
IO16#	B03	151	OC-6	**I/O 16-BIT CHIP SELECT:** Active low signal indicating the present data transfer is a 16-bit, 1 wait-state, I/O cycle.
IRQ	A17	13	O-13	**INTERRUPT REQUEST:** This output is used to indicate that the 82750PD needs attention.
M/IO#	B02	145	I-1	**MEMORY-I/O:** This signal distinguishes the bus cycle from being either a memory or an I/O (High = Memory cycle, Low = I/O cycle).
MSBURST#	D05	149	I-1	**MASTER BURST:** This active low input signal is used to indicate that the current EISA bus master is capable of supporting the next cycle as a burst cycle.
NOWS#	D07	153	OC-6	**NO (ZERO) WAIT STATE:** This active low output indicates that the device can complete the present bus cycle without inserting any additional wait cycles.
REFRESH#	C05	157	I-2	**REFRESH:** Active low input used to indicate a refresh cycle.
RENA	H04	130	OC-14	**RECEIVER ADDRESS ENABLE:** Active high output is used to enable external receiver to gate address bits 31:0 onto AD[31:0].
RESET	B05	159	I-2	**SYSTEM RESET:** Reset is an active high input used to reset or initialize the 82750PD.
SLBURST#	C04	147	OC-6	**SLAVE BURST:** This active low output signal is driven by the 82750PD to indicate that it is capable of accepting burst cycles.
START#	A01	143	I-1	**START CYCLE:** An active low input signal used to indicate the start of an EISA cycle.
W/R#	C03	144	I-1	**WRITE/READ:** This signal distinguishes the bus cycle as either a read or write transfer (High = Write, Low = Read).

Table 5. Micro Channel Interface—32-Bit

Name	PGA-Pin	PQFP-Pin	Type	Description
AD[31:0]	See Table 12 for Pin Numbers	See Table 16 for Pin Numbers	I/O-8	**ADDRESS-DATA [31:0]:** Multiplexed between System Address [31:0] and Data [31:0].
BE# [3] BE# [2:0]	B01 D03, C02, C01	141 140–138	I-1 I-3	**BYTE ENABLE[3:0]:** These active low input signals identify which byte of the data lines is valid for the cycle.
CHRDY	E02	133	O-3	**CHANNEL READY:** This active high output is driven low by the 82750PD to extend a command cycle.
CMD#	D04	146	I-1	**COMMAND:** Command is an active low input indicating that a channel cycle is in progress.
DIR	H03	129	OC-14	**DATA DIRECTION:** Direction control line for data transceivers. Low = Read bus cycles. High = Write bus cycles.
DS16#/DS32#	E03	135	O-3	**DATA SIZE 16 OR 32:** Active low output signal used for the DS16# and DS32# signal of an EISA bus. In a 32-bit EISA system, the 82750PD will drive both the DS16# and DS32# signals, with this pin indicating a 32-bit transfer. In a 16-bit EISA system, this signal will drive only the DS16# signal of the EISA bus, indicating a 16-bit transfer.
EN# [1:0]	F03, G03	132	OC-14	**DATA OUTPUT ENABLE [1]:** Active low signal for the output enable of the external transceiver. (EN# [0] controls the low byte.)
IRQ	A17	13	OC-13	**INTERRUPT REQUEST:** This output is used to indicate that the 82750PD requires attention.
M/IO#	B02	145	I-1	**MEMORY - I/O:** This signal distinguishes the bus cycle from being either a memory or an I/O cycle (High = Memory cycle, Low = I/O cycle).
MADE24	B03	151	I-6	**MEMORY ADDRESS ENABLE 24:** This active high input signal is active when the memory address is less than 16M.
REFRESH#	C05	157	I-2	**REFRESH:** Active low input signal used to indicate a refresh cycle.
RENA	H04	130	OC-14	**RECEIVER ADDRESS ENABLE:** Active high output is used to enable external receiver to gate address bits 31:0 onto AD[31 :0].
RESET	B05	159	I-2	**SYSTEM RESET:** The reset is an active high input used to reset or initialize the 82750PD

Table 5. Micro Channel Interface—32-Bit (Continued)

Name	PGA-Pin	PQFP-Pin	Type	Description
S1# S0#	C03 A01	144 143	I-1	**STATUS BITS [1,0]:** These bits indicate the start and type of cycle. The commands are: **S0# S1# Function** 0 0 Reserved 0 1 Write 1 0 Read 1 1 Reserved
SBHE#	E04	142	I-3	**SYSTEM BYTE HIGH ENABLE:** Active low input to enable transfer of data on the high data byte (D[15:8]), and is used with A[0] to distinguish between high and low byte transfers.
SETUP#	A02	156	I-1	**CARD SETUP:** An active low input used to place the 82750PD in Setup Mode to enable programming and read operations of the chip POS functions.
SFDBK#	G04	134	O-3	**CARD SELECT FEEDBACK:** An active low output indicating that an adapter is present at the address specified during a channel cycle.

Table 6. PCI Interface

Name	PGA-Pin	PQFP-Pin	Type	Description
AD[31:0]	See Table 12 for Pin Numbers	See Table 16 for Pin Numbers	I/O-8	**ADDRESS-DATA [31:0]:** Multiplexed address and data lines.
C/BE# [3:0]	F04, D02, E03, G04	137–134	I-3	**BUS COMMAND-BYTE ENABLE [3:0]:** These lines are multiplexed between the bus command and the byte enables. During the address phase of a transaction these lines are used to define the bus command. During the data phase these lines are used as byte enables.
CLK	F14	11	I-1	**CLOCK:** Input signal which provides timing for all transactions on PCI. All signals are sampled on the rising edge of CLK.
DEVSEL#	G03	131	I/O-14	**DEVICE SELECT:** Active low output indicating the 82750PD has decoded its address as the target of the current PCI access.
FRAME#	E02	133	I-3	**CYCLE FRAME:** Active low input indicating the beginning and duration of an access.

Table 6. PCI Interface (Continued)

Name	PGA-Pin	PQFP-Pin	Type	Description
IDSEL	A02	156	I-1	**INITIALIZATION DEVICE SELECT:** This input is used as a chip select during configuration read and write transactions.
IRDY#	D07	153	I-6	**INITIATOR READY:** Active low input to signify that data is present on AD[31:0] during write cycles, and to signify the PCI Master is prepared to accept data during read cycles.
IRQ	A17	13	O-13	**INTERRUPT REQUEST:** This output is used to indicate that the 82750PD requires attention.
PAR	H03	129	I/O-14	**PARITY:** This input/output pin completes even parity across AD [31:0] and C/BE# [3:0].
RESET	B05	159	I-2	**RESET:** Reset is an active high input used to reset or initialize the 82750PD.
STOP#	H04	130	I/O-14	**STOP:** Active low output from the 82750PD that requests the PCI master to stop the current transaction.
TRDY#	F03	132	I/O-14	**TARGET READY:** Active low output to signify data is present on AD[31:0] during read cycles, and to signify the 82750PD is prepared to accept data during write cycles.

Table 7. VL-Bus Interface

Name	PGA-Pin	PQFP-Pin	Type	Description
AD[31:0]	See Table 12 for Pin Numbers	See Table 16 for Pin Numbers	I/O-8	**ADDRESS-DATA [31:0]:** Multiplexed address [31:2] and data [31:0] lines.
BE# [3:0]	F04, D02, E03, G04	137–134	I-3	**BYTE ENABLE [3:0]:** These active low input signals describe which bytes of the 32 bits of data are involved with the current VL-Bus transfer.
BLAST#	D05	149	I-1	**BURST LAST:** Active low input indicating that the next time the BRDY# signal is asserted the burst cycle will complete.
BRDY#	D07	153	OC-6	**BURST READY:** Active low output to terminate the current cycle of a burst transfer.
D/C#	C02	139	I-1	**DATA-CODE STATUS:** This signal indicates whether the current cycle is transferring data or code.
DIR	H03	129	OC-3	**DATA DIRECTION:** Direction control line for data transceivers. Low = Read bus cycles. High = Write bus cycles.
EN#	G03	131	OC-14	**DATA OUTPUT ENABLE:** Active low signal for the output enable of external data transceivers.

Table 7. VL-Bus Interface (Continued)

Name	PGA-Pin	PQFP-Pin	Type	Description
ID[4:0]	D04, B02, C03, A01, E04	146–142	I-1 I-3	**IDENTIFIER [4:0]:** These input pins are used to identify the type and speed of the host CPU.
IRQ	A17	13	O-13	**INTERRUPT REQUEST:** This output is used to indicate that the 82750PD requires attention.
LADS#	C04	147	I-6	**LOCAL ADDRESS DATA STROBE:** This active low input indicates the start of a cycle.
LCLK	F14	11	I-1	**LOCAL CPU CLOCK:** Input signal which is a 1X clock that follows the same phase as an i486™ CPU.
LDEV#	F03	132	OC-14	**LOCAL DEVICE:** This output is used to signal that the current cycle is a VL-Bus cycle.
LRDY#	C06	155	I/O-7	**LOCAL READY:** Active low output to terminate the current bus cycle.
M/IO#	C01	138	I-3	**MEMORY OR I/O STATUS:** This input indicates the type of access currently executing on the VL-Bus. A high signifies a memory cycle. A low on this signal signifies an I/O cycle.
RDYRTN#	A02	156	I-1	**READY RETURN:** Active low input signal which indicates the end of the current cycle.
RESET	B05	159	I-2	**SYSTEM RESET:** This active high input forces the 82750PD into a known state.
RENA	H04	130	OC-14	**RECEIVER ADDRESS ENABLE:** Active high output is used to enable external receiver to gate address bits 31:0 onto AD[31:0].
W/R#	E02	133	I-3	**WRITE OR READ STATUS:** This input indicates the type of access currently executing on the VL-Bus. A write access is indicated by a high on this pin, while a read access is indicated by a low on this pin.

3.2.2 SHARED FRAME BUFFER INTERCONNECT (SFBI)

Table 8. Shared Frame Buffer Interconnect

Name	PGA-Pin	PQFP-Pin	Type	Description
CAS# [3:0]	P17, L4, L15, N16	40–37	OC-5	**COLUMN ADDRESS STROBE [3:0]:** These active low outputs are the column address strobes to each RAM bank, CAS# [0] to the first bank, CAS# [1] to the second, etc.
DSF	H15	27	OC-10	**SPECIAL FUNCTION INPUT FLAG:** Active high output used when new functions such as flash write cycles are used.
GRANT	H17	26	I-2	**GRANT:** Active high input signal from the SFBI arbiter signifying the 82750PD has mastership of the SFBI.
MA[9:0]	H14, E17, D17, F15, E16, G14, C17, D16, B17, C16	23-14	OC-11	**MEMORY ADDRESS [9:0]:** These ten bits of address are multiplexed with the row and column address. Supports either symmetric-type RAMs (9 row/9 column) or asymmetric-type (10 row/8 column).
MCLK	E15	12	I-1	**MEMORY CLOCK:** Clock input for SFBI timing.
MD[63:0]	See Tables 12 and 13 for Pin Numbers	See Tables 16 and 17 for Pin Numbers	I/O-4	**MEMORY DATA [63:0]:** SFBI 64 bits of data. MD[63:32] are not used in the 1 MB configuration.
MPRQ[1,0]	F17, G15	25, 24	I/O-4	**MEMORY PRIORITY REQUEST [1,0]:** Two-bit priority output from the 82750PD to be used in SFBI arbitration. **MPRQ[1] MPRQ[0] Function** 0 0 Highest Priority 0 1 Medium Priority 1 0 Lowest Priority 1 1 No Priority (idle)
RAS#	M15	41	OC-12	**ROW ADDRESS STROBE:** This active low output is the row address strobe to all RAM banks.
TRG/OE#	J17	28	OC-10	**TRANSFER-OUTPUT ENABLE:** This function pin is used to select serial transfers or output enable of VRAM.
WE# [7:0]	N17, M16, K14 K15, L17, K17 J15, J14	36–29	OC-10	**WRITE ENABLES [7:0]:** These active low outputs are the write enables for each data byte (WE# [0] to MD[7:0], WE# [1] to MD[15:8], etc.).

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3.2.3 EVENT INTERFACES

Table 9. Event Interfaces

Name	PGA-Pin	PQFP-Pin	Type	Description
CLKOUT (for ISA)	F03	132	O-3	**CLOCK OUT:** This output is the internal clock synchronized to MCLK. This clock is half the frequency of MCLK and can be used to follow the internal state of the 82750PD.
CLKOUT (for PCI)	C02	139	O-3	**CLOCK OUT:** This output is the internal clock synchronized to MCLK. This clock is half the frequency of MCLK and can be used to follow the internal state of the 82750PD.
PMON# (for ISA)	G03	131	O-14	**PROGRAM MONITOR:** Active low output available for software debug.
PMON# (for PCI)	C01	138	O-3	**PROGRAM MONITOR:** Active low output available for software debug.
SLDATA#*	N15	42	I/O-4	**SynchroLink DATA:** Active low signal for serial transfer of all information across the SynchroLink.
SLDATA*	M14	43	I/O-4	**SynchroLink CLOCK:** The rising edge of this signal is used to latch incoming data on the SLDATA# line. The falling edge is used by the 82750PD to enable output data on the SLDATA# line.
VBUS[3:0]* (for ISA)	F04, D02, E03, G04	137–134	I-3	**VIDEO COMMUNICATION BUS [3:0]:** Asynchronous inputs to communicate events to the 82750PD.
VBUS[3,2,0] VBUS[1]* (for PCI)	C03, A01, B01, E04	144, 143, 141 142	I-1 I-3	**VIDEO COMMUNICATION BUS [3:0]:** Asynchronous inputs to communicate events to the 82750PD.

*Either the SynchroLink interface or the VBUS input is operational as the event interface, but not both. Refer to the *82750PD Programmer's Reference Manual* (Order No. 272352) for additional information on configuring which interface is used for event communication.

3.2.4 POWER, GROUND, AND RESERVED PINS

Table 10. Power, Ground, and Reserved Pins

Name	PGA-Pin	PQFP-Pin	Type	Description
Reserved	D01	128	—	**RESERVED:** This pin is not used and should not be connected.
V_{CC}	N01, S08, A09, M01, A11, F01, A05, G01, S05, L01, K01, A06, J01, P01, H01, S11, M17, S12, G17	54, 60, 72, 84, 96, 150, 158 174, 190, 196	—	**POWER:** Power pins provide the +5V D.C. supply input.
V_{SS}	B08, L16, B06 B11, G02, K16, B12, F16, M02, J16, H16, R07, R12, G16, R08, K02, H02, R10, J02, R11, A16, B07, C11, C14, L02, P07, P13, Q03, Q17, R09, R15, S01	1, 3, 8, 46, 50, 52, 56, 64, 65, 68, 80, 81, 91, 92, 98, 103, 112, 121, 148, 154, 162, 167, 168, 170, 178, 182, 185, 186, 194	—	**GROUND:** Ground pins provide the 0V connection to which all inputs and outputs are referenced.

1

3.3 Pinout

3.3.1 PGA

This group of tables presents the host interface signals for the Pin Grid Array (PGA) package. The tables are structured as follows:

Table 11— Universal Host Bus Interface Control Signals (Pin Order)

Table 12— Universal Host Bus Interface A/D Signals (Pin Order)

Table 13— Other Signals (Pin Order)

Table 14— Host Interface A/D Signals (Name Order)

Table 15— Other Signals (Name Order)

Table 11. Universal Host Bus Interface Control Signals—PGA Package (Pin Order)

Pin #	ISA	EISA	Micro Channel	PCI	VL-Bus
A01	IOR#	START#	S0#	VBUS[2](1)	ID[1]
A02	AEN	AEN	SETUP#	IDSEL	RDYR#
A17	IRQ	IRQ	IRQ	IRQ	IRQ
B01	(3)	BE#[3]	BE#[3]	VBUS[0](1)	(3)
B02	MEMW#	M/IO#	M/IO#	(3)	ID[3]
B03	IOCS16#	IO16#	MADE24	(2)	(3)
B05	RESET	RESET	RESET	RESET	RESET
C01	DIR	BE#[0]	BE#[0]	PMON#(1)	M/IO#
C02	RENA	BE#[1]	BE#[1]	CLKOUT(1)	D/C#
C03	IOW#	W/R#	S1#	VBUS[3](1)	ID[2]
C04	BALE	SLBURST#	(3)	(2)	LADS#
C05	REFRESH#	REFRESH#	REFRESH#	(3)	(3)
C06	IOCHRDY	EXRDY	(3)	(2)	LRDY#
D02	VBUS[2](1)	(2)	(3)	C/BE#[2]	BE#[2]
D03	(2)	BE#[2]	BE#[2]	(2)	(2)
D04	MEMR#	CMD#	CMD#	(3)	ID[4]
D05	(3)	MSBURST#	(3)	(3)	BLAST#
D06	MEMCS16#	EX32#	(3)	(2)	(3)
D07	NOWS#	NOWS#	(3)	IRDY#	BRDY#
E02	(3)	EN#[23]	CHRDY	FRAME#	W/R#
E03	VBUS[1]1	(2)	DS16#/DS32#	C/BE#[1]	BE#[1]
E04	SBHE#	(2)	SBHE#	VBUS[1](1)	ID[0]
F03	CLKOUT(1)	EN#[1]	EN#[1]	TRDY#	LDEV#
F04	VBUS[3](1)	(3)	(3)	C/BE#[3]	BE#[3]
F14	(3)	BCLK	(3)	CLK	LCLK
G03	PMON#(1)	EN#[0]	EN#[0]	DEVSEL#	EN#
G04	VBUS[0](1)	(2)	SFDBK#	C/BE#[0]	BE#[0]
H03	EN#[0]	DIR	DIR	PAR	DIR
H04	EN#[1]	RENA	RENA	STOP#	RENA

NOTES:
1. These signals share pins used for the Host Interface but are described in the Event Interface.
2. These pins are no-connects.
3. These pins must be tied to V_{SS}.

Table 12. Universal Host Bus Interface Address/Data Signals—PGA Package (Pin Order)

Pin #	ISA	EISA	Micro Channel	PCI	VL-BUS
E01	AD[2]	AD[2]	AD[2]	AD[2]	AD[2]
F02	AD[1]	AD[1]	AD[1]	AD[1]	AD[1]
J03	AD[0]	AD[0]	AD[0]	AD[0]	AD[0]
J04	AD[3]	AD[3]	AD[3]	AD[3]	AD[3]
K03	AD[4]	AD[4]	AD[4]	AD[4]	AD[4]
K04	AD[7]	AD[7]	AD[7]	AD[7]	AD[7]
L03	AD[9]	AD[9]	AD[9]	AD[9]	AD[9]
L04	AD[13]	AD[13]	AD[13]	AD[13]	AD[13]
M03	AD[10]	AD[10]	AD[10]	AD[10]	AD[10]
M04	A[16]	AD[16]	AD[16]	AD[16]	AD[16]
N02	AD[6]	AD[6]	AD[6]	AD[6]	AD[6]
N03	AD[14]	AD[14]	AD[14]	AD[14]	AD[14]
N04	A[20]	AD[20]	AD[20]	AD[20]	AD[20]
P02	AD[8]	AD[8]	AD[8]	AD[8]	AD[8]
P03	A[19]	AD[19]	AD[19]	AD[19]	AD[19]
P04	A[23]	AD[23]	AD[23]	AD[23]	AD[23]
P05		AD[27]	AD[27]	AD[27]	AD[27]
P06		AD[26]	AD[26]	AD[26]	AD[26]
Q01	AD[5]	AD[5]	AD[5]	AD[5]	AD[5]
Q02	AD[12]	AD[12]	AD[12]	AD[12]	AD[12]
Q04		AD[25]	AD[25]	AD[25]	AD[25]
Q05		AD[28]	AD[28]	AD[28]	AD[28]
Q06		AD[31]	AD[31]	AD[31]	AD[31]
R01	AD[11]	AD[11]	AD[11]	AD[11]	AD[11]
R02	AD[15]	AD[15]	AD[15]	AD[15]	AD[15]
R03	A[18]	AD[18]	AD[18]	AD[18]	AD[18]
R04	A[22]	AD[22]	AD[22]	AD[22]	AD[22]
R05		AD[29]	AD[29]	AD[29]	AD[29]
R06		AD[30]	AD[30]	AD[30]	AD[30]
S02	A[17]	AD[17]	AD[17]	AD[17]	AD[17]
S03	A[21]	AD[21]	AD[21]	AD[21]	AD[21]
S04		AD[24]	AD[24]	AD[24]	AD[24]

NOTE:
Blank pins must be tied to V_{SS}.

Table 13. Other Signals—PGA Package (Pin Order)

Pin	Name
A03	MD[61]
A04	MD[58]
A05	V_{CC}
A06	V_{CC}
A07	MD[57]
A08	MD[55]
A09	V_{CC}
A10	MD[52]
A11	V_{CC}
A12	MD[51]
A13	MD[48]
A14	MD[45]
A15	MD[36]
A16	V_{SS}
B04	MD[63]
B06	V_{SS}
B07	V_{SS}
B08	V_{SS}
B09	MD[53]
B10	MD[50]
B11	V_{SS}
B12	V_{SS}
B13	MD[46]
B14	MD[41]
B15	MD[35]

Pin	Name
B16	MD[32]
B17	MA[1]
C07	MD[60]
C08	MD[59]
C09	MD[54]
C10	MD[49]
C11	V_{SS}
C12	MD[44]
C13	MD[43]
C14	V_{SS}
C15	MD[37]
C16	MA[0]
C17	MA[3]
D01	reserved*
D08	MD[62]
D09	MD[56]
D10	MD[47]
D11	MD[40]
D12	MD[42]
D13	MD[39]
D14	MD[38]
D15	MD[33]
D16	MA[2]
D17	MA[7]
E14	MD[34]

Pin	Name
E15	MCLK
E16	MA[5]
E17	MA[8]
F01	V_{CC}
F15	MA[6]
F16	V_{SS}
F17	MPRQ[1]
G01	V_{CC}
G02	V_{SS}
G14	MA[4]
G15	MPRQ[0]
G16	V_{SS}
G17	V_{CC}
H01	V_{CC}
H02	V_{SS}
H14	MA[9]
H15	DSF
H16	V_{SS}
H17	GRANT
J01	V_{CC}
J02	V_{SS}
J14	WE# [0]
J15	WE# [1]
J16	V_{SS}

NOTE:
*The reserved pin must be left unconnected.

Table 13. Other Signals—PGA Package (Pin Order) (Continued)

Pin	Name
J17	TRG/OE
K01	V_{CC}
K02	V_{SS}
K14	WE#[5]
K15	WE#[4]
K16	V_{SS}
K17	WE#[2]
L01	V_{CC}
L02	V_{SS}
L14	CAS#[2]
L15	CAS#[1]
L16	V_{SS}
L17	WE#[3]
M01	V_{CC}
M02	V_{SS}
M14	SLCLK
M15	RAS#
M16	WE#[6]
M17	V_{CC}
N01	V_{CC}
N14	MD[2]
N15	SLDATA#
N16	CAS#[0]
N17	WE#[7]
P01	V_{CC}

Pin	Name
P07	V_{SS}
P08	MD[29]
P09	MD[23]
P10	MD[16]
P11	MD[13]
P12	MD[7]
P13	V_{SS}
P14	MD[5]
P15	MD[1]
P16	MD[0]
P17	CAS#[3]
Q03	V_{SS}
Q07	MD[30]
Q08	MD[26]
Q09	MD[25]
Q10	MD[20]
Q11	MD[19]
Q12	MD[14]
Q13	MD[9]
Q14	MD[11]
Q15	MD[6]
Q16	MD[3]
Q17	V_{SS}
R07	V_{SS}

Pin	Name
R08	V_{SS}
R09	V_{SS}
R10	V_{SS}
R11	V_{SS}
R12	V_{SS}
R13	MD[17]
R14	MD[10]
R15	V_{SS}
R16	MD[8]
R17	MD[4]
S01	V_{SS}
S05	V_{CC}
S06	MD[31]
S07	MD[28]
S08	V_{CC}
S09	MD[27]
S10	MD[24]
S11	V_{CC}
S12	V_{CC}
S13	MD[22]
S14	MD[21]
S15	MD[18]
S16	MD[15]
S17	MD[12]

Table 14. Universal Host Bus Interface Address/Data Signals—PGA Package (Name Order)

Pin #	ISA	EISA	Micro Channel	PCI	VL-Bus
J03	AD[0]	AD[0]	AD[0]	AD[0]	AD[0]
F02	AD[1]	AD[1]	AD[1]	AD[1]	AD[1]
E01	AD[2]	AD[2]	AD[2]	AD[2]	AD[2]
J04	AD[3]	AD[3]	AD[3]	AD[3]	AD[3]
K03	AD[4]	AD[4]	AD[4]	AD[4]	AD[4]
Q01	AD[5]	AD[5]	AD[5]	AD[5]	AD[5]
N02	AD[6]	AD[6]	AD[6]	AD[6]	AD[6]
K04	AD[7]	AD[7]	AD[7]	AD[7]	AD[7]
P02	AD[8]	AD[8]	AD[8]	AD[8]	AD[8]
L03	AD[9]	AD[9]	AD[9]	AD[9]	AD[9]
M03	AD[10]	AD[10]	AD[10]	AD[10]	AD[10]
R01	AD[11]	AD[11]	AD[11]	AD[11]	AD[11]
Q02	AD[12]	AD[12]	AD[12]	AD[12]	AD[12]
L04	AD[13]	AD[13]	AD[13]	AD[13]	AD[13]
N03	AD[14]	AD[14]	AD[14]	AD[14]	AD[14]
R02	AD[15]	AD[15]	AD[15]	AD[15]	AD[15]
M04	A[16]	AD[16]	AD[16]	AD[16]	AD[16]
S02	A[17]	AD[17]	AD[17]	AD[17]	AD[17]
R03	A[18]	AD[18]	AD[18]	AD[18]	AD[18]
P03	A[19]	AD[19]	AD[19]	AD[19]	AD[19]
N04	A[20]	AD[20]	AD[20]	AD[20]	AD[20]
S03	A[21]	AD[21]	AD[21]	AD[21]	AD[21]
R04	A[22]	AD[22]	AD[22]	AD[22]	AD[22]
P04	A[23]	AD[23]	AD[23]	AD[23]	AD[23]
S04		AD[24]	AD[24]	AD[24]	AD[24]
Q04		AD[25]	AD[25]	AD[25]	AD[25]
P06		AD[26]	AD[26]	AD[26]	AD[26]
P05		AD[27]	AD[27]	AD[27]	AD[27]
Q05		AD[28]	AD[28]	AD[28]	AD[28]
R05		AD[29]	AD[29]	AD[29]	AD[29]
R06		AD[30]	AD[30]	AD[30]	AD[30]
Q06		AD[31]	AD[31]	AD[31]	AD[31]

NOTE:
Blank pins are no-connect for the ISA.

Table 15. Other Signals—PGA Package (Name Order)

Name	Pin	Name	Pin	Name	Pin
CAS# [3]	P17	MD[46]	B13	MD[12]	S17
CAS# [2]	L14	MD[45]	A14	MD[11]	Q14
CAS# [1]	L15	MD[44]	C12	MD[10]	R14
CAS# [0]	N16	MD[43]	C13	MD[9]	Q13
DSF	H15	MD[42]	D12	MD[8]	R16
GRANT	H17	MD[41]	B14	MD[7]	P12
MA[9]	H14	MD[40]	D11	MD[6]	Q15
MA[8]	E17	MD[39]	D13	MD[5]	P14
MA[7]	D17	MD[38]	D14	MD[4]	R17
MA[6]	F15	MD[37]	C15	MD[3]	Q16
MA[5]	E16	MD[36]	A15	MD[2]	N14
MA[4]	G14	MD[35]	B15	MD[1]	P15
MA[3]	C17	MD[34]	E14	MD[0]	P16
MA[2]	D16	MD[33]	D15	MPRQ[1]	F17
MA[1]	B17	MD[32]	B16	MPRQ[0]	G15
MA[0]	C16	MD[31]	S06	RAS#	M15
MCLK	E15	MD[30]	Q07	reserved*	D01
MD[63]	B04	MD[29]	P08	SLDATA#	N15
MD[62]	D08	MD[28]	S07	SLCLK	M14
MD[61]	A03	MD[27]	S09	TRG/OE	J17
MD[60]	C07	MD[26]	Q08	V_{CC}	N01
MD[59]	C08	MD[25]	Q09	V_{CC}	S08
MD[58]	A04	MD[24]	S10	V_{CC}	A09
MD[57]	A07	MD[23]	P09	V_{CC}	M01
MD[56]	D09	MD[22]	S13	V_{CC}	A11
MD[55]	A08	MD[21]	S14	V_{CC}	F01
MD[54]	C09	MD[20]	Q10	V_{CC}	A05
MD[53]	B09	MD[19]	Q11	V_{CC}	G01
MD[52]	A10	MD[18]	S15	V_{CC}	S05
MD[51]	A12	MD[17]	R13	V_{CC}	L01
MD[50]	B10	MD[16]	P10	V_{CC}	K01
MD[49]	C10	MD[15]	S16	V_{CC}	A06
MD[48]	A13	MD[14]	Q12	V_{CC}	J01
MD[47]	D10	MD[13]	P11	V_{CC}	P01

NOTE:
*The reserved pin must be tied to V_{SS}.

Table 15. Other Signals—PGA Package (Name Order) (Continued)

Name	Pin	Name	Pin	Name	Pin
V_{CC}	H01	V_{SS}	H16	V_{SS}	P07
V_{CC}	S11	V_{SS}	R07	V_{SS}	P13
V_{CC}	M17	V_{SS}	R12	V_{SS}	Q03
V_{CC}	S12	V_{SS}	G16	V_{SS}	Q17
V_{CC}	G17	V_{SS}	R08	V_{SS}	R09
V_{SS}	B08	V_{SS}	K02	V_{SS}	R15
V_{SS}	L16	V_{SS}	H02	V_{SS}	S01
V_{SS}	B06	V_{SS}	R10	WE# [7]	N17
V_{SS}	B11	V_{SS}	J02	WE# [6]	M16
V_{SS}	G02	V_{SS}	R11	WE# [5]	K14
V_{SS}	K16	V_{SS}	A16	WE# [4]	K15
V_{SS}	B12	V_{SS}	B07	WE# [3]	L17
V_{SS}	F16	V_{SS}	C11	WE# [2]	K17
V_{SS}	M02	V_{SS}	C14	WE# [1]	J15
V_{SS}	J16	V_{SS}	L02	WE# [0]	J14

3.3.2 PQFP

This group of tables presents the host interface signals for the Plastic Quad Flat Package (PQFP). The tables are structured as follows:

Table 16— Universal Host Bus Interface Control Signals (Pin Order)

Table 17— Universal Host Bus Interface A/D Signals (Pin Order)

Table 18— Other Signals (Pin Order)

Table 19— Other Signals (Name Order)

Table 16. Universal Host Bus Interface Control Signals—PQFP Package (Pin Order)

Pin #	ISA	EISA	Micro Channel	PCI	VL-Bus
11	(3)	BCLK	(3)	CLK	LCLK
13	IRQ	IRQ	IRQ	IRQ	IRQ
129	EN#[0]	DIR	DIR	PAR	DIR
130	EN#[1]	RENA	RENA	STOP#	RENA
131	PMON#(1)	EN#[0]	EN#[0]	DEVSEL#	EN#
132	CLKOUT(1)	EN#[1]	EN#[1]	TRDY#	LDEV#
133	(3)	EN#[23]	CHRDY	FRAME#	W/R#
134	VBUS[0](1)	(2)	SFDBK#	C/BE#[0]	BE#[0]
135	VBUS[1](1)	(2)	DS16#/32#	C/BE#[1]	BE#[1]
136	VBUS[2](1)	(2)	(3)	C/BE#[2]	BE#[2]
137	VBUS[3](1)	(3)	(3)	C/BE#[3]	BE#[3]
138	DIR	BE#[0]	BE#[0]	PMON#(1)	M/IO#
139	RENA	BE#[1]	BE#[1]	CLKOUT(1)	DC#
140	(2)	BE#[2]	BE#[2]	(2)	(2)
141	(3)	BE#[3]	BE#[3]	VBUS[0](1)	(3)
142	SBHE#		SBHE#	VBUS[1](1)	ID[0]
143	IOR#	START#	S0#	VBUS[2](1)	ID[1]
144	IOW#	W/R#	S1#	VBUS[3](1)	ID[2]
145	MEMW#	M/IO#	M/IO#	(3)	ID[3]
146	MEMR#	CMD#	CMD#	(3)	ID[4]
147	BALE	SLBURST#	(3)	(2)	LADS#
149	(3)	MSBURST#	(3)	(3)	BLAST#
151	IOCS16#	IO16#	MADE24	(2)	(3)
152	MEMCS16#	EX32#	(3)	(2)	(3)
153	NOWS#	NOWS#	(3)	IRDY#	BRDY#
155	IOCHRDY	EXRDY	(3)	(2)	LRDY#
156	AEN	AEN	SETUP#	IDSEL	RDYRTN#
157	REFRESH#	REFRESH#	REFRESH#	(3)	(3)
159	RESET	RESET	RESET	RESET	RESET

NOTES:
1. These signals share pins used for the Host Interface but are described in the Event Interface. VBUS tested on PCI only (not ISA).
2. These pins are no-connects.
3. These pins must be tied to V_{SS}.

Table 17. Universal Host Bus Interface Address/Data Signals—PQFP Package (Pin Order)

Pin #	ISA	EISA	Micro Channel	PCI	VL-Bus
89		AD[31]	AD[31]	AD[31]	AD[31]
90		AD[30]	AD[30]	AD[30]	AD[30]
93		AD[29]	AD[29]	AD[29]	AD[29]
94		AD[28]	AD[28]	AD[28]	AD[28]
95		AD[27]	AD[27]	AD[27]	AD[27]
97		AD[26]	AD[26]	AD[26]	AD[26]
99		AD[25]	AD[25]	AD[25]	AD[25]
100		AD[24]	AD[24]	AD[24]	AD[24]
101	A[23]	AD[23]	AD[23]	AD[23]	AD[23]
102	A[22]	AD[22]	AD[22]	AD[22]	AD[22]
104	A[21]	AD[21]	AD[21]	AD[21]	AD[21]
105	A[20]	AD[20]	AD[20]	AD[20]	AD[20]
106	A[19]	AD[19]	AD[19]	AD[19]	AD[19]
107	A[18]	AD[18]	AD[18]	AD[18]	AD[18]
108	A[17]	AD[17]	AD[17]	AD[17]	AD[17]
109	A[16]	AD[16]	AD[16]	AD[16]	AD[16]
110	AD[15]	AD[15]	AD[15]	AD[15]	AD[15]
111	AD[14]	AD[14]	AD[14]	AD[14]	AD[14]
113	AD[13]	AD[13]	AD[13]	AD[13]	AD[13]
114	AD[12]	AD[12]	AD[12]	AD[12]	AD[12]
115	AD[11]	AD[11]	AD[11]	AD[11]	AD[11]
116	AD[10]	AD[10]	AD[10]	AD[10]	AD[10]
117	AD[9]	AD[9]	AD[9]	AD[9]	AD[9]
118	AD[8]	AD[8]	AD[8]	AD[8]	AD[8]
119	AD[7]	AD[7]	AD[7]	AD[7]	AD[7]
120	AD[6]	AD[6]	AD[6]	AD[6]	AD[6]
122	AD[5]	AD[5]	AD[5]	AD[5]	AD[5]
123	AD[4]	AD[4]	AD[4]	AD[4]	AD[4]
124	AD[3]	AD[3]	AD[3]	AD[3]	AD[3]
125	AD[2]	AD[2]	AD[2]	AD[2]	AD[2]
126	AD[1]	AD[1]	AD[1]	AD[1]	AD[1]
127	AD[0]	AD[0]	AD[0]	AD[0]	AD[0]

NOTE:
Blank pins must be tied to V_{SS}.

Table 18. Other Signals—PQFP Package (Pin Order)

Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	39	CAS#[2]	76	MD[22]
2	MD[38]	40	CAS#[3]	77	MD[23]
3	V_{SS}	41	RAS#	78	MD[24]
4	MD[37]	42	SLDATA#	79	MD[25]
5	MD[36]	43	SLCLK	80	V_{SS}
6	MD[35]	44	MD[0]	81	V_{SS}
7	MD[34]	45	MD[1]	82	MD[26]
8	V_{SS}	46	V_{SS}	83	MD[27]
9	MD[33]	47	MD[2]	84	V_{CC}
10	MD[32]	48	MD[3]	85	MD[28]
12	MCLK	49	MD[4]	86	MD[29]
14	MA[0]	50	V_{SS}	87	MD[30]
15	MA[1]	51	MD[5]	88	MD[31]
16	MA[2]	52	V_{SS}	91	V_{SS}
17	MA[3]	53	MD[6]	92	VSS
18	MA[4]	54	V_{CC}	96	V_{CC}
19	MA[5]	55	MD[7]	98	V_{SS}
20	MA[6]	57	MD[8]	103	V_{SS}
21	MA[7]	58	MD[9]	112	V_{SS}
22	MA[8]	59	MD[10]	121	V_{SS}
23	MA[9]	60	V_{CC}	128	reserved*
24	MPRQ[0]	61	MD[11]	148	V_{SS}
25	MPRQ[1]	62	MD[12]	150	V_{CC}
26	GRANT	63	MD[13]	154	V_{SS}
27	DSF	64	V_{SS}	158	V_{CC}
26	TRG/OE#	65	V_{SS}	160	MD[63]
29	WE#[0]	66	MD[14]	161	MD[62]
30	WE#[1]	67	MD[15]	162	V_{SS}
31	WE#[2]	68	V_{SS}	163	MD[61]
32	WE#[3]	69	MD[16]	164	MD[60]
33	WE#[4]	70	MD[17]	165	MD[59]
34	WE#[5]	71	MD[18]	166	MD[58]
35	WE#[6]	72	V_{CC}	167	V_{SS}
36	WE#[7]	73	MD[19]	168	V_{SS}
37	CAS#[0]	74	MD[20]	169	MD[57]
38	CAS#[1]	75	MD[21]	170	V_{SS}

NOTE:
*The reserved pin must be tied to V_{SS}.

Table 18. Other Signals—PQFP Package (Pin Order) (Continued)

Pin	Name
171	MD[56]
172	MD[55]
173	MD[54]
174	V_{CC}
175	MD[53]
176	MD[52]
177	MD[51]
178	V_{SS}
179	MD[50]

Pin	Name
180	MD[49]
181	MD[48]
182	V_{SS}
183	MD[47]
184	MD[46]
185	V_{SS}
186	V_{SS}
187	MD[45]
188	MD[44]

Pin	Name
189	MD[43]
190	V_{CC}
191	MD[42]
192	MD[41]
193	MD[40]
194	V_{SS}
195	MD[39]
196	V_{CC}

Table 19. Other Signals—PQFP Package (Name Order)

Name	Pin
CAS# [3]	40
CAS# [2]	39
CAS# [1]	38
CAS# [0]	37
DSF	27
GRANT	26
MA[9]	23
MA[8]	22
MA[7]	21
MA[6]	20
MA[5]	19
MA[4]	18
MA[3]	17
MA[2]	16
MA[1]	15
MA[0]	14
MCLK	12
MD[63]	160
MD[62]	161
MD[61]	163
MD[60]	164
MD[59]	165
MD[58]	166
MD[57]	169
MD[56]	171
MD[55]	172
MD[54]	173
MD[53]	175
MD[52]	176
MD[51]	177
MD[50]	179
MD[49]	180
MD[48]	181
MD[47]	183
MD[46]	184
MD[45]	187
MD[44]	188
MD[43]	189
MD[42]	191
MD[41]	192
MD[40]	193
MD[39]	195
MD[38]	2
MD[37]	4
MD[36]	5
MD[35]	6
MD[34]	7
MD[33]	9
MD[32]	10
MD[31]	88
MD[30]	87
MD[29]	86
MD[28]	85
MD[27]	83
MD[26]	82
MD[25]	79
MD[24]	78
MD[23]	77
MD[22]	76
MD[21]	75
MD[20]	74
MD[19]	73
MD[18]	71
MD[17]	70
MD[16]	69
MD[15]	67
MD[14]	66
MD[13]	63
MD[12]	62
MD[11]	61
MD[10]	59
MD[9]	58
MD[8]	57
MD[7]	55
MD[6]	53
MD[5]	51
MD[4]	49
MD[3]	48
MD[2]	47
MD[1]	45
MD[0]	44
MPRQ[1]	25
MPRQ[0]	24
RAS#	41
reserved*	128
SLDATA#	42
SLCLK	43
TRG/OE	28
V_{CC}	54
V_{CC}	60
V_{CC}	72
V_{CC}	84
V_{CC}	96
V_{CC}	150
V_{CC}	158
V_{CC}	174
V_{CC}	190
V_{CC}	196
V_{SS}	1
V_{SS}	3
V_{SS}	8
V_{SS}	46
V_{SS}	50
V_{SS}	52
V_{SS}	56
V_{SS}	64
V_{SS}	65
V_{SS}	68

NOTE:
*The reserved pin must be left unconnected.

Table 19. Other Signals—PQFP Package (Name Order) (Continued)

Name	Pin
V_{SS}	80
V_{SS}	81
V_{SS}	91
V_{SS}	92
V_{SS}	98
V_{SS}	103
V_{SS}	112
V_{SS}	121
V_{SS}	148

Name	Pin
V_{SS}	154
V_{SS}	162
V_{SS}	167
V_{SS}	168
V_{SS}	170
V_{SS}	178
V_{SS}	182
V_{SS}	185
V_{SS}	186

Name	Pin
V_{SS}	194
WE# [7]	36
WE# [6]	35
WE# [5]	34
WE# [4]	33
WE# [3]	32
WE# [2]	31
WE# [1]	30
WE# [0]	29

3.4 Mechanical Data

Refer to Intel's Packaging Handbook, (Order No. 240800), for detailed information on packaging of the 82750PD.

3.5 Package Thermal Specifications

The 82750PD is specified for operations when T_C (the case temperature) is within the range of 0°C to 85°C. T_C may be measured in any environment to determine whether the 82750PD is within specified operation range. The case temperature should be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from case to ambient) with the following equation:

$$T_A = T_C - P * \theta_{CA}$$

where P is the power dissipated.

Typical values for θ_{CA} at various airflows are given in Table 20 for the 196-lead PQFP package. Table 21 shows the maximum T_A allowable (without exceeding T_C) at various airflows.

1

Table 20. Thermal Resistance (°C/W)

	θ_{CA} vs Airflow-ft/min (m/sec)					
Package	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
196-Lead	19.5	14.5	11.5	9.5	8.5	8.1

Table 21. Maximum T_A at Various Airflows (°C)

		T_A vs Airflow-ft/min (m/sec) (0°C)					
Package	MCLK Frequency (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
196-Lead	50	46	56	62	66	68	69

4.0 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Case Temperature under Bias . . . −65°C to +110°C

Storage Temperature . . . . −65°C to +150°C

Voltage on Any Pin
with Respect to V_{SS} . . . . −0.5V to V_{CC} +0.5V

Supply Voltage
with Respect to V_{SS} . . . . −0.5V to +6.5V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Operating Conditions

Table 22. Operating Conditions

Symbol	Parameter	Min	Max	Units
T_{CASE}	Temperature	0	85	°C
V_{CC}	Supply Voltage	4.75	5.25	V
f_{PCI}	PCI Host Interface Frequency		33	MHz
f_{VL}	VL-Bus Host Interface Frequency		33	MHz
f_{MCLK}	SFBI Interface Frequency		50	MHz

4.3 Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Every 82750PD-based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane and every V_{SS} pin must be connected to the ground plane. Unused pins should not be connected.

4.4 DC Specifications

Table 23. DC Characteristics (over specified operating conditions)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = Rated Buffer Current*		0.2	0.4	V
V_{OH}	Output High Voltage	I_{OH} = Rated Buffer Current*	2.4	3.4		V
V_T^+	Schmitt Trigger +ev Threshold			2.0	2.4	V
V_T^-	Schmitt Trigger −ve Threshold		0.6	0.8		V
O_{LI}	Output Leakage Current	$V_{SS} < V_{IN} < V_{CC}$		0	±10	μA
I_{LI}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$		0	±10	μA
I_{CC}	Active Mode Current	f_{MCLK} = Max V_{CC} = Max			300	mA
C_S	Pin Capacitance	Any Pin to V_{SS}			10	pF

*See Table 25.

Table 24. Additional PCI Class II DC Characteristics (over specified operating conditions)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OL}(AC)	Switch Low Current	V_{OUT} = 1.4V	95			mA
I_{OH}(AC)	Switch High Current	V_{OUT} = 2.2V	−44			mA

Table 25. Pin Type Rated Buffer Currents

Type	Description
1	TTL Input Buffer
2	TTL Input Buffer, Schmitt Triggered
3	TTL Bi-Directional Buffer, $I_{OL} = I_{OH}$ = 4 mA
4	TTL Bi-Directional Buffer, $I_{OL} = I_{OH}$ = 6 mA
5	TTL Bi-Directional Buffer, $I_{OL} = I_{OH}$ = 18 mA
6	TTL Bi-Directional Buffer, $I_{OL} = I_{OH}$ = 24 mA
7	TTL Bi-Directional Buffer, Schmitt Triggered, I_{OH} = 24 mA
8	TTL Bi-Directional, I_{OL} = 6 mA, I_{OH} = 2 mA, PCI Class II
9	TTL Three-State Output Buffer, $I_{OL} = I_{OH}$ = 4 mA
10	TTL Three-State Output Buffer, $I_{OL} = I_{OH}$ = 6 mA
11	TTL Three-State Output Buffer, $I_{OL} = I_{OH}$ = 12 mA
12	TTL Three-State Output Buffer, $I_{OL} = I_{OH}$ = 18 mA
13	TTL Three-State Output Buffer, $I_{OL} = I_{OH}$ = 24 mA
14	TTL Three-State Output Buffer, I_{OL} = 6 mA, I_{OH} = 2 mA, PCI Class II

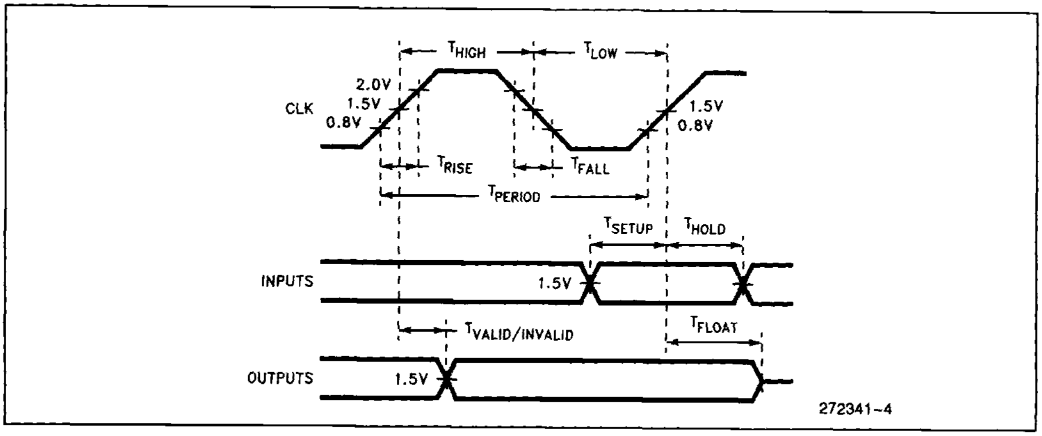


Figure 4. AC Waveform Test Points

4.5 AC Characteristics

4.5.1 UNIVERSAL HOST BUS INTERFACE TIMINGS

Table 26. Host Bus Timings—ISA

Symbol	Description	Min (ns)	Max (ns)
T1	REFRESH# Setup Time to Memory Command Active	30	
T2	REFRESH# Hold Time from Memory Command Inactive	10	
T3	SBHE# Setup Time to Memory Command Active	10	
T4	SBHE# Hold Time from Memory Command Inactive	10	
T5	Address [16:0] Setup Time to Memory Command Active	10	
T6	Address [16:0] Hold Time from Memory Command Active	10	
T7	Read Data Valid from IOCHRDY Active		20
T8	Read Data Invalid from MEMR# Inactive	0	
T9	Write Data Setup Time to MEMW# Inactive	20	
T10	Write Data Hold Time from MEMW# Inactive	10	
T11	A[23:17] Setup Time to BALE Inactive	10	
T12	A[23:17] Hold Time from BALE Inactive	5	
T13	MEMCS16# Active from Address [23:17] Valid		20
T13a	MEMCS16# Active from Address [16:0] Valid		10.5
T14	MEMCS16# Inactive from Address [23:17] Invalid		20
T14a	MEMCS16# Inactive from Address [16:0] Invalid		10.5
T15	IOCHRDY Inactive from Memory Command Active		13
T16	EN# [1,0], DIR, RENA Active from Memory Command Active		20
T17	EN# [1,0], DIR, RENA Inactive from Memory Command Inactive	5	20
T18	NOWS# Delay from MEMW# Command		10

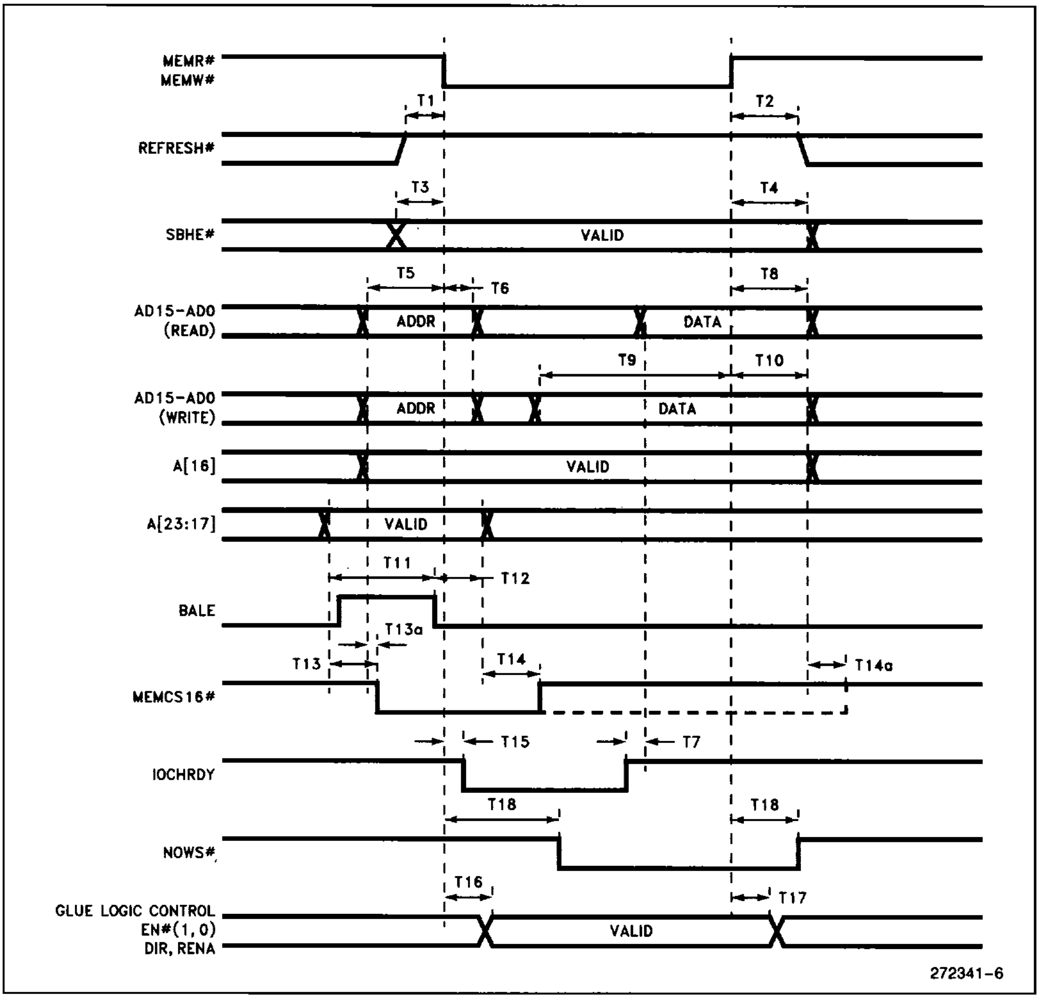


Figure 5. Host Bus Timings—ISA

Table 27. Host Bus Timings—EISA

Symbol	Description	Min (ns)	Max (ns)
T1	BLCK Period	120	
T2	BCLK High Time	54	
T3	BCLK Low Time	54	
T4	START# Setup Time to BCLK Rising	30	
T5	START# Hold Time from BCLK Rising	2	
T6	M/IO#, W/R# Setup Time to BCLK Rising	30	
T7	M/IO#, W/R# Hold Time from BCLK Rising	8	
T8a	Address Setup Time to BCLK Falling (Burst)	20	
T8b	Address Setup Time to BCLK Rising	20	
T8c	BE# [3:0] Setup Time to BCLK Rising	5	
T9a	Address Hold Time from BCLK Falling (Burst)	5	
T9b	Address Hold Time from BCLK Rising	10	
T9c	BE# [3:0] Hold Time from BCLK Rising	2	
T10a	Write Data Setup Time to BCLK Rising (Burst)	30	
T10b	Write Data Setup Time to BCLK Falling	10	
T11a	Write Data Hold Time from BCLK Rising (Burst)	5	
T11b	Write Data Hold Time from BCLK Falling	10	
T12	Read Data Valid from BCLK Rising		30
T13	Read Data Invalid from CMD# Inactive	2	
T14	EXRDY Inactive from BCLK Rising		20
T15	EXRDY Active from BCLK Falling		20
T16	EX32#, NOWS# Active from Address Valid		30
T17	EX32#, NOWS# Inactive from BCLK		70
T18	EN# [23,1,0], DIR, RENA Active from BCLK Rising		30
T19	EN# [23,1,0], DIR, RENA Inactive from BCLK Falling		30

1

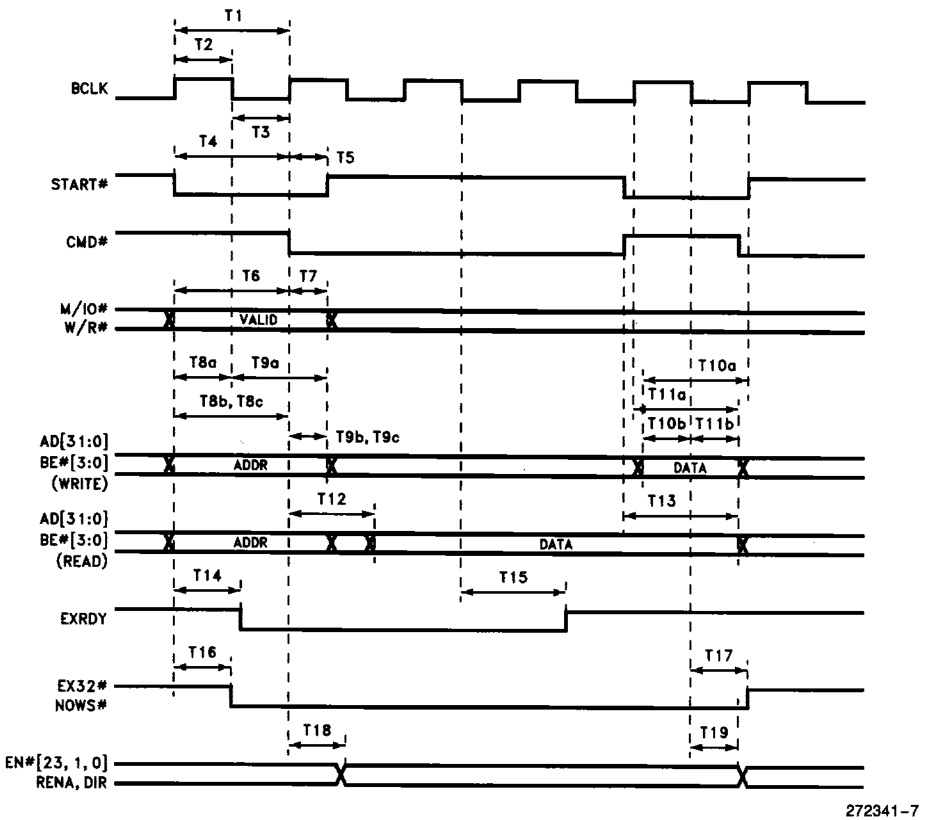


Figure 6. Host Bus Timings—EISA

Table 28. Host Bus Timings—Micro Channel

Symbol	Description	Min (ns)	Max (ns)
T1	S0#, S1#, M/IO#, REFRESH#, MADE24 Setup Time to CMD# Active	30	
T2	S0#, S1#, M/IO#, REFRESH#, MADE24 Hold Time from CMD# Active	10	
T3	Address Setup Time to CMD# Active	20	
T4	Address Hold Time from CMD# Active	10	
T5	Write Data Setup Time to CMD# Inactive	20	
T6	Write Data Hold Time from CMD# Inactive	10	
T7	Read Data Valid to CHRDY Active	20	
T8	Read Data Invalid from CMD# Inactive	0	20
T9	SFDBK# Active from Address Valid		30
T10	SFDBK# Inactive from CMD# Active	0	10
T11	CHRDY Active from Address Valid		20
T12	EN#[1,0], DIR, RENA Active from CMD# Active		20
T13	EN#[1,0], DIR, RENA Inactive from CMD# Inactive		20

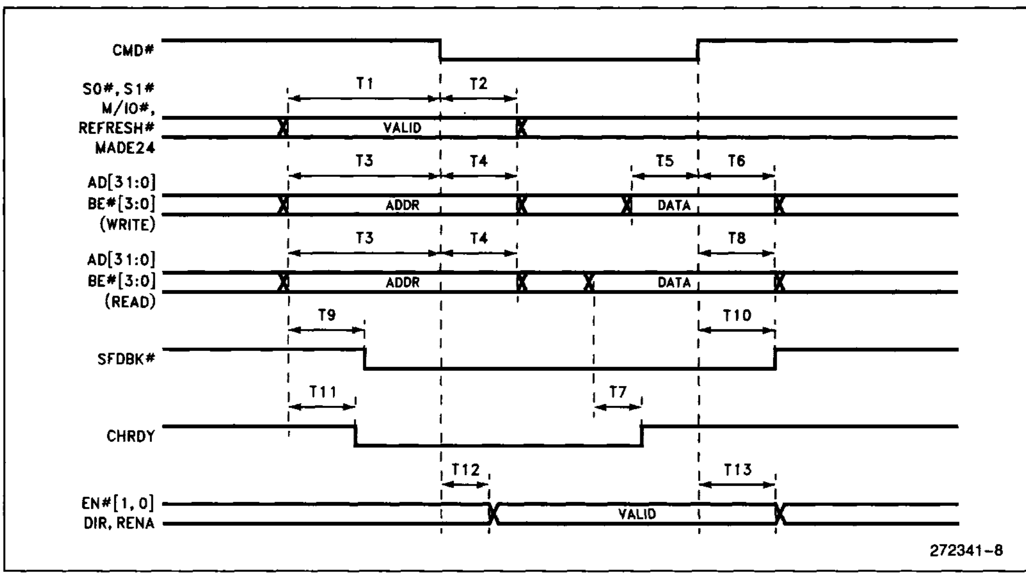


Figure 7. Host Bus Timings—Micro Channel

Table 29. Host Bus Timings—PCI

Symbol	Parameter	33-10	Units	Notes
TI	CLK to Signal Valid Delay (max)	Class II- 11	ns	C_L = 50 pF
T2	CLK to Signal Invalid Delay (min)	2	ns	
T3	Output Hi-Z to Active from CLK (min)	2	ns	
T4	Output Active to Hi-Z from CLK (max)	28	ns	Minimum = Tval min
T5	Input Signal Valid Setup Time before CLK (min)	7	ns	
T6	Input Signal Hold Time from CLK (min)	0	ns	

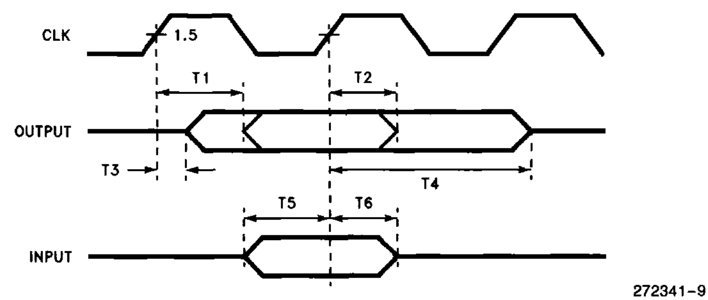


Figure 8. Host Bus Timings—PCI

Table 30. Host Bus Timings—VL-Bus

Symbol	Description	Min (ns)	Max (ns)
T1	LCLK Period	30	
T2	LCLK High Time	14	
T3	LCLK Low Time	14	
T4	LADS# Setup Time to LCLK	7	
T5	LADS# Hold Time from LCLK	3	
T6	M/IO#, D/C#, W/R#, BE#[3:0] Setup Time to LCLK	7	
T7	M/IO#, D/C#, W/R#, BE#[3:0] Hold Time from LCLK	3	
T8	Address Setup Time to LCLK	2	
T9	Address Hold Time from LCLK	1	
T10	Read Data Valid from LCLK	10	15
T11	Read Data Float from LCLK	2	
T12	Write Data Setup Time to LCLK	2	
T13	Write Data Hold time from LCLK	1	
T14	LDEV# Active from Address Valid		20
T16	LDEV# Inactive from LCLK		20
T17	LRDY#, BRDY# Inactive from LCLK		10
T18	LRDY#, BRDY# Active from LCLK		10
T19	LRDY#, BRDY# Float from LCLK		10
T20	EN#, RENA, DIR Active from LCLK	10	
T21	EN#, RENA, DIR Inactive from LCLK	10	

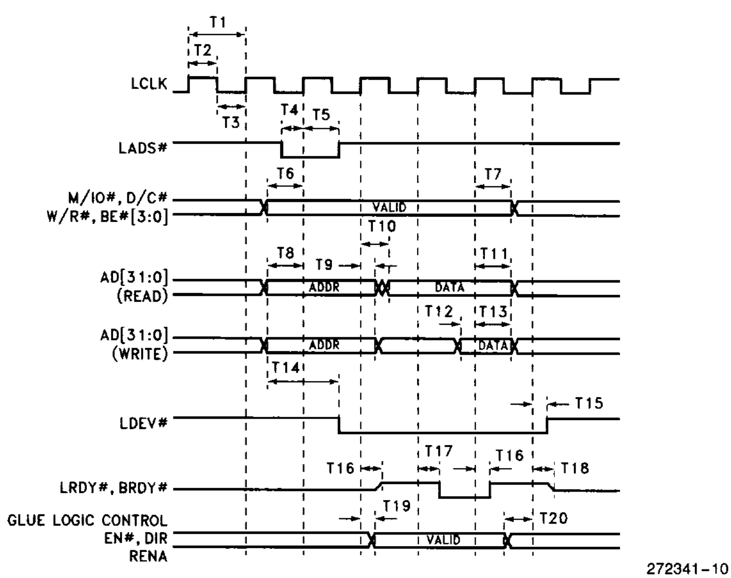


Figure 9. Host Bus Timings—VL-Bus

4.5.2 SHARED FRAME BUFFER INTERCONNECT TIMINGS

Table 31. Shared Frame Buffer Interconnect Timings

Symbol	Description	Min (ns)	Max (ns)
T1	MCLK Period	20	
T2	MCLK High Pulse	8	13.2
T3	MCLK Low Pulse	8	13.2
T4	MCLK to RAS# Delay	0	22
T5	MCLK to CAS# Delay	0	30
T6	Read Data to CAS# Setup	1	
T7	MCLK to OE# Delay	0	40
T8	MCLK to WE# Delay	0	35
T9	MCLK to Address Delay	2	31
T10	MCLK to Write Data Delay	2	35
T11	RESET High Pulse Width	92T1	
Td	Delta of h>l or l>h of Any Signal (i.e., (HL) = TdRAS(LH) ± Td)		2

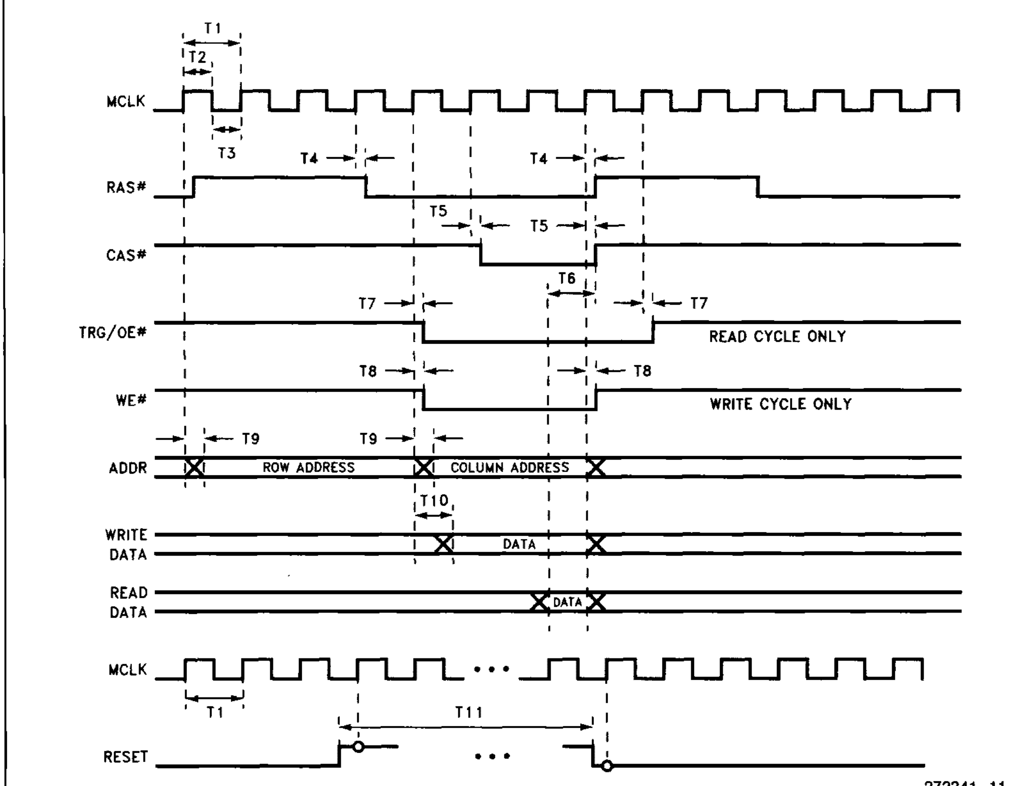


Figure 10. Shared Frame Buffer Interconnect Timings

Table 32. Shared Frame Buffer Interconnect Arbitration Timings

Symbol	Description	Min (ns)	Max (ns)
T1	MPRQ Valid from MCLK		16
T2*	Grant Setup Time to MCLK	5	

*This timing need only be met to guarantee max GRANT to RAS# delay illustrated in the bus waveform figures found in Section 6.

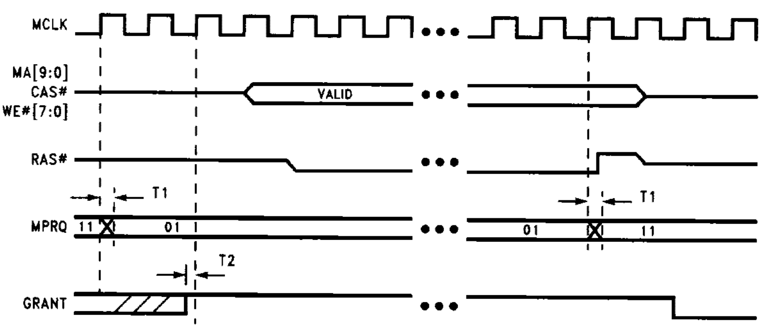


Figure 11. Shared Frame Buffer Interconnect Arbitration Timings

4.5.3 EVENT INTERFACE TIMINGS

Table 33. Event Synchronization Bus Timings

Symbol	Description	Min (ns)	Max (ns)
T1	SLCLK Period	120	125
T2	SLCLK Low Pulse	48	
T3	SLCLK High Pulse	48	
T4	SLDATA# Valid from SLCLK		20
T5	SLDATA# Float from SLCLK		20
T6	SLDATA# Setup Time to SLCLK	20	
T7*	SLDATA# Hold Time from SLCLK	10	

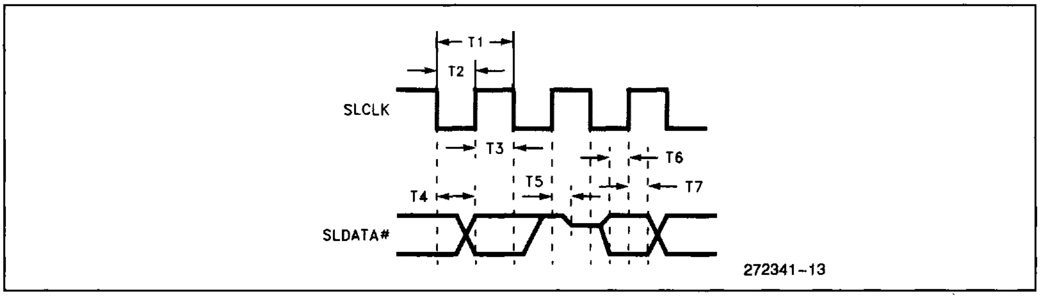


Figure 12. SynchroLink Timings

Table 34. VBUS Timings

Symbol	Parameter	Min (ns)	Max (ns)
T1	VBUS Setup Time to MCLK	10	
T2	VBUS Hold Time after MCLK	10	

NOTE:
VBVS tested on PCI only.

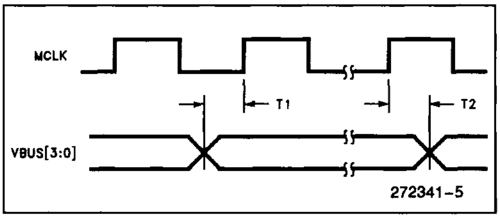


Figure 13. VBUS Timings

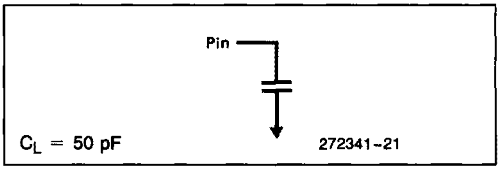


Figure 14. AC Test Load Circuit

5.0 RESET CONFIGURATION

The 82750PD is configured during reset. The configuration options include selecting the universal host bus interface type, I/O Base address, Shared Frame Buffer Interconnect memory type, and device ID for the 82750PD. This section outlines the reset pin assignments for device configuration. Each option is described. The reset sequence is also defined.

5.1 Reset Input Pin Function

The following tables describe the pins used to configure the 82750PD into the proper operating condition.

Table 35. 82750PD Reset Configuration Inputs

Reset Setup Function	82750PD Pin	Value
BUSTYP[2:0]	MD[2:0]	
Reserved	MD[3]	Must Be High
IOBASE[8:0]	MD[12:4]	
Reserved	MD[13]	Must Be Low
MSLOT16	MD[14]	
MEMTYPE	MD[15]	
Reserved	MD[16]	Must Be Low
DEVID[1:0]	MPRQ[1:0]	
DEVID[2]	GRANT	

BUSTYP[2:0] (Host Bus Type)—These decoded bits are listed in Table 36.

IOBASE[8:0] (I/O Base Address)—The configuration for these pins directly correlates (MSB through LSB) to the I/O base address which can read and write through I/O to the 82750PD. For example, the base address of 2EAH would set IOBASE[8:0] to 175H (right shift 1 bit). See the 82750PD Programmer's Reference Manual (Order No. 272352) for details.

MSLOT16 (Micro Channel Slot, 16 Bit)—This pin is used if the BUSTYP is 2 (Micro Channel). If this pin is pulled high it will indicate that the 82750PD is configured to a 16-bit Micro Channel bus. A low on this pin will configure the 82750PD for the 32-bit Micro Channel bus.

MEMTYPE (Memory Type)—This pin indicates the access method for the memory type being used. A low indicates symmetric RAMs (9 row/9 column) are used in the Shared Frame Buffer. A high indicates asymmetric RAMs (110 row/8 column) are used in the Shared Frame Buffer.

DEVID[2:0] (Device ID)—These bits identify which device the 82750PD is configured as in the system. Pulling all these pins low configures the 82750PD to "device 0", setting these pins to the value 1 (Low, Low, High) configures the 82750PD to "device 1" and so on. There is a total of eight device ID options.

Reserved—These pins are reserved and should be pulled to the value indicated.

Table 36. Bus Type Field Decode

UHBI Configuration	Number	BUSTPY[2]	BUSTYP[1]	BUSTYP[0]
EISA	0	Low	Low	Low
ISA	1	Low	Low	High
Micro Channel	2	Low	High	Low
Reserved	3	Low	High	High
PCI	4	High	Low	Low
Reserved	5	High	Low	High
Reserved	6	High	High	Low
VESA	7	High	High	High

5.2 Reset Initialization Sequence

The 82750PD is initialized as a result of the RESET input being asserted. The initialization process has several phases as shown in the timing diagram below.

Table 37. Reset Sequence Timing

Symbol	Parameter	Min	Max	Units	Notes
T1	Reset Recognition Time	67	67	MCLKs	1, 2, 3
T2	Reset Hold Time	25			3
T3	Configuration Input Setup Time	5		MCLKs	3
T4	Configuration Input Hold Time	1		MCLKs	

NOTES:
1. The RESET input is asynchronous to MCLK, however RESET must meet setup and hold times with respect to MCLK to guarantee recognition in a particular clock (see AC Characteristics).
2. Once RESET is recognized in a particular clock, there is an internal delay, before it takes effect.
3. The minimum RESET pulse width is given by T1 + T2.

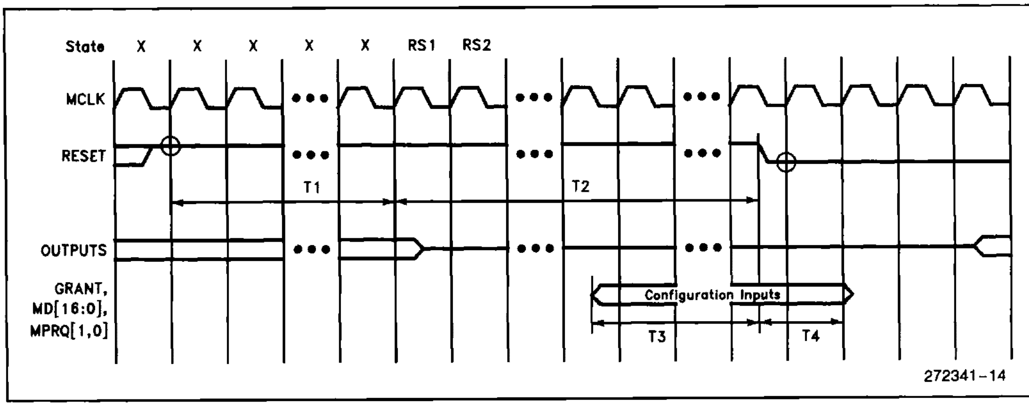


Figure 15. Reset Initialization Sequence

During the first phase (T1) of the initialization process the RESET input is synchronized to MCLK. Additionally, the RESET input is "filtered." To prevent a "false reset" from occurring, the 82750PD ensures that the RESET signal has been active for a minimum amount of time (T1) before recognizing an active RESET as valid. If the RESET input goes inactive before the minimum recognition time (T1), the RESET activation will be ignored.

If a valid reset is recognized, the 82750PD will proceed to the second phase (T2) of the initialization process. During this phase, the internal state of the 82750PD is initialized and ALL outputs are floated. During the third phase (T3) the reset configuration pins are sampled as initialization parameters (see Section 5.1 for details). These configuration parameters will be latched when RESET is deactivated (falling edge). The duration of T1 is not tested. Only the total duration T1 + T2 is tested.

6.0 BUS WAVEFORMS

This section supplements the information in Section 4. The waveforms here do not replace the information in Section 4. The figures in this section illustrate the relationships between the bus signals for the PCI interface and the signals for the SFBI. Durations of the SFBI signals are listed in terms of MCLK periods.

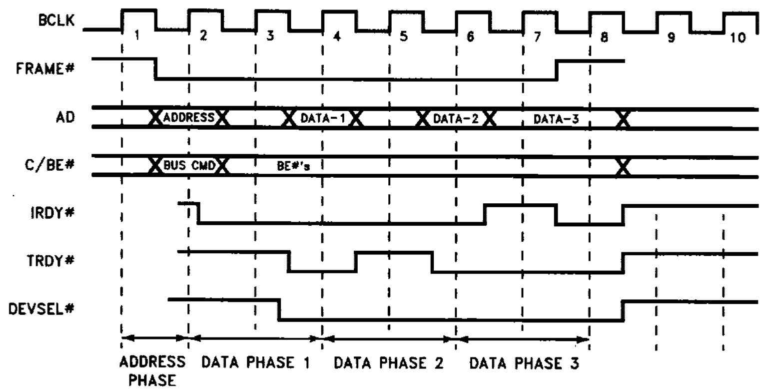


Figure 16a. PCI Waveforms: Basic Read Bus Transaction

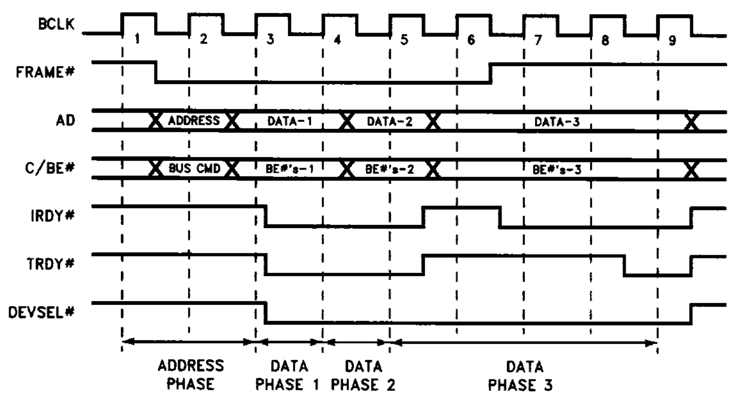
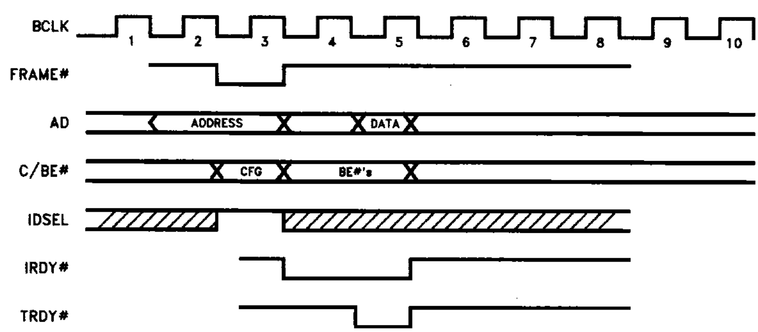


Figure 16b. PCI Waveforms: Basic Write Bus Instruction



NOTES:

1. Due to the series resistor on IDSEL the Address setup will be required during BCLK #2 for the 82750PD.
2. TRDY# will be driven low by device ID0.

Figure 16c. PCI Waveforms: Configuration Bus Transaction

Table 38. Shared Frame Buffer Interconnect Waveforms (Non-Page Mode Cycle Timings)

Symbol	Description	MCLK Periods
T1	RAS# Pulse Width	4
T2	RAS# Precharge Time	3
T3	RAS# to CAS# Delay Time	2
T4	CAS# Pulse Width	2
T5	OE# to CAS# Setup Time	1
T6	CAS# to OE# Delay	0
T7	Write Command Setup Time	1
T8	Write Command Hold Time	2
T9	Row Address Setup Time	1
T10	Row Address Hold Time	1
T11	Column Address Setup Time	1
T12	Column Address Hold Time	2
T13	Data Out Delay Time	2

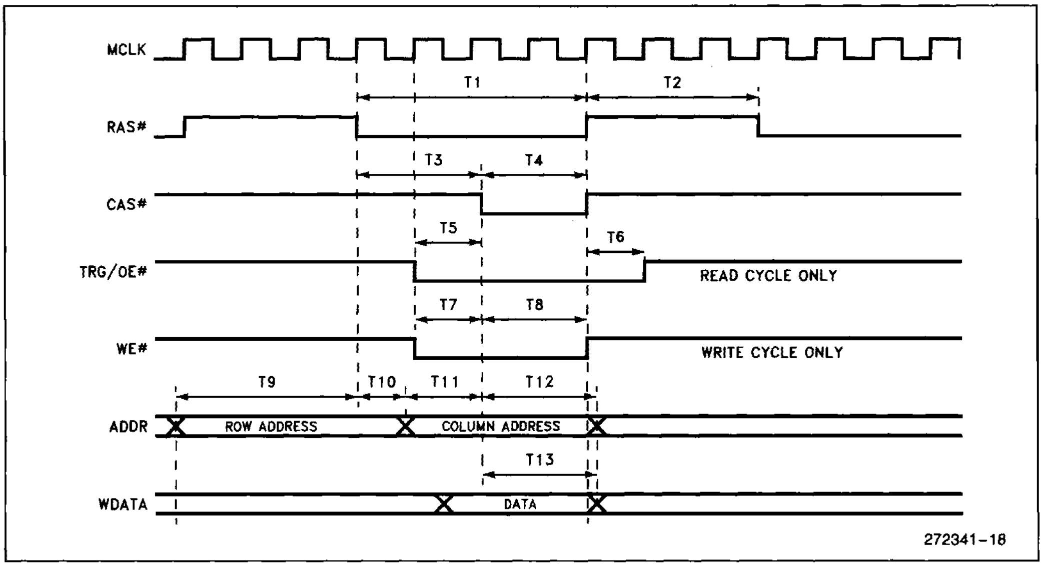


Figure 17. Shared Frame Buffer Interconnect Waveforms (Non-Page Mode Cycle Timings)

Table 39. Shared Frame Buffer Interconnect Waveforms (Fast Page Mode Cycle Timings)

Symbol	Description	MCLK Cycles
T1	RAS# to CAS# Delay Time	2
T2	RAS# Precharge Time	3
T3	CAS# Pulse Width	2
T4	CAS# Pulse Width in Page Cycle	1
T5	CAS# Precharge Time	1
T6	OE# to CAS# Setup Time	1
T7	CAS# to OE# Delay	0
T8	Write Command Setup Time	1
T9	Write Command Hold Time	2
T10	Write Command Setup Time in Page Cycle	1
T11	Write Command Hold Time in Page Cycle	1
T12	Row Address Setup Time	1
T13	Row Address Hold Time	1
T14	Column Address Setup Time	1
T15	Column Address Hold Time	2
T16	Data in Hold Time	2
T17	Data in Hold Time in Write Page Cycle	1
T18	Access Time from Column Address	3
T19	Access Time from CAS# in Read Page Cycle	1
T20	Access Time from Row Address	7
T21	Access Time from CAS#	2
T22	Access Time from Column Address in Read Page Cycle	2
T23	Access Time from RAS#	3

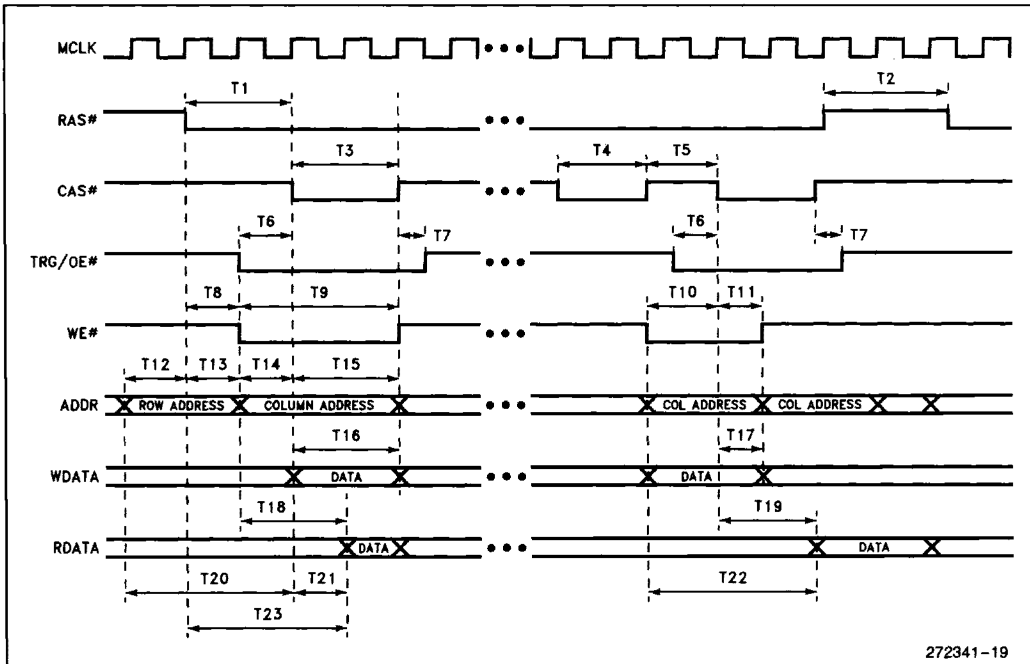


Figure 18. Shared Frame Buffer Interconnect Waveforms

Table 40. Shared Frame Buffer Interconnect Arbitration Timings (Fast Page Mode Cycle Timings)

Symbol	Description	Min (ns)	Max (ns)
T1	GRANT to RAS# Active		2TC
T2	Request Release to GRANT Inactive		2TC

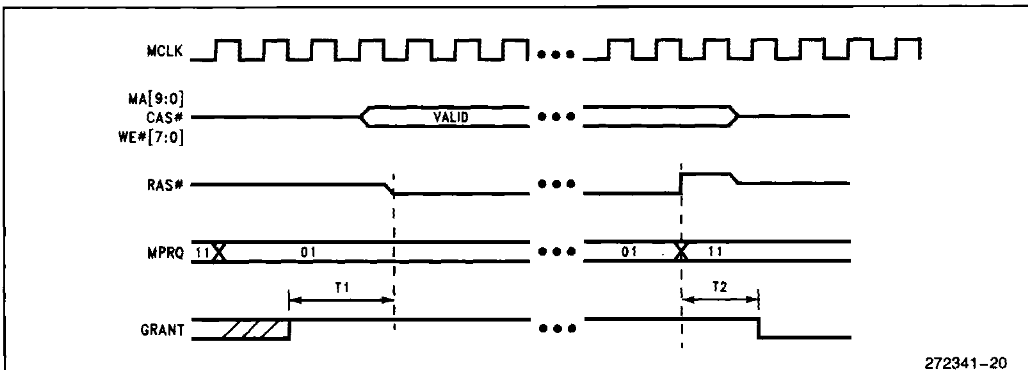


Figure 19. Shared Frame Buffer Interconnect Arbitration Timings