

# SP9920

## 50MBIT MANCHESTER DECODER WITH IDLE CODE DETECT

The SP9920 is a monolithic silicon integrated circuit for clock and data recovery from a Manchester biphasic mark encoded input signal. It operates from a single 5V supply with ECL outputs, and has an Idle Code Detect output.

### FEATURES

- 20M-50M Operating Range
- Single 5V Supply
- Sensitive Differential Input
- ECL Output
- Input Signal Detection from Lock Detect
- Output
- No False Frequency Lock
- Idle Code Detect

### APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.5V
Storage temperature	-55°C to +125°C
Operating temperature range	-40°C to +85°C

### ORDERING INFORMATION

- SP9920 DG Ceramic Package
- SP9920 MP SO Package
- SP9920 LC Chip Carrier Package

### ASSOCIATED PRODUCTS

- SP9921 50MBit Manchester Decoder
- SP9960 50MBit Manchester Decoder + LED Drive
- SP9901 50MBit Transimpedance Amplifier

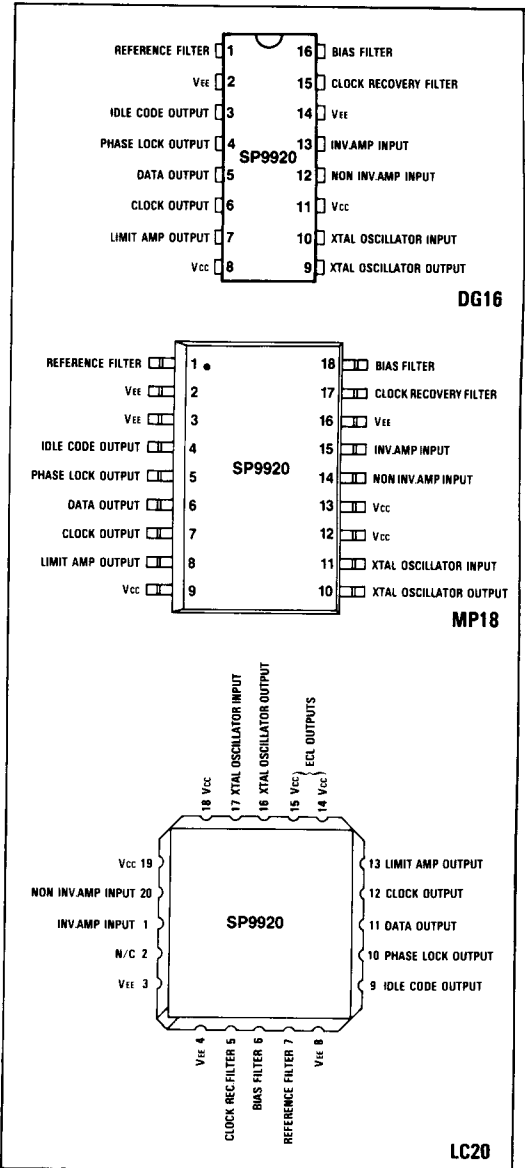


Fig.1 Pin connections - top view (not to scale)

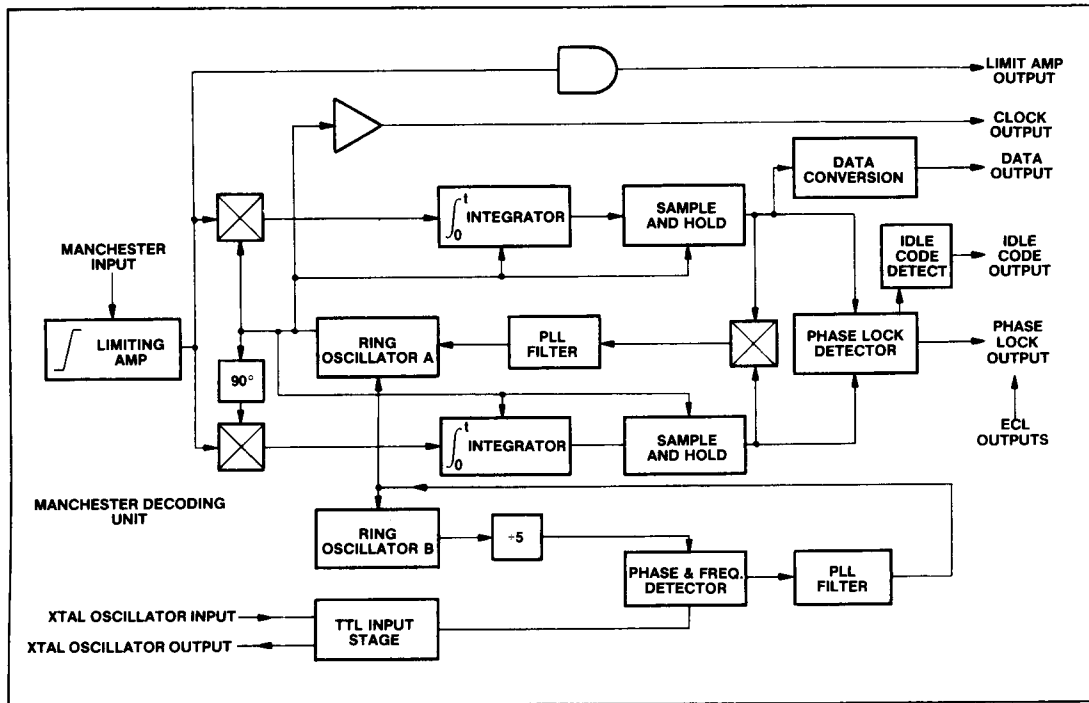


Fig.2 Block diagram of SL9920

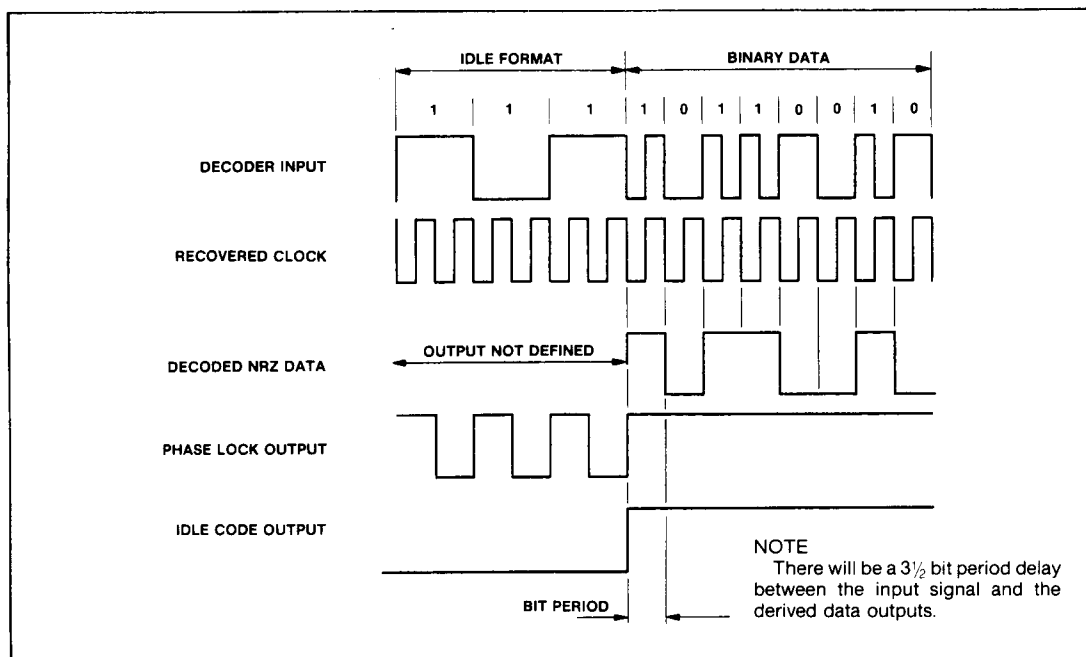


Fig.3 Timing diagram

**ELECTRICAL CHARACTERISTICS**

**Test conditions (unless otherwise stated):**

Supply voltage = 5V ± 10%. T<sub>amb</sub> = -40 °C to +85 °C

Voltages measured with respect to positive supply

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
<b>Power supply</b>					
Pins 2 & 15 - 8 & 11					
Supply voltage	-4.5		-5.5	V	
Supply current		100		mA	
<b>Limiting amplifier</b>					
Pins 12 & 13					
Differential input drive	10		1000	mV	rms
Input offset voltage			5	mV	
Input bias voltage		-2.5		V	½ supply voltage
Differential input impedance		1000		Ohms	
Pin 10					
Clock rate/REF frequency ratio		5			TTL clock ref
<b>Clock recovery PLL</b>					
PLL pull in/pull off	±10%				From centre frequency defined by REF frequency input
<b>ECL outputs (10k)</b>					
Pins 3, 4, 5, 6 & 7					
Output high voltage	-0.96		-0.81	V	
Output low voltage	-1.85		-1.65	V	
Internal pull down current		2		mA	
Output drive current			10	mA	

**OPERATING NOTES**

The circuit incorporates two phase locked loops, one acting as a frequency comparator providing bias to determine the centre operating frequency of the clock recovery circuit. The operating frequency is modified by the second loop to produce a clock signal locked to the input signal.

The SP9920 uses a crystal oscillator reference. The reference frequency is 1/5 of the signal clock frequency. The input signal is amplified by a differential limiting amplifier, with an ECL output. NRZ data output together with a clock output is provided, also with ECL levels.

A phase lock detector provides input signal detection. Decoding is accomplished by means of a Costas loop incorporating on-chip integrate and hold circuits. The loop response characteristics are determined by external resistor and capacitor forming the phase lock loop filter.

The circuit incorporates a differential limiting amplifier as an input stage, which is capable of operating with a 10mV

input signal. Output drive of the clock, data and phase lock signals are ECL compatible. A logic '1' signal is generated at the phase lock output when the data signal is greater than the error signal in the Costas loop, thus indicating the clock is in phase with the signal input. An offset is incorporated such that when no signal is present on the input the phase lock output is logic '0'.

Also provided on-chip is a crystal oscillator maintaining circuit operating at 1/5 of the input clock frequency, and an Idle Code Detect output which is an ECL 10K logic level.

The second phase lock loop is used to set up the centre operating frequency of the ring oscillator circuits. This is achieved by comparing a divided down sister oscillator (Ring Oscillator B) output with an external clock reference signal derived from the internal crystal oscillator. The ring oscillator in the Costas loop is designed such that its frequency can be pulled ±10% off the reference frequency by the phase correcting signal from the PLL filter.