SEEQ

Technology Incorporated

Full Duplex

80C240

100 Base-T4/10Base-T Ethernet Media Interface Adapter

PRELIMINARY

February 6,1997

SEEQ Hurricane™, Full Duplex Designation

HURRICANE™

SEEQ's Hurricane family of products offer 100MBit Fast Ethernet Solutions. Symbol identifies product as a part of SEEQ's Hurricane family.

Full Duplex

Symbol identifies product as Full Duplex device.

Features

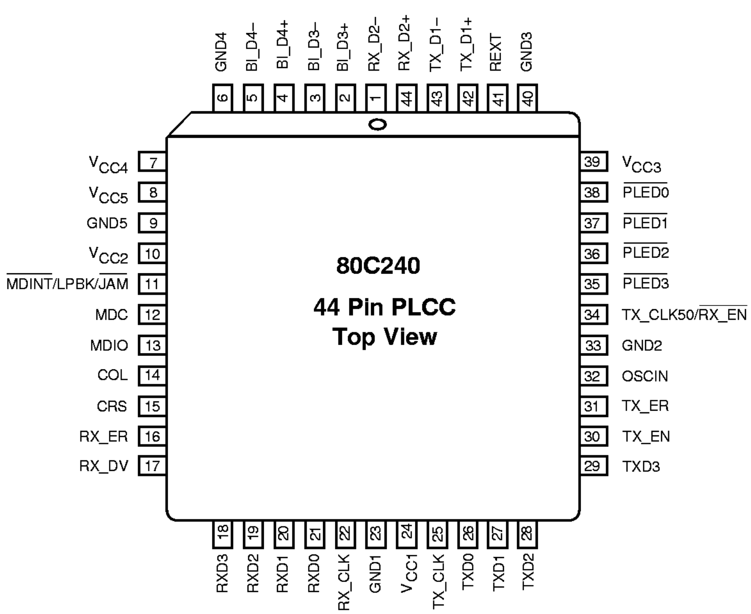
- ***100 Mbps Over Category 3/4/5 UTP Wire***
- ***Single Chip Interface Between Ethernet Controller and Twisted Pair Wire***
- ***Fully Integrated Ethernet 802.3 PHY Sublayer***
- ***On Chip Wave Shaping and Filters***
  - ***No External Filters Required***
- ***Few External Components***
- ***Meets All Applicable IEEE 802.3, 10BaseT, 100BaseT4 Standards***
- ***MII Interface To Ethernet Controller***
- ***MI Interface For Configuration & Status***
- ***AutoNegotiation For 100/10 and Full/Half Duplex Selection per IEEE 802.3 Section 28***
- ***Many User Features and Options***
  - ***Dual Speed - 10/100 Mbps***
  - ***Full Duplex***
  - ***Reverse Polarity Correction***
  - ***Smart Squelch***
  - ***Receive Level Adjust***
  - ***Powerdown***
  - ***Link Disable***
  - ***Transmit Disable***
  - ***Loopback***
  - ***MII Tristate***
  - ***Jam***

Note: Check for latest Data Sheet revision before starting any designs.

Call SEEQ Technology (510) 226-7400 x3051.

- ***Status Outputs***
  - ***Link***
  - ***Reverse Polarity***
  - ***Pair Swap***
  - ***EOP/Codeword/DC Balance Error***
  - ***Preamble Error***
  - ***Align Skew Error***
  - ***Jabber***
  - ***Full Duplex***
  - ***10/100***
  - ***AutoNegotiation Status***
  - ***Serial Port Interrupt***
- ***LED Outputs***
  - ***Link***
  - ***Activity***
  - ***Full Duplex***
  - ***10/100***
  - ***User Programmable***
- ***44L PLCC***

Pin Configuration



Hurricane is a trademark of SEEQ Technology Inc.

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1.0 Pin Description

Pin	Pin Name	I/O	Description
8 7 39 10 24	V_{CC5} V_{CC4} V_{CC3} V_{CC2} V_{CC1}	—	**Positive Supply.** +5 +/-5% Volts.
9 6 40 33 23	GND5 GND4 GND3 GND2 GND1	—	**Ground.** 0 Volts.
42	TX_D1+	O	**Twisted Pair Transmit Output, Positive, Pair 1.** This pin is an output for both 100BaseT4 and 10BaseT modes.
43	TX_D1-	O	**Twisted Pair Transmit Output, Negative, Pair 1.** This pin is an output for both 100BaseT4 and 10BaseT modes.
44	RX_D2+	I	**Twisted Pair Transmit Input, Positive, Pair 2.** This pin is an input for both 100BaseT4 and 10BaseT modes.
1	RX_D2-	I	**Twisted Pair Transmit Input, Negative, Pair 2.** This pin is an input for both 100BaseT4 and 10BaseT modes.
2	BI_D3+	I/O	**Twisted Pair Transmit Input/Output, Positive, Pair 3.** This pin is an input/output for 100BaseT4 mode only.
3	BI_D3-	I/O	**Twisted Pair Transmit Input/Output, Negative, Pair 3.** This pin is an input/output for 100BaseT4 mode only.
4	BI_D4+	I/O	**Twisted Pair Transmit Input/Output, Positive, Pair 4.** This pin is an input/output for 100BaseT4 mode only.
5	BI_D4-	I/O	**Twisted Pair Transmit Input/Output, Negative, Pair 4.** This pin is an input/output for 100BaseT4 mode only.
41	REXT	—	**Transmit Current Set.** An external resistor connected between this pin and GND will set the output current level for the transmit twisted pair outputs.
32	OSCIN	I	**Clock Oscillator Input.** There must be either a 25 Mhz crystal or a 25 Mhz clock tied between this pin and GND. TX_CLK and TX_CLK50 outputs are generated from this input.
34	TX_CLK50 ($\overline{\text{MDA4}}$)	I/O Pullup	**50 Mhz Transmit Clock Output/Management Interface Address Input.** This pin provides a 50 Mhz clock output to an external device and is synchronized to TX_CLK and OSCIN. At powerup or reset, this pin is high impedance and the value on this pin is latched in as an address for the MI serial port.
	$\overline{\text{RX\_EN}}$	I Pullup	**Receive Enable Input** 1 = Receive Controller Outputs are High Impedance 0 = Active
25	TX_CLK	O	**Transmit Clock Output.** This controller interface output provides clock to the controller. Transmit data from the controller on TXD, TX_EN, and TX_ER is clocked in on rising edges of TX_CLK and OSCIN.

Pin Description (continued)

Pin	Pin Name	I/O	Description
30	TX_EN	I	**Transmit Enable Input.** This controller interface input has to be asserted active high to indicate that data on TXD and TX_ER is valid and is clocked in on rising edges of TX_CLK and OSCIN.
29 28 27 26	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data Input.** These controller interface inputs contain nibble data to be transmitted on the TP outputs and are clocked in on rising edges of TX_CLK and OSCIN.
31	TX_ER	I	**Transmit Error Input.** This controller interface input initiates, upon assertion, a special pattern to be transmitted on the twisted pair outputs and is clocked in on rising edges of TX_CLK when TX_EN is asserted.
22	RX_CLK	O	**Receive Clock Output.** This controller interface output provides a clock to the controller. Receive data on RXD, RX_DV, and RX_ER is clocked out to the controller on falling edges of RX_CLK.
15	CRS	O	**Carrier Sense Output.** This controller interface output is asserted when valid data is detected on the receive twisted pair inputs and is clocked out on falling edges of RX_CLK.
17	RX_DV	O	**Receive Data Valid Output.** This controller interface output is asserted active high when valid decoded data is present on the RXD outputs and is clocked out on falling edges of RX_CLK.
18 19 20 21	RXD3 RXD2 RXD1 RXD0	O	**Receive Data Output.** These controller interface outputs contain receive nibble data from the TP input and are clocked out on falling edges of RX_CLK.
16	RX_ER	O	**Receive Error Output.** This controller interface output is asserted active high when a coding or other specified errors are detected on the receive twisted pair inputs and is clocked out on falling edges of RX_CLK
14	COL	O	**Collision Output.** This controller interface output is asserted when collision between transmit and receive data is detected.
12	MDC	I	**Management Interface Clock Input.** This MI clock shifts serial data into and out of MDIO on rising edges.
13	MDIO	I/O	**Management Interface Data Input/Output.** This bidirectional pin contains serial MI data that is clocked in and out on rising edges of the MDC clock.
11	$\overline{\text{MDINT}}$/ LPBK	I/O O.D. Pullup	**Management Interface Interrupt Output/Loopback Input.** When MII Controller Interface selected, this pin is an interrupt output and is asserted active low whenever there is a change in certain read MI serial port register bits, and deasserted after all changed bits have been read out. When BII Controller Interface is selected, this pin is a active high loopback input.
	$\overline{\text{JAM}}$	I Pullup	Automatic Jam Input. 1 = Normal 0 = Jam Packet Transmitted When Receive Activity Detected

Pin Description (continued)

Pin	Pin Name	I/O	Description
35	$\overline{PLED3}$ (MDA3)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** This pin can be programmed through the MI serial port to be either a Link Detect output or a user select output. This pin can drive an LED from V_{CC}. During powerup or reset, this pin is high impedance and the value on this pin is latched in as an address for the MI serial port. When programmed as Link Pulse Detect Output: 1 = No Detect 0 = Link Detected
36	$\overline{PLED2}$ (MDA2)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** This pin can be programmed through the MI serial port to be either an Activity Detect output or a user select output. This pin can drive an LED from V_{CC}. During powerup or reset, this pin is high impedance and the value on this pin is latched in as an address for the MI serial port. When programmed as an Activity Detect Output: 1 = No Activity 0 = Transmit Or Receive Packet Occurred, Hold Low For 100 mS
37	$\overline{PLED1}$ (MDA1)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** This pin can be programmed through the MI serial port to be either a Full Duplex Detect output or a user select output. This pin can drive an LED from V_{CC}. During powerup or reset, this pin is high impedance and the value on this pin is latched in as an address for the MI serial port. When programmed as Full Duplex Detect Output: 1 = Half Duplex 0 = Full Duplex
38	$\overline{PLED0}$ (MDA0)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** This pin can be programmed through the MI serial port to be either a 100 Mbps Speed Detect output or a user select output. This pin can drive an LED from V_{CC}. During powerup or reset, this pin is high impedance and the value on this pin is latched in as an address for the MI serial port. When programmed as 100/10 Mbps Speed Detect Output: 1 = 10 Mbps 0 = 100 Mbps

2.0 Block Diagram

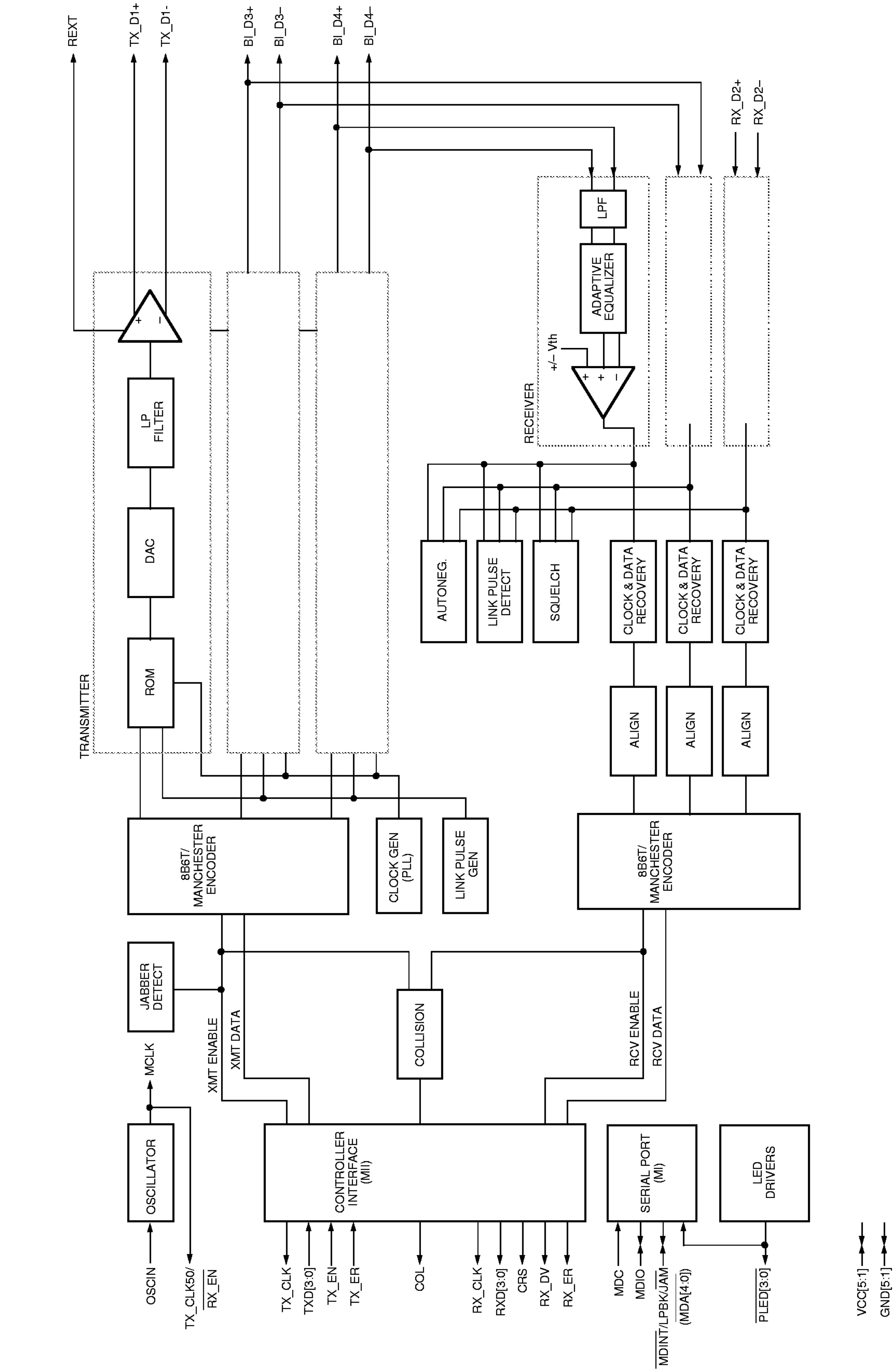


Figure 1. 80C240 Block Diagram

3.0 Functional Description

3.1 INTRODUCTION

The 80C240 is a highly integrated analog interface IC for twisted pair Ethernet applications. The 80C240 can be configured for 100 Base-T4 Ethernet operation (100 Mbps) or 10Base-T Ethernet operation (10 Mbps). The 80C240 integrates the entire PHY Sublayer as defined in IEEE 802.3 Section 23.

The 80C240 consists of 8B6T/Manchester encoder, twisted pair transmitter with wave shaping and on chip filters, twisted pair transmit output driver, twisted pair receiver with on chip equalizer and filters, clock and data recovery, 8B6T/Manchester decoder, controller interface (MII), and serial port (MI).

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters and common mode chokes normally required in 100BaseT4 and 10BaseT applications.

The 80C240 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with an AutoNegotiation algorithm compliant to IEEE 802.3 Section 28.

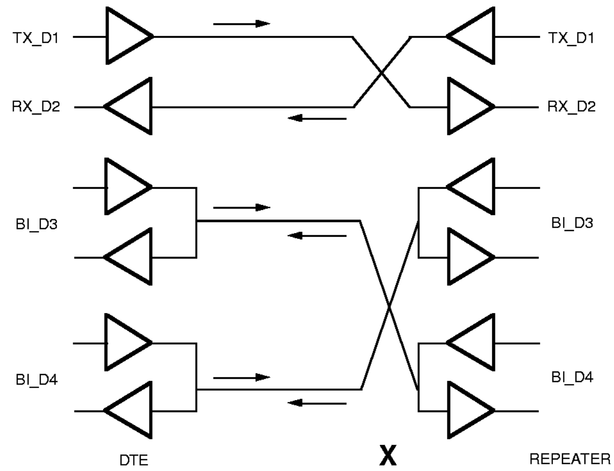
The 80C240 can access ten registers through the MI serial port. These registers contain configuration inputs, status outputs, and device capabilities.

The 80C240 is ideal as a media interface for 100BaseT4/10BaseT adapter cards, motherboards, switching hubs, managed hubs, and external PHY's.

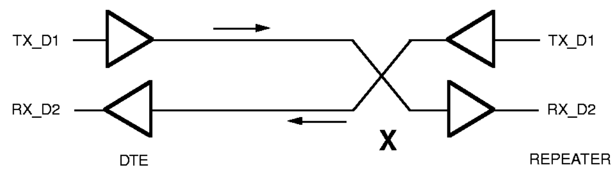
3.2 GENERAL

The 80C240 is a complete 100/10 Mbps Ethernet Media Interface IC. The 80C240 has nine main sections: controller interface, encoder, decoder, clock and data recovery, aligner, twisted pair transmitter, twisted pair receiver, MI serial port, and crystal oscillator. A block diagram is shown in Figure 1.

The 80C240 can operate as a 100Base-T4 device (hereafter referred to 100 Mbps mode) or as a 10Base-T device (hereafter referred to as 10 Mbps mode). The difference in data rate between the 100 Mbps mode and 10 Mbps mode is primarily due to the usage of the twisted pairs. The 10 Mbps mode uses 2 pairs (one for transmit and one for receive) with Manchester encoded 10 Mhz binary data to achieve a 10 Mbps thruput. The 100 Mbps mode uses 4 pairs (three for transmit/receive and one for collision) with 8B6T encoded 12.5 Mhz ternary data to achieve a thruput of 100 Mbps. This wire usage is shown in Figure 2 and complies with the IEEE 802.3 specifications. The data



a.) 100 BASE-T4 MODE



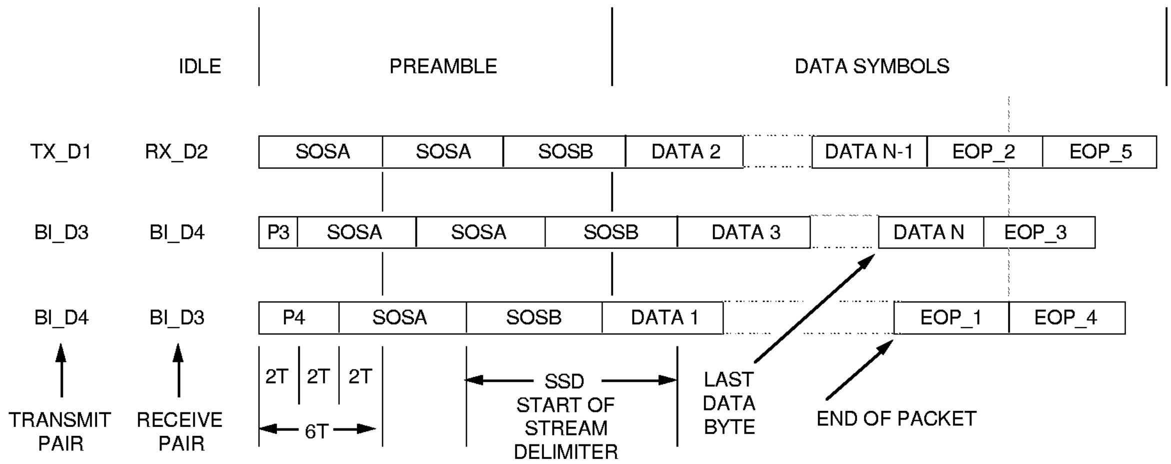
b.) 10 BASE-T MODE

Figure 2. Twisted Pair Wire Usage

symbol format on the twisted pair cable for the 100 and 10 Mbps modes are also defined in the IEEE 802.3 specifications and shown in Figure 3.

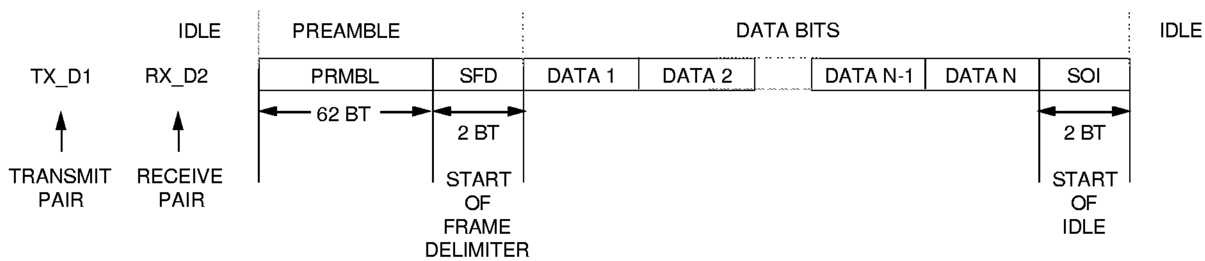
On the transmit side for 100 Mbps operation, NRZ data is received on the controller interface from an external Ethernet controller per the format shown in Figure 4. The NRZ data is then sent to the encoder for formatting and encoding into three parallel channels. The three channels of encoded data are then sent to three TP transmitters. The TP transmitter is composed of a waveform generator that preshapes the output, a filter to remove high frequency components, and an output driver to drive the 100 ohm twisted pair cable. In addition, the transmitter generates link pulses.

On the receive side for 100 Mbps operation, three twisted pair receivers receive incoming encoded data from the twisted pair cable, remove high frequency noise from the input, equalizes the input signal to compensate for the effects of the cable, and then converts the data from twisted pair levels to internal digital levels. The twisted pair receiver also detects link pulses, implements the autoconfiguration algorithm, detects and corrects for reverse polarity on the twisted pair inputs, and implements a



sosa	=	[1 –1 1 –1 1 –1]
sosb	=	[1 –1 1 –1 –1 1]
eop1	=	[1 1 1 1 1 1]
eop2	=	[1 1 1 1 –1 –1]
eop3	=	[1 1 –1 –1 0 0]
eop4	=	[–1 –1 –1 –1 –1 –1]
eop5	=	[–1 –1 0 0 0 0]
bad_code	=	[–1 –1 –1 1 1 1]
zero_code	=	[0 0 0 0 0 0]
P3		[1 –1]
P4		[1 –1 1 –1]

a). 100 Base-T4



PRMBL = [1 0 1 0 .....] 62B LONG

SFD = [1 1]

SOI = [1 1] WITH NO MID BIT TRANSITION

b). 10Base-T

Figure 3. Twisted Pair Data Symbol Format

squelch algorithm to reject invalid signals. The output of the twisted pair receivers then goes to three clock and data recovery blocks which recovers a clock from each of the three TP data streams, recovers the data for each of the three data streams, and converts the data back to NRZ per the format shown in Figure 4. The three NRZ data channels are then realigned to eliminate any skew by the aligner section. The deskewed NRZ data is then decoded and unformatted by the decoder and transmitted to an external Ethernet controller through the controller interface.

10 Mbps operation is similar to the 100 Mbps operation except, (1) 10 Mbps operation has a single transmit channel and a single receive channel, and (2) 10 Mbps operates at lower data rate.

The MI (Management Interface) serial port is a bidirectional port through which configuration inputs can be set and status outputs can be read. A crystal oscillator generates a master clock for the device.

Each block plus the operating modes are described in more detail in the following sections. Since the 80C240 can operate either as a 100BaseT4 or a 10BaseT device, each of the following sections describes the performance of the respective section in both 100 and 10 Mbps modes.

3.3 CONTROLLER INTERFACE

3.3.1 General

The 80C240 has two interfaces to an external controller: Media Independent Interface (MII) and Bit Wide Interface (BII). The MII operates at both 100 and 10 Mbps, but the BII operates at only 10 Mbps. The selection of MII or BII is done by setting the controller interface bit in the MI serial port Configuration 1 register.

3.3.2 Media Independent Interface (MII) - 100 Mbps

The MII is a nibble wide packet data interface defined in IEEE 802.3 and shown in Figure 4. The 80C240 meets all the MII requirements outlined in IEEE 802.3. The 80C240 can directly connect, without any external logic, to any Ethernet controllers which also complies with the IEEE 802.3 MII specifications.

The MII consists of eighteen signals: four transmit data bits (TXD[3:0]), transmit clock (TX_CLK), transmit enable (TX_EN), transmit error (TX_ER), four receive data bits (RXD[3:0]), receive clock (RX_CLK), carrier sense (CRS), receive data valid (RX_DV), receive data error (RX_ER), and collision (COL). The transmit and receive clocks operate at 25 MHz in 100 Mbps mode.

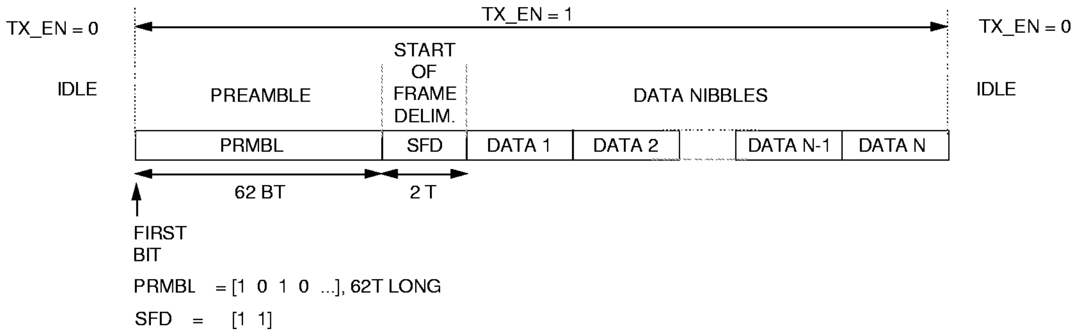
On the transmit side, when TX_EN is deasserted, no data is clocked into the device. When TX_EN is asserted on rising edge of TX_CLK, data on TXD[3:0] is clocked into the device on rising edges of the TX_CLK clock output. TXD[3:0] input data is nibble wide packet data whose format needs to be the same as specified in IEEE 802.3 and shown in Figure 4. When the data on TXD[3:0] has been latched into the device, TX_EN is deasserted on rising edge of TX_CLK.

TX_ER is also clocked in on rising edges of the TX_CLK clock. TX_ER is a transmit error signal which, when asserted, will substitute an error byte in place of the normal data byte that was clocked in on the two TXD[3:0] nibbles at that time. The error byte is defined in the IEEE 802.3 specification. Since the TX_ER error byte is two nibbles long, TX_ER must be asserted high for two TX_CLK clock cycles. If TX_ER is asserted during preamble, the preamble and SSD are transmitted unaltered and the first data byte is replaced with the error byte. If an odd number of nibbles have been clocked into the device, TX_EN and TX_CLK are extended an additional clock cycles and the error byte is inserted for the last two data nibbles.

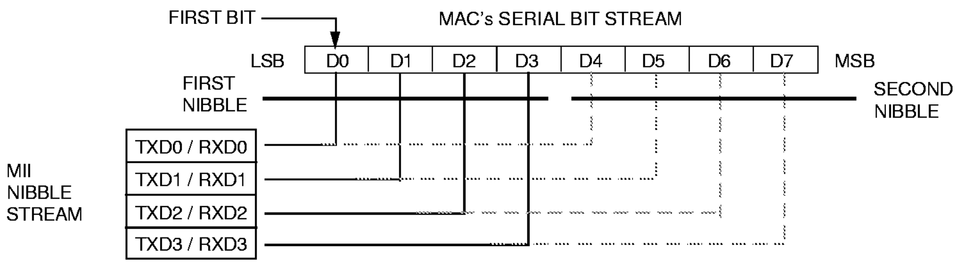
Since OSCIN input clock generates the TX_CLK output clock, TXD[3:0], TX_EN, and TX_ER are also clocked in on rising edges of OSCIN. There is an additional 50 MHz clock output, TX_CLK50, generated from OSCIN which is available for external use and does not change frequency when 100/10 Mbps mode changes.

On the receive side, when invalid data is sensed on the TP inputs, the receiver is idle. During idle, RX_CLK follows TX_CLK, RXD[3:0] is held low, and CRS, RX_DV, and RX_ER are deasserted. When a valid packet is detected on the TP receive inputs, CRS is asserted and the clock recovery process starts on the incoming data. After the receive clock has been recovered from the data, the RX_CLK is switched over to the recovered clock and the data valid signal RX_DV is asserted on a falling edge of RX_CLK. While RX_DV is asserted, valid data is clocked out on RXD[3:0] on falling edges of the RX_CLK clock. The RXD[3:0] data has the same packet format as the TXD[3:0] data and is specified in IEEE 802.3 and shown in Figure 4. When the end of packet is detected, CRS and RX_DV are deasserted. CRS and RX_DV also stay deasserted as long as the device is in the Link Fail State.

RX_ER is a receive error output which is asserted when certain errors defined in IEEE 802.3 specifications are detected on a data byte. Since the receive errors are detected on a byte basis and data is outputted in nibbles



a.) MII Frame Format



b.) MII Nibble Order

Signals	Bit Value																			
TXDO	X	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
TXD1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st preamble nibble transmitted.
2. 1st sfd nibble transmittted.
3. 1st data nibble transmitted.
4. D0 thru D7 are the first 8 bits of the data field.

c.) Transmit Preamble and SFD bits

Signals	Bit Value																			
RXDO	X	X	X	X	X	X	X	X	X	X	X	X	1[1]	1	1	1	1[2]	1	D0[3]	D4[4]
RXD1	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

1. 1st preamble nibble received.
2. 1st sfd nibble received.
3. 1st data nibble received.
4. D0 thru D7 are the first 8 bits of the data field.

d.) Receive Preamble and SFD Bits

Figure 4. MII Data Packet Format

transmitters. In order to do this, the 8B6T encoder strips on RXD[3:0], RX_ER is asserted for two RX_CLK cycles during the same time that the two nibbles containing the error are being outputted.

The collision output, COL, is asserted whenever the collision condition is detected.

3.3.3 MII - 10 Mbps

10 Mbps operation is identical to the 100 Mbps operation except, (1) TX_CLK and RX_CLK clock frequency is reduced to 2.5 MHz, (2) TX_ER is ignored, and (3) RX_ER is disabled and always held low.

3.3.4 BII - 10 Mbps

The bit wide interface is available in 10 Mbps mode only. When BII is selected, the controller interface is identical to MII 10 Mbps except, (1) data is inputted/outputted bit wide (not nibble wide) on TXD0/RXD0 only, and (2) TX_CLK and RX_CLK clock are both 10 Mhz.

3.3.5 MII Disable

The MII and BII inputs and outputs can be disabled by setting the MII disable bit in the MI serial port Control register. If the MI address lines are pinstrapped to all 1's, the 80C240 powers up and reset with the MII inputs disabled, MII outputs in high impedance state, and TP transmitter disabled. Otherwise, the 80C240 powers up and resets with the MII inputs and outputs and TP outputs enabled.

3.3.6 Receive Output Disable

The TX_CLK50/RX_EN pin (pin 34) can be configured to be RX_EN, a high impedance control for the receive controller output signals. When RX_EN is asserted high, then RX_CLK, RXD[3:0], RX_DV, RX_ER, and COL outputs are placed in high impedance state. TX_CLK50/RX_EN can be configured to be RX_EN by setting the pin 34 configuration select bit in the MI serial port Configuration 1 register. When TX_CLK50/RX_EN is configured to be RX_EN, the MI address MDA4 is tied high internally and the TX_CLK50 function is disabled.

3.3.7 Programmable CRS Delay

The delay of CRS from the start of the receive packet can be adjusted with the CRS assert delay select bit in the MI serial port Configuration 1 register. The CRS assert delay can be selected to be either 215-275 nS (DTE) or 0-155 nS (repeater). When the CRS assert delay bit is set for repeater mode, the internal TX_EN to CRS loopback path is disabled.

3.4 ENCODER

3.4.1 8B6T Encoder - 100 Mbps

The 8B6T encoder converts the NRZ data from the controller interface into three data streams for the three TP off preamble and SFD bits from the NRZ input data, encodes 8 data bits into 6 ternary data symbols, partitions the data streams into three separate channels, adds start of stream (SOS) and start of stream delimiter (SSD) symbols to all three channels, and adds end of packet (EOP) symbols to all three channels as required by IEEE 802.3 and as shown in Figure 3. The 8B6T encoding algorithm is specified in IEEE 802.3. 8B6T encoding of the NRZ data occurs only when TX_EN is asserted.

3.4.2 Manchester Encoder - 10 Mbps

The Manchester encoder converts the 10 Mbit NRZ data from the controller interface into a single Manchester encoded serial data stream and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3 and shown in Figure 3. The Manchester encoding process combines clock and data such that the first half of the bit cell contains the complement of the data, and the second half of the bit cell contains the true data, as specified in IEEE 802.3. This guarantees that a transition always occurs in the middle of the bit cell. Manchester encoding of the NRZ data occurs only when TX_EN is asserted.

3.5 DECODER

3.5.1 8B6T Decoder - 100 Mbps

The 8B6T decoder converts the three data streams from the three receivers into NRZ data for the controller interface. The 8B6T decoder strips off SOS, SSD, and EOP ternary symbols, decodes 6 ternary data symbols into 8 data bits, and partitions the 8 data bits into 2 data nibbles as required by IEEE 802.3 specifications. The 8B6T decoding algorithm for the ternary symbols is specified in IEEE 802.3. 8B6T decoding of the ternary data occurs only when valid data is detected on the three receive TP inputs.

The decoder detects end of packet, codeword, DC balance, and preamble errors in the incoming data stream as specified in the IEEE 802.3. These errors are indicated by asserting RX_ER output pin and by setting end of packet, codeword, DC balance, and preamble error bits in the MI serial port Status Output register.

3.5.2 Manchester Decoder - 10 Mbps

The Manchester decoder converts the single data stream from the TP receiver into NRZ data for the controller interface by stripping off the SOI pulse and then decoding the data. In Manchester encoded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. Since the clock and data recovery block separates the clock and data from the TP receiver data stream, the Manchester decoding process is inherently performed by that block.

3.6 CLOCK AND DATA RECOVERY

3.6.1 Clock Recovery - 100 Mbps

There are three separate clock recovery blocks for each of the three incoming TP data streams. Clock recovery is done with a PLL. When valid data is detected on the TP receive input, the PLL input is switched to the incoming data. The PLL then recovers the clock by locking onto zero crossings of the preamble of the incoming signal from the twisted pair wire. The recovered clock frequently is 25 Mhz. The PLL can lock onto the preamble signal in less than 10 transitions (bit times) and can reliably perform the data recovery process with up to ±9.5 nS of jitter on the TP input. While the PLL is in the process of locking onto the preamble signal, some of the preamble data symbols are lost. However, the clock recovery recovers enough preamble data symbols to pass at least 6 nibbles of preamble to the receive controller interface as required by the IEEE 802.3 specification and shown in Figure 4.

3.6.2 Data Recovery - 100 Mbps

There are three separate data recovery blocks for each of the three incoming TP data streams. Data recovery is done by latching in data from TP receiver with the recovered clock extracted by the PLL.

3.6.3 Clock Recovery - 10 Mbps

The clock recovery process for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the clock is recovered from only one TP input, (2) the recovered clock frequency is 10 Mhz and (3) at least 8 nibbles of preamble data are passed to the receive controller interface.

3.6.4 Data Recovery - 10 Mbps

The data recovery process for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the data is recovered from only one TP input, and (2) the recovery clock frequency is 10 MHz. As mentioned in the Manchester Decoder section, the data recovery process inherently decodes Manchester encoded data.

3.7 ALIGNER

3.7.1 100 Mbps

The three data streams on the TP receive inputs might not be perfectly aligned in time and may be skewed with respect to each other. The aligner removes any time skew between the three input data streams and synchronizes the three data streams to a single clock edge for easier decoding. The aligner can compensate for up to 90 nS of time delay difference or align skew error between the three incoming bit streams. If the align skew error is greater than 120 nS, then the align skew error bit is set in the MI serial port Status Output register.

The 80C240 can detect up to three errors in the preamble as required in the IEEE 802.3 specification. Preamble error is reported by asserting RX_ER for the entire packet and by asserting the preamble error bit in the MI serial port Status Output register.

3.7.2 10 Mbps

The aligner is disabled in 10 Mbps mode.

3.8 TWISTED PAIR TRANSMITTER

3.8.1 Transmitter - 100 Mbps

The transmitter consists of a waveform generator and line driver.

The purpose of the waveform generator is to shape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM outputs; the ROM outputs are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Section 23 and also shown in Figure 5. The transmitter also meets the transmit ISI requirements outlined in IEEE 802.3 Section 23 and shown in Figure 6. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 3/4/5 twisted pair cable tied directly to the TP output pins without any external filters. During the idle period, no output signal is transmitted on the TP outputs (except link pulse).

The 80C240 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most applications.

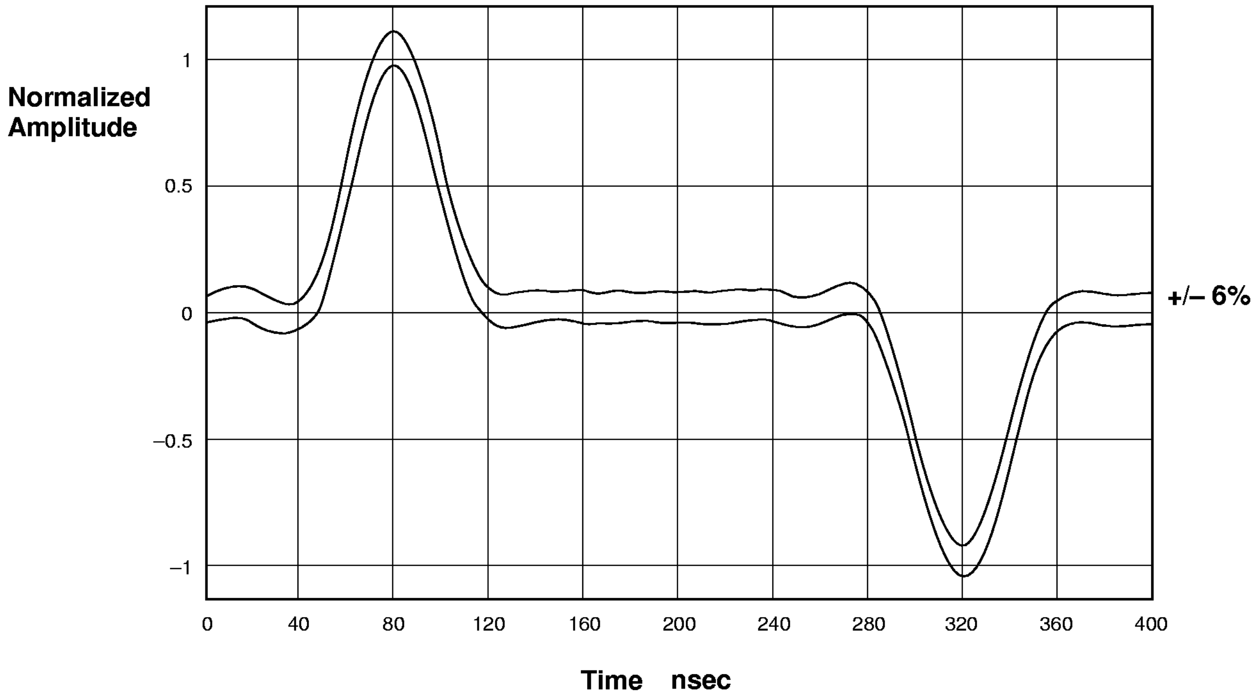


Figure 5. TP Output Voltage Pulse Template - 100 Mbps

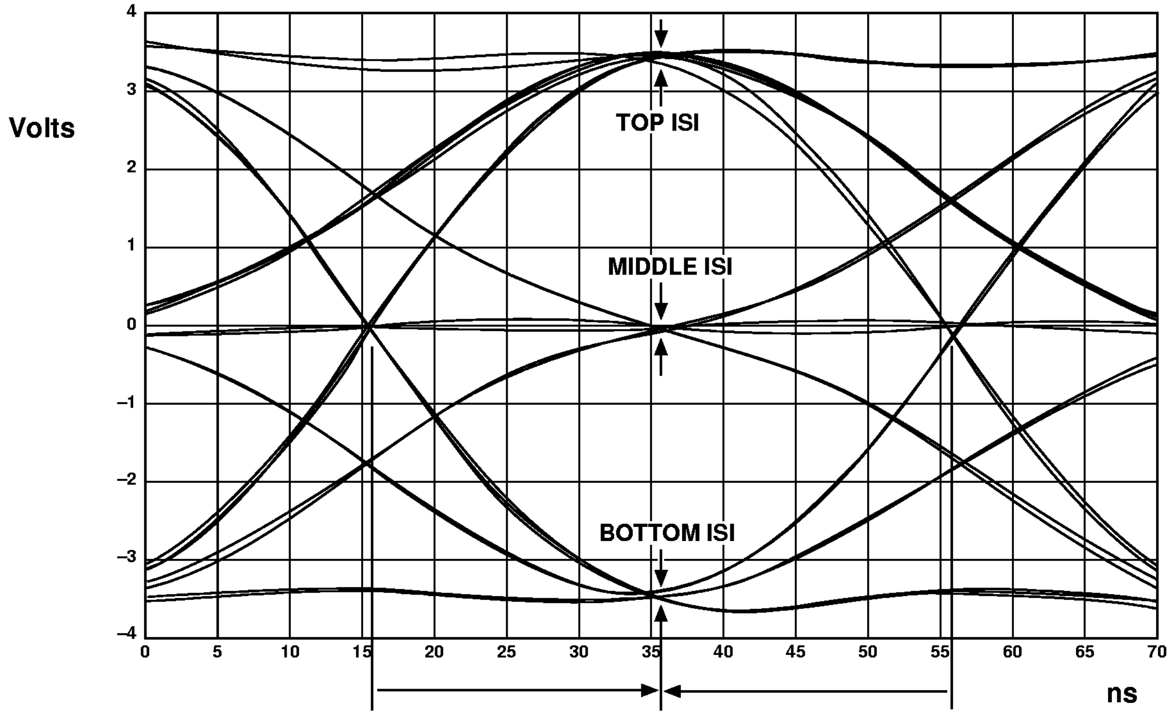


Figure 6. TP Output Voltage ISI Template - 100 Mbps

3.8.2 Transmitter - 10 Mbps

The transmitter operation in 10 Mbps mode is identical to the 100 Mbps mode except, (1) the output template is modified, by digitally altering the ROM addresses, to meet the transmit output pulse template requirements outlined in IEEE 802.3 Section 14 and also shown in Figure 7.

3.8.3 Optional Reference Voltage Input

The transmit output current level is derived from an internal reference voltage and the external resistor on REXT pin. The internal reference voltage is derived from V_{CC}. The internal reference voltage can be accessed externally and overridden by setting the external VREF bit in the MI serial port Configuration 1 register and by applying an external reference voltage to the $\overline{MDINT}$/LPBK/$\overline{JAM}$ pin. When this bit is set, the interrupt function is disabled and the Jam and BII interface modes are unavailable. The 80C240 meets all the IEEE 802.3 output level requirements with the internal reference and 5% supply tolerance.

3.8.4 Transmit Activity Indication

Transmit activity can be programmed to appear on the $\overline{PLED2}$ pin by setting the programmable LED output select bits in the MI serial port LED Configuration 1 register. When the $\overline{PLED2}$ pin is programmed to be an activity detect output, this pin is asserted low for 100 mS every time a transmit or receive packet occurs. The $\overline{PLED2}$ output is open drain with resistor pullup and can drive an LED from V_{CC} or can drive another digital input.

3.8.5 Transmit Disable

The TP transmitter can be disabled by setting the transmit disable bit in the MI serial port Configuration 1 register. When the transmit disable bit is set, the TP transmitter is forced into the idle state, no data is transmitted, no link pulses are transmitted, and internal loopback is disabled.

3.9 Twisted Pair Receiver

3.9.1 Receiver - 100 Mbps

There are three separate receivers for each of the three TP inputs. The three TP receivers detect input signals from the three twisted pair inputs and convert them to three digital data streams ready for clock and data recovery. The receivers can reliably detect data from a 100Base-T4 compliant transmitter that has been passed through 0-100 meters of 100 ohm UTP category 3/4/5 twisted pair cable.

Each receiver consists of a low pass filter, adaptive equalizer, and comparators. The TP receiver inputs first pass through a low pass filter designed to eliminate any high frequency noise on the input. The signal then goes to an adaptive equalizer. The adaptive equalizer compensates for the low pass characteristic of the cable, and it has the ability to adapt and compensate for 0-100 meters of category 3/4/5 UTP 100 ohm twisted pair cable. The comparators convert the equalized signal to digital levels.

3.9.2 Receiver - 10 Mbps

The 10 Mbps mode receiver is identical to the 100 Mbps mode receiver except, (1) the receiver is single channel only, (2) the receiver is able to detect input signals from the twisted pair cable that is within the template shown in Figure 8, (3) the adaptive equalizer is disabled (set to zero cable length adjustment), and (4) the output of the squelch comparator is used for squelch, link pulse detect, SOI detect, reverse polarity detect.

3.9.3 Squelch - 100 Mbps

The squelch block determines if the TP input contains valid data. There are three separate squelch blocks for each of the three TP receive inputs. Each squelch block has a squelch comparator which compares the TP input against fixed positive and negative thresholds, called squelch levels. The output from the squelch comparator goes to a digital squelch circuit which determines if the receive input data on that channel is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels for three bit times with alternating polarity starting with the first negative going transition within a 40-80 nS interval, the data is considered to be valid for that channel and the receiver now enters into the unsquelch state. When all three squelch circuits are in the unsquelch state, that is, all three squelch circuits detect valid data, then the input signal is deemed to be valid and CRS is asserted. The device stays in the unsquelch state until the end of packet is detected. End of packet is detected when either EOP1 is detected on one of the three channels by the decoder or 7 consecutive 0's are detected on input RX_D2±. When the end of packet is detected, the receive squelch is turned on again and CRS and RX_DV are deasserted. The receiver meets the squelch requirements defined in IEEE 802.3 Section 23.

3.9.4 Squelch, 10 Mbps

The TP squelch algorithm for 10 Mbps mode is identical to the 100 Mbps mode except, (1) there is only one TP receive input channel, (2) the receiver goes into the unsquelch state if the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 100-250 nS interval, (3) in the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. (4) the end of packet is detected when the SOI (Start Of Idle) pulse is sensed, and (5) the receiver meets the squelch requirements defined in IEEE 802.3 Section 14.

3.9.5 Equalizer Disable

The adaptive equalizer can be disabled (or enabled) by setting the equalizer disable bit in the MI serial port

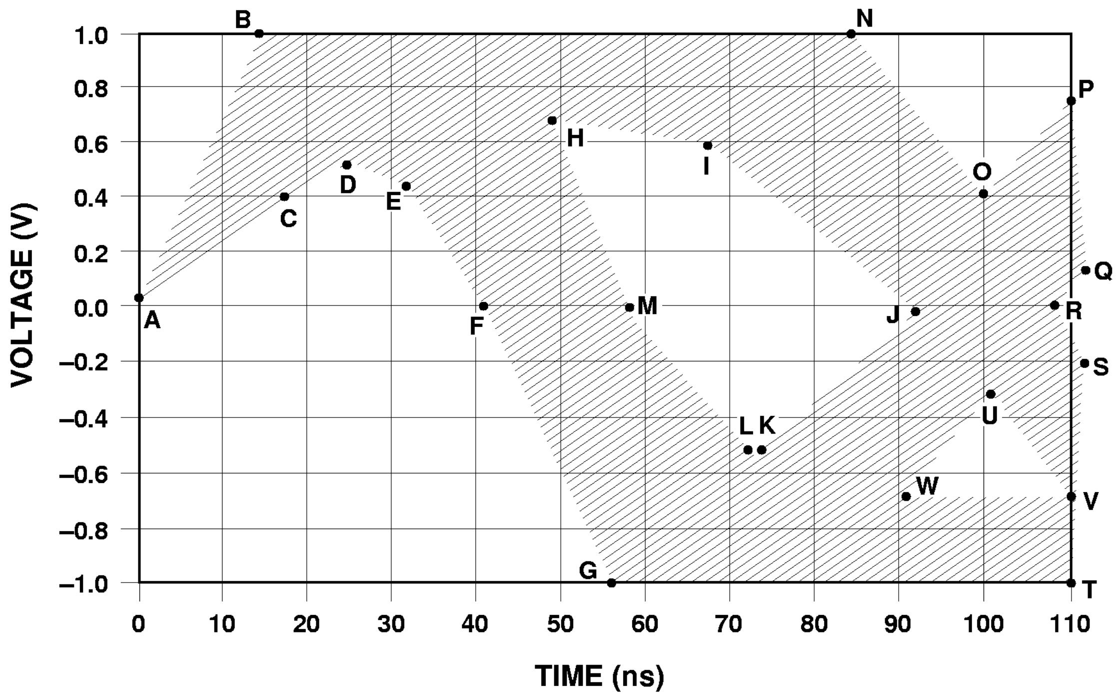


Figure 7. TP Output Voltage Template-10 Mbps

Voltage Template Values for Figure 7

Reference	Time (ns) Internal MAU	Voltage (V)
A	0	0
B	15	1.0
C	15	0.4
D	25	0.55
E	32	0.45
F	39	0
G	57	-1.0
H	48	0.7
I	67	0.6
J	89	0
K	74	-0.55
L	73	-0.55
M	61	0
N	85	1.0
O	100	0.4
P	110	0.75
Q	111	0.15
R	111	0
S	111	-0.15
T	110	-1.0
U	100	-0.3
V	110	-0.7
W	90	-0.7

Configuration 1 register. When disabled, the equalizer is forced into the response it would normally have if zero cable length was detected. When in 100 Mbps mode, the equalizer defaults to the enabled position; in 10 Mbps mode, the equalizer defaults to the disabled position.

3.9.6 Receive Activity Detection

Receive activity can be programmed to appear on the PLED2 pin by setting the programmable LED output select bits in the MI serial port Configuration 2 register. When the PLED2 pin is programmed to be an activity detect output, this pin is asserted low for 100 mS every time a transmit or receive packet occurs. The PLED2 output is open drain with resistor pullup and can drive an LED from V_{CC} or can drive another digital input.

3.9.7 Receive Level Adjust

The receiver squelch and unsquelch levels can be lowered by 4.5 dB by setting the receive level adjust bit in the MI serial port Configuration 1 register. By setting this bit, the device can support cable lengths exceeding 100 meters.

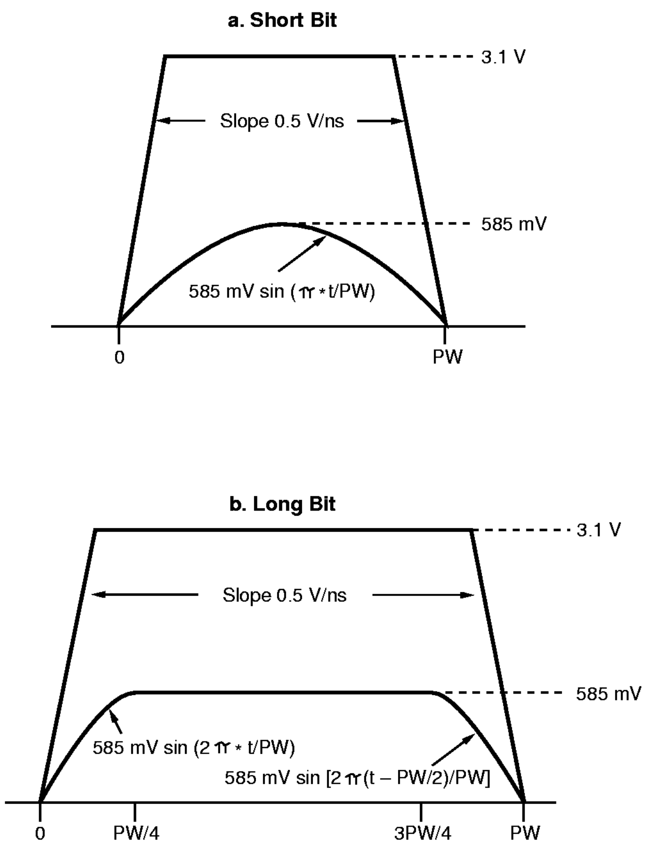


Figure 8. TP Input Voltage Template-10 Mbps

3.10 END OF PACKET

3.10.1 100 Mbps

The end of packet for 100 Mbps mode is signaled on each channel by a unique EOP (End of Packet) data pattern as defined in IEEE 802.3 Section 23 and shown in Figure 3.

The transmit EOP1-5 patterns are generated by the 8B6T encoder and inserted at the end of the transmit data packet on each channel. The EOP1-5 patterns are not fixed to any specific channels. The channel that finishes its data packet first appends EOP1 after the last data packet, EOP2 is appended to the next channel in sequence, etc. as shown in Figure 3.

The receive EOP patterns are detected by the 8B6T decoder. Once the EOP1 pattern is detected on any receive channel or if 7 consecutive 0's are detected on RX_D2±, data reception is ended and CRS and RX_DV are deasserted. If 7 consecutive 0's are detected but no EOP1 is detected, RX_ER is asserted on the last two MII data nibbles.

3.10.2 10 Mbps

The end of packet for 10 Mbps mode is signaled with the SOI (Start of Idle) pulse. The SOI pulse is a positive double wide pulse inserted at the end of every packet .

The TP transmitter generates an SOI pulse at the end of data transmission after TX_EN is deasserted. The TP transmitted SOI output pulse is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Section 14 and shown in Figure 9.

The TP receiver detects the SOI pulse by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and CRS and RX_DV are deasserted.

3.11 LINK INTEGRITY & AUTONEGOTIATION

3.11.1 General

The 80C240 can be configured to implement either the standard link integrity algorithm or the AutoNegotiation algorithm.

The standard link integrity algorithm is used to indicate and establish an active link to and from a remote device. The standard link integrity algorithm is different for 100Base-T4 and 10Base-T modes. The standard link integrity algorithm for 100Base-T4 mode is the same as specified in IEEE 802.3 Section 23. The standard link integrity algorithm for 10Base-T mode is the same as specified in IEEE 802.3 Section 14.

The AutoNegotiation algorithm is used to indicate and establish an active link to and from a remote device as well as automatically configuring the device for either 100Base-T4, 10Base-T Full Duplex, or 10Base-T Half Duplex modes depending on the highest common denominator operating mode. The AutoNegotiation algorithm is the same as specified in IEEE 802.3 Section 28. The AutoNegotiation algorithm also will interoperate with a remote device that may not have the AutoNegotiation algorithm but only the 100Base-T4 or 10Base-T standard algorithms.

The selection of the standard link integrity algorithm or AutoNegotiation algorithm is done with the AutoNegotiation enable bit in the MI serial port Control register.

3.11.2 10Base-T Link Integrity Algorithm

The transmit and receive 10Base-T algorithms are the same as defined in IEEE 802.3 Section 14. The 10Base-T algorithm uses normal link pulses, or NLP's to establish link integrity. The transmit link pulse meets the template defined in IEEE 802.3 Section 14 and shown in Figure 10. Refer to IEEE 802.3 Section 14 for more details.

3.11.3 100Base-T4 Link Integrity Algorithm

The transmit and receive 100Base-T4 algorithms are the same as defined in IEEE 802.3 Section 23. The 100Base-T4 algorithm uses T4 link pulses, or T4LP's to establish link integrity. The transmit link pulse meets the template defined in IEEE 802.3 Section 23 and shown in Figure 11. Refer to IEEE 802.3 Section 23 for more details.

3.11.4 AutoNegotiation Algorithm

The transmit and receive AutoNegotiation algorithms are the same as defined in IEEE 802.3 section 28. The AutoNegotiation algorithm uses a burst of link pulses, called fast link pulses or FLPs, to pass up to 16 bits of signaling data back and forth between the 80C240 and a remote device. The transmit FLP pulses meet the template defined in IEEE 802.3 Section 14 and shown in Figure 10. A timing diagram contrasting NLP's, T4LP's and FLP's is shown in Figure 12.

The FLP's are used to advertise the device capabilities to a remote device. The selection of advertised capabilities for the 80C240 is done by setting the appropriate bits in the MI serial port AutoNegotiation Advertisement register. In

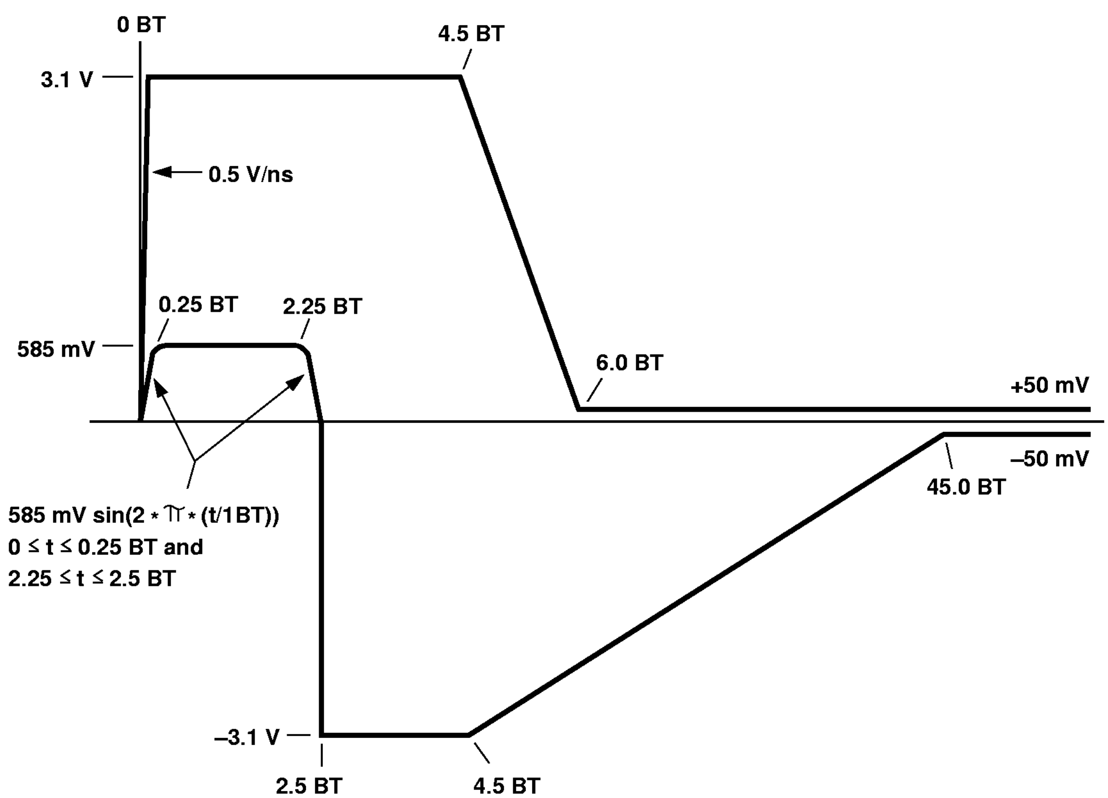


Figure 9. SOI Output Voltage Template - 10 Mbps

the 80C240, the supported device capabilities are 100Base-T4, 10Base-T Full Duplex, and 10Base-T Half Duplex operation. The capabilities read back from the remote device are stored in the MI serial port AutoNegotiation Remote End Capability register.

The AutoNegotiation algorithm is initiated by any of the following events: (1) powerup, (2) device reset, (3) AutoNegotiation reset, (4) device enters the Link Fail State, (5) AutoNegotiation enabled. Once the negotiation process is completed, the 80C240 configures itself for either 100Base-T4, 10Base-T Half Duplex, or 10Base-T Half Duplex operation, depending on the outcome of the AutoNegotiation process. When the AutoNegotiation process is completed, the 80C240 switches back to either the 100Base-T4 or 10Base-T link integrity algorithms, depending on what was negotiated. The outcome or result of the AutoNegotiation process is stored in the speed detect and duplex detect bits in the MI serial port Status Output register.

The AutoNegotiation algorithm embedded in the 80C240 is more complicated than stated above. Refer to IEEE 802.3 Section 28 for more details if needed.

3.11.5 AutoNegotiation Status

The status of the negotiation process can be monitored by reading the AutoNegotiation status bits in the MI serial port Status and Status Output registers. The MI serial port Status register contains a single AutoNegotiation acknowledgement bit which indicates when an AutoNegotiation sequence has been initiated and successfully completed. The MI serial port Status Output register contains two AutoNegotiation status bits which indicate one of four possible conditions: (1) AutoNegotiation Started - This means that an AutoNegotiation sequence has been initiated but has not been completed, (2) AutoNegotiation Stuck - This means that the AutoNegotiation process has been ongoing for over 1200-1500 mS and has not yet completed, (3) AutoNegotiation Done - This means that an AutoNegotiation sequence has been initiated and successfully completed, and (4) AutoNegotiation Not Detected - This means that AutoNegotiation ability was not detected from the remote device.

3.11.6 AutoNegotiation Enable

The AutoNegotiation algorithm can be enabled or disabled with the AutoNegotiation enable bit in the MI serial port Control register. When AutoNegotiation algorithm is dis-

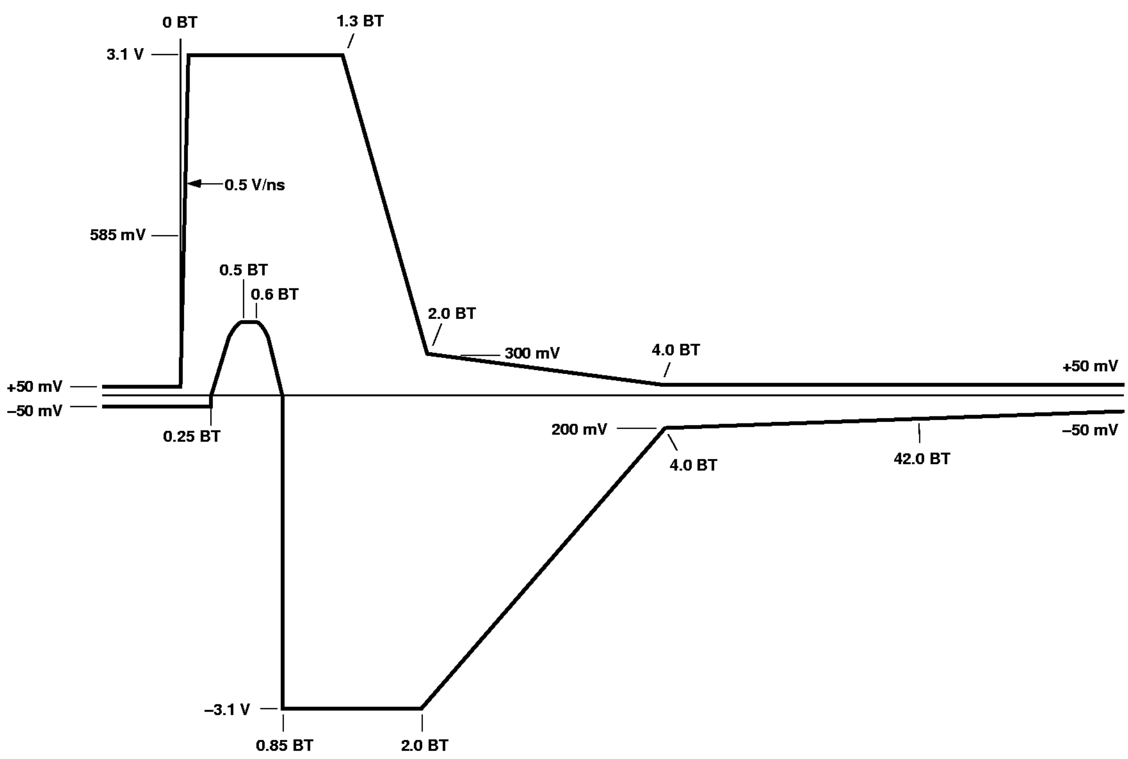


Figure 10. Link Pulse Output Voltage Template - NLP, FLP

abled, the selection of 100Base-T4 or 10Base-T modes is determined by the speed select bit in the MI serial port Control register, and the selection of 10Base-T Full or Half Duplex is determined by the duplex select bit in the MI serial port Control register. When the AutoNegotiation algorithm is enabled, the selection of 100Base-T4, 10Base-T Half duplex, or 10Base-T Full Duplex mode is determined by the outcome of the AutoNegotiation process which is automatically initiated when the bit is enabled.

3.11.7 AutoNegotiation Reset

The AutoNegotiation process can be initiated at any time by setting the AutoNegotiation reset bit in the MI serial Port Control Register.

3.11.8 Link Indication

Receive link pulse detect activity on RX_D2± can be monitored through the link detect bit in the MI serial port Status and Status Output registers or it can also be programmed to appear on the PLED3 pin by setting the programmable LED output select bits in the MI serial port Configuration 2 register. When the PLED3 pin is programmed to be a link pulse detect output, this pin is asserted low whenever the device is in the Link Pass State. The PLED3 output is open drain with resistor pullup and can drive an LED from V_{CC} or can drive another digital input.

The PLED3 and PLED0 LED output driver pins are default programmed to Link Detect and 100/10Base-T Detect, respectively. These two pins can be reconfigured to indicate Link Detect 100Base-T4 and Link Detect 10Base-T, respectively, by setting the LED default function select bit in the MI serial port Configuration 2 register.

Link pulses are only transmitted on one pair, TX_D1± and received on one pair, RX_D2±. Thus the IEEE specified link integrity algorithm only verifies that these two pairs are connected. The 80C240 verifies the link integrity of the other two pairs, BI_D3± and BI_D4±, by monitoring activity. If activity is present on RX_D2±, then activity is also expected on BI_D3± and BI_D4±. If no activity occurs on BI_D3± and BI_D4± when RX_D2± is active, then the inactive bits for these lines are set in the MI serial port Status Output register.

3.11.9 Link Disable

The link pulse function can be disabled by setting a MI serial port register bit in the Configuration 1 register. When the link pulse function is disabled, the device ignores the reception of link pulses, stays in the Link Pass state, configures itself for Half/Full Duplex based on the value of the duplex bit in the MI serial port Control register, configures itself for 100/10Base-T operation based on the values of the speed bit in the MI serial port Control register, and continues to transmit NLP's or T4LP's depending on whether the device is in 10Base-T or 100Base-T4 mode.

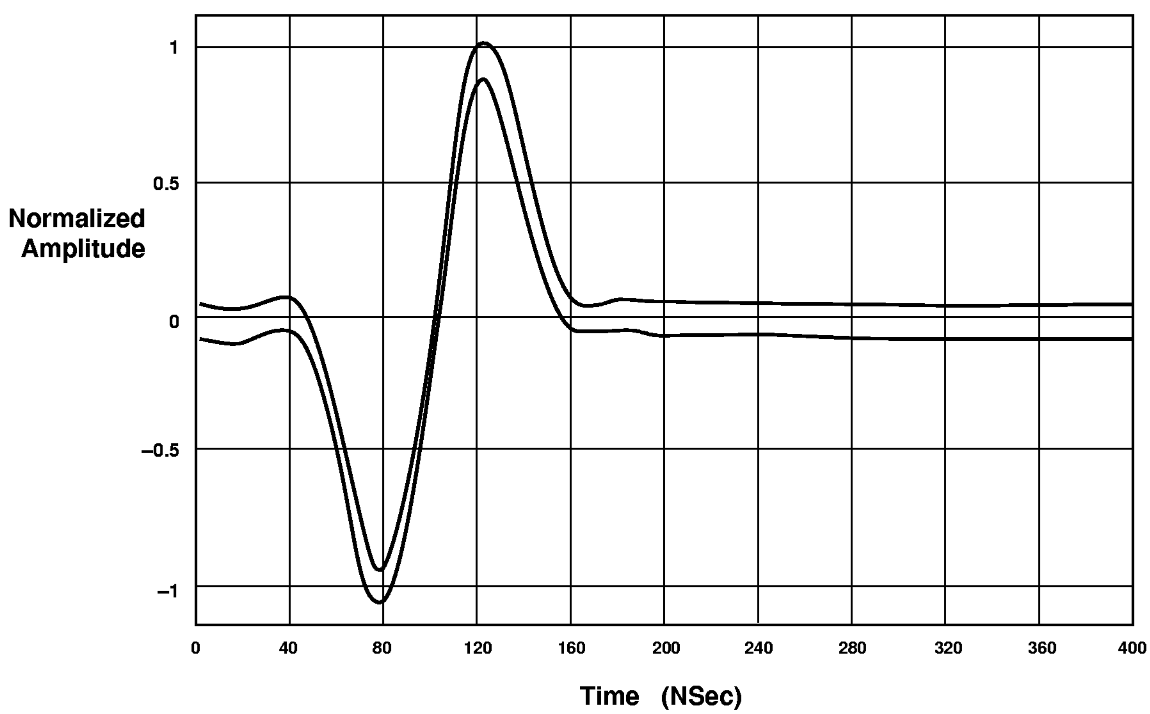


Figure 11. Link Pulse Output Voltage Template - T4LP

3.12 COLLISION

3.12.1 100 Mbps

Collision occurs whenever transmit and receive occur simultaneously.

There are two ways collision can be sensed by the 80C240.

The first way collision is sensed is when transmission is in progress (TX_EN is asserted) and then valid data is sensed on RX_D2. When this occurs, TP data continues to be transmitted on TX_D1, TP 0's are transmitted on BI_D3 and BI_D4, TP data is received on RX_D2, RXD[3:0] outputs all 0's, internal CRS loopback is disabled, and the collision signals are asserted.

The second way collision is sensed is when reception is in progress (CRS is asserted) and then TX_EN is asserted. When this occurs, TP data continues to be received on BI_D3 and BI_D4 and RX_D2, TP data is transmitted on TX_D1 only, internal CRS loopback is disabled, and the collision signals are asserted.

The collision function is disabled if the device is in the Link Fail state, or if the device is in internal or diagnostic loopback modes.

Collision can be monitored through the COL controller interface output signal.

The controller interface collision signal, COL, can be tested by setting the collision test register bit in the MI serial port Control register. When this bit is set, TX_EN is looped back onto COL and the TP transmitter is disabled.

3.12.2 10 Mbps

Collision in 10 Mbps mode is identical to the 100 Mbps mode except, (1) only one transmit and one receive pair are used to sense collision, (2) collision is asserted when the jabber condition has been detected, (3) collision is disabled in Full Duplex mode.

3.13 JABBER

3.13.1 100 Mbps

This function disabled in 100 Mbps mode.

3.13.2 10 Mbps

Jabber condition occurs when the transmit packet, or TX_EN, exceeds its maximum allowable length. When jabber is detected, the TP transmit outputs are forced to

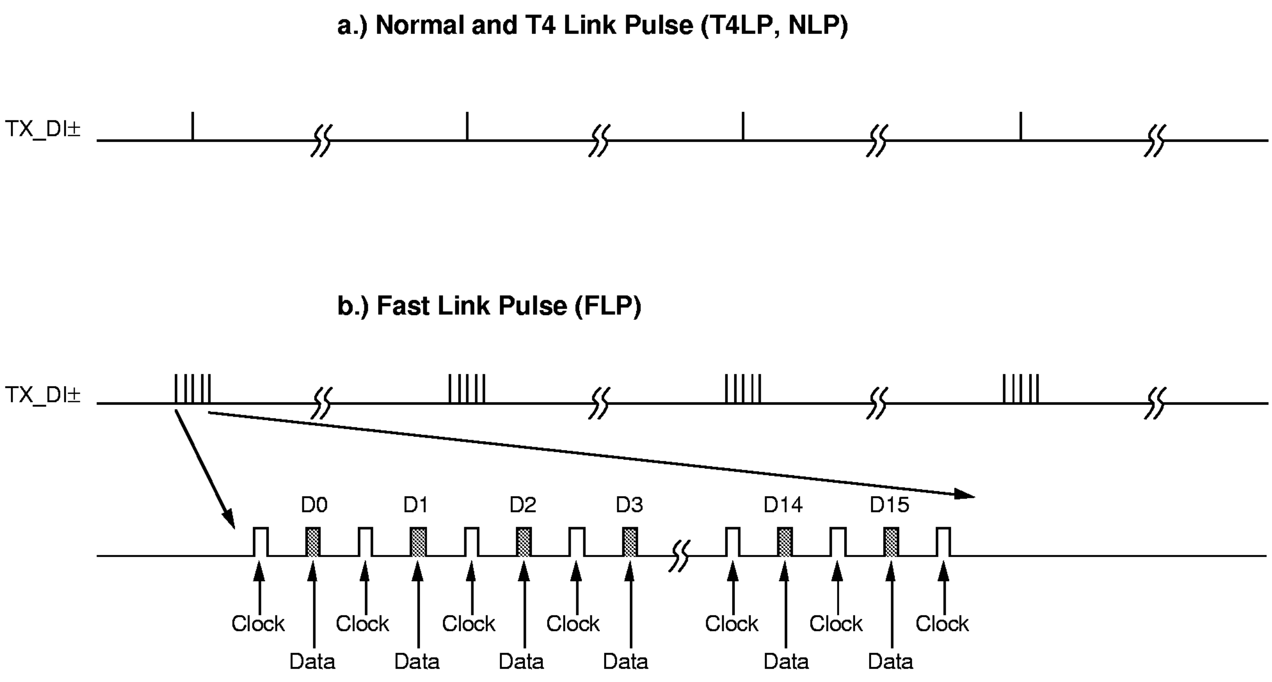


Figure 12 NLP vs. T4LP vs. NLP Link Pulse

the idle state, collision is asserted, and register bits in the MI serial port Status and Status Output registers are set. Jabber function can be disabled by setting a bit in the MI serial port Configuration 1 register.

3.14 RECEIVE POLARITY CORRECTION

3.14.1 100 Mbps

The polarity of the signals on the TP receive input is continuously monitored. If either 3 consecutive link pulses or 3 consecutive SSD patterns indicate incorrect polarity on any one of the three TP receive inputs, the polarity is internally determined to be incorrect, and a reverse polarity bit is set in the MI serial port Status Output register.

The 80C240 will automatically correct for the reverse polarity condition with the autopolarity feature. Autopolarity can be disabled by setting the polarity disable bit in the MI serial port Configuration 1 register.

3.14.2 10 Mbps

The reverse polarity detection for the 10 Mbps mode is the same as the 100 Mbps mode except, (1) the receiver is single channel, and (2) either 3 consecutive link pulses or 3 consecutive SOI pulses are used to determine reverse polarity.

3.15 PAIR SWAP

3.15.1 100 Mbps

The Link Integrity Algorithm guarantees that RX_D2 pair is connected to the 80C240. The 80C240 can detect if the BI_D3 and BI_D4 pairs are swapped by detecting the relative delay in the SSD symbols received on these two pairs. If these two pairs are determined to be swapped, the pair swap bit is set in the MI serial port Status Output register.

3.15.2 10 Mbps

This function is disabled in 10Mbps mode.

3.16 FULL DUPLEX MODE

3.16.1 100 Mbps

This function is disabled in 100 Mbps mode.

3.16.2 10 Mbps

Full Duplex mode allows transmission and reception to occur simultaneously. When Full Duplex mode is enabled, collision is disabled, and internal loopback is disabled.

The 80C240 can be either forced into the Half or Full Duplex mode, or the device also can detect either Half or Full Duplex capability from a remote device and automatically place itself in the correct mode.

The device can be forced into the Full or Half Duplex modes by setting the duplex bit in the MI serial port Control register.

The device can automatically configure itself for Full or Half Duplex modes by using the AutoNegotiation scheme to advertise and detect Full and Half Duplex capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity and AutoNegotiation section.

A Full Duplex Detect Status output bit is available in the MI serial port Status Output register. In addition, Full Duplex Detect can be programmed to appear on the $\overline{PLED1}$ pin by setting the LED output select bits in the MI Serial Port Configuration 2 Register. When the $\overline{PLED1}$ pin is programmed to be a full duplex detect output, this pin is asserted low when the device is configured for Full Duplex operation. The $\overline{PLED1}$ output is open drain with resistor pullup and can drive an LED from V_{CC} or can drive another digital input.

3.17 100/10 MBPS SELECTION

The device can be forced into either the 100 or 10 Mbps mode, or the device also can detect 100 or 10 Mbps capability from a remote device and automatically place itself in the correct mode.

The device can be forced into either the 100 or 10 Mbps mode by setting the speed select bit in the MI serial port Control register.

The device can automatically configure itself for 100 or 10 Mbps mode by using the AutoNegotiation scheme to advertise and detect 100 and 10 Mbps capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity and AutoNegotiation section.

A device speed (100/10 Mbps) status output bit is available through the speed bit in the MI serial port Status Output register, or it can also be programmed to appear on the $\overline{PLED0}$ pin by setting the programmable LED output select bits in the MI serial port Configuration 2 register. When the $\overline{PLED0}$ pin is programmed to be speed detect output, this pin is asserted low when the device is configured for 100 Mbps operation. The $\overline{PLED0}$ output is open drain with resistor pullup and can drive an LED from V_{CC} or can drive another digital input.

3.18 LOOPBACK

3.18.1 100 Mbps

TX_EN is internally looped back onto CRS during every transmit packet. This CRS loopback is disabled during collision, in Link Fail State, when the transmit disable bit is set in the MI serial port Configuration 1 register, and when the CRS assert delay bit is set high (Repeater Mode) in the MI Serial Port Select Register.

A diagnostic loopback mode is also available and can be selected by setting the loopback bit in the MI serial port Control register. When loopback is enabled, TXD[3:0] data is looped back onto RXD[3:0], TX_EN is looped back onto CRS, RX_DV operates normally, the TP receive and transmit paths are disabled, the transmit link pulses are halted, and the Half/Full Duplex modes do not change.

3.18.2 10 Mbps

In order to emulate coax Ethernet behavior, transmitted data on TX_D1+ is routinely internally looped back onto the receive section and sent out on the receive controller pins RXD[3:0], CRS, RX_DV, and RXC as if it was a regular received packet. The loopback function is disabled if the device is in the Link Fail State, jabber condition, or in Full Duplex mode.

A diagnostic loopback mode is also available and can be selected by setting the loopback bit in the MI serial port Control register. This loopback mode is identical in function to the one described in the previous 100 Mbps Loopback section.

If the device is in the BII Interface mode, the MDINT/LPBK JAM pin becomes a diagnostic loopback input select pin LPBK. In BII interface mode, the interrupt function (MDINT) is disabled and the Jam function (JAM) is unavailable.

3.19 JAM

3.19.1 100 Mbps

The 80C240 has an automatic JAM feature which will cause the device to automatically transmit a JAM packet if receive activity is detected. This automatic JAM feature is enabled when the MDINT/LPBK/JAM pin is programmed to be a JAM input by setting the Pin 11 configuration bit in the MI serial port Configuration register. When pin JAM = 0 and receive activity is detected on RX_D2± (and Pin 11 is programmed to be a JAM input), the following JAM packet is transmitted on TX_D1±: SOSA, SOSA, SOSB, BAD_CODE, BAD_CODE, BAD_CODE. Transmission occurs on twisted pair TX_D1± only; pairs BI_D3± and BI_D4± are silent. When the Jam feature is enabled, the interrupt function (MDINT) is disabled and the loopback function (LPBK) is unavailable with this pin.

3.19.2 10 Mbps

This function is disabled in 10 Mbps mode.

3.20 RESET

The 80C240 can be reset by setting the reset bit in the MI serial port Control register. When this bit is set, an internal poweron reset pulse is generated which resets all internal circuits, forces the MI serial port bits to their default values, and latches in the MI address values. After the poweron reset pulse has finished, the reset bit in the MI serial port Control register is cleared and the device is ready for normal operation. The device is ready for normal operation 500 mS after the reset was initiated.

3.21 POWERDOWN

The 80C240 can be powered down by setting the powerdown bit in the MI serial port Control register. In powerdown mode, the TP outputs are in high impedance state, all functions are disabled except the MI serial port, and the power consumption is reduced to less than 0.5 mW. The device is reset when the device powers up from either the powerdown state or with initial application of V_{CC}. The device is ready for normal operation 500 mS after powerdown was deasserted or application of V_{CC}.

3.22 OSCILLATOR

The 80C240 requires a 25 Mhz reference frequency for internal signal generation. This 25 Mhz reference frequency is generated by either connecting an external 25 Mhz crystal between OSCIN and GND or an external 25 Mhz clock to OSCIN.

3.23 LED DRIVERS

The PLED[3:0] outputs are open drain with a resistor pullup. These outputs can drive LED's tied to V_{CC}.

The PLED[3:0] outputs can be programmed through the MI serial port to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink.

PLED[3:0] can be individually programmed by appropriately setting the LED output select bits in the MI serial port Configuration 2 register. When a PLED[3:0] is programmed for its Normal function, that output indicates the specific functions described in the MI serial port Configuration 2 register shown on Table 11 (Link Detect, Activity, Full Duplex Detect, 100Mbps Detect). When a PLED[3:0] is programmed to be On, that LED output driver will go low, thus turning on the LED under user control. When a PLED[3:0] is programmed to be Off, that LED output driver will turn off, thus turning off the LED under user control. When a PLED[3:0] is programmed to Blink, that LED output driver will continuously blink at a rate of 100 mS on, 100 mS off.

The Normal functions for PLED[3:0] can be changed from Link Detect, Activity, Full Duplex Detect, and 100 Mbps Detect to Link Detect 100 Mbps, Activity, Full Duplex and Link Detect 10 Mbps respectively by appropriately setting the LED default select bit in the MI serial port Configuration 2 register.

3.24 MI SERIAL PORT

3.24.1 Signal Description

The MI serial port has eight pins, MDC, MDIO, $\overline{MDINT}$, and MDA[4:0]. MDC is the serial shift clock input. MDIO is a bidirectional data I/O pin. $\overline{MDINT}$ is an interrupt output. MDA[4:0] are address pins for the MI serial port.

$\overline{MDA[4:0]}$ inputs share to the same pins as the TX_CLK50 and PLED[3:0] outputs, respectively. At powerup or reset, the output drivers are tristated for an interval called the poweron reset time. During the poweron reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port address.

3.24.2 Timing

The MI serial port is idle when at least 32 continuous 1's are detected on MDIO and remains idle as long as continuous 1's are detected. During idle, MDIO is in the high impedance state. When the MI serial port is in the idle state, a 01 pattern on the MDIO pin initiates a serial shift cycle. Data on MDIO is then shifted in on the next 14 rising edges of MDC (MDIO is high impedance). If the register address was not set to 11111, on the next 16 rising edges of MDC, data is either shifted in or out on MDIO, depending on whether a write or read cycle was selected with the bits READ and WRITE. After the 32 MDC cycles have been completed, one complete register has been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the the idle condition (at least 32 continuous 1's) is detected.

$\overline{MDINT}$ is an output pin that goes low whenever any one of the interrupt bits changes state in the MI serial port registers. After the MI serial port bit that set the interrupt is read out, the interrupt is cleared and $\overline{MDINT}$ is reset back to a high. Refer to the interrupt section for more details.

3.24.3 Multiple Register Access

Multiple registers can be accessed on a single MI serial port access cycle with the multiple register access feature. The multiple register access feature can be enabled by setting the multiple register access bit in the MI Serial Port

Table 2. MI Register Bit Type Definition

Symbol	Name	Definition	
		Write Cycle	**Read Cycle**
W	Write	Input	No Operation, Hi Z
R	Read	No Operation, Hi Z	Output
R/W	Read/Write	Input	Ouput
R/W SC	Read/Write, Self Clearing	Input, Clears Itself After Operation Completed	Output
R/LH	Read, Latching High	No Operation, Hi Z	Output When Bit Goes High, Bit Latched When Bit Is Read, Bit Reset Low.
R/LL	Read, Latching Low	No Operation, Hi Z	Output When Bit Goes Low, Bit Latched. When Bit Is Read, Bit Reset High.
R/LT	Read, Latching On Transition	No Operation, Hi Z	Output When Bit Transitions, Bit Latched And Interrupt Set. When Bit Is Read, Interrupt Cleared And Bit Updated.

Configuration 2 register. When multiple register access is enabled, multiple registers can be accessed by setting the register address to 11111 during the first 16 MDC clock cycles. There is no actual register residing in register address location 11111, so when the register address set to 11111, all eleven registers are accessed on the 176 rising edges of MDC that occur after the first 16 MDC clock cycles of the MI serial port access cycle. The registers are accessed in numerical order from 0 to 20. After all 192 MDC clocks have been completed, all the registers have been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

3.24.4 Frame Structure

The structure of the serial port frame is shown in Table 3. Each serial port access cycle consists of 32 bits (or 192 bits if REGAD=11111 and multiple register access is enabled), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16/192 bits are from one/all of the eleven internal registers.

The first 2 bits in the MI serial port frame are start bits and need to be written as a 01 for the serial port cycle to continue. The next two bit are a read and write bit which determine if the accessed data register bits will be read or write. The next 5 bits are device addresses and PHY_AD[4:0] must match the inverted values latched in from pins $\overline{\text{MDA[4:0]}}$ during the poweron reset time for the serial port access to continue. The next 5 bits are register address select bits which select one of the eleven data registers for access. The next 2 bits are turnaround bits which are not actual register bits but extra time to switch MDIO from write to read if necessary. The final 16 bits of the MI serial port cycle (or 192 bits if REGAD = 11111 and multiple register access is enabled), come from the data register designated in the register address bits REGAD[4:0].

3.24.5 Bit Types

Since the serial port is bidirectional, there are many different types of bits. Write bits (W) are inputs during a write cycle and are high impedance during a read cycle. Read bits (R) are outputs during a read cycle and high impedance during a write cycle. Read/Write bits (R/W) are actually write bits which can be read out during a read cycle. R/WSC bits are R/W bits that clear themselves after a set period of time or after a specific even has completed. R/LH bits are read bits that latch themselves when they go high, and they stay latched high until read. After they are read, they are reset low. R/LL bits are read bits that latch themselves when they go low, and they stay latched low until read. After they are read, they are reset high. R/LT are read bits that latch themselves whenever they make a transition or change value, and they stay latched until they are read. After they are read, they are updated to their current value. R/LT bits can also be programmed to assert the interrupt function a described in the Interrupt section. The bit type definitions are summarized in Table 2.

3.24.6 Interrupt

The 80C240 has hardware and software interrupt capability. The interrupts are triggered by certain output status bits (interrupt bits) in the serial port. As indicated previously, R/LT bits are read bits that latch on transition. R/LT bits are also called interrupt bits if they are not masked out with the Mask register bits. Interrupt bits automatically latch themselves into their register locations and assert the interrupt indication when they change state. Interrupt bits stay latched until they are read. When interrupt bits are read, the interrupt indication is deasserted and the interrupt bits that caused the interrupt to happen are updated to their current value. Each interrupt bit can be individually masked and subsequently be removed as an interrupt bit by setting the appropriate mask register bits in the Mask register.

Interrupt indication is done in three ways: (1) $\overline{\text{MDINT/LPBK/JAM}}$ pin, (2) INT bit in the MI serial port Status Output register, and (3) interrupt pulse on MDIO. The $\overline{\text{MDINT/LPBK/JAM}}$ is an active low interrupt output indication that is available on pin 11 provided that pin 11 is not programmed to be a loopback or jam input. The INT bit in the Status Output register is an active high interrupt indicator and is always available. An interrupt pulse on MDIO also indicates interrupt and is available when the MDIO interrupt pulse select bit is set in the MI serial port Configuration 2 register. When this bit is set, an interrupt is signaled by a low going pulse on MDIO when MDC is high and the serial port is in the idle state as shown in Figure13. Once MDIO goes low with an interrupt pulse, MDIO stays low until MDC returns low. Once MDC returns low, then MDIO goes back to high impedance state. If the interrupt occurs while the serial port is being accessed, then the MDIO pulse is delayed until one clock bit after the serial port access cycle is ended as shown in Figure 13.

3.24.7 Register Structure

The 80C240 has eleven internal 16 bit registers. One register is reserved for factory use, and the other ten registers are available for setting configuration inputs and reading status outputs. A map of the registers is shown in Table 4. The ten accessible registers consist of six registers that are defined by IEEE 802.3 specification (Registers 0-5) and four registers that are unique to the 80C240 (Registers 16-20).

The structure and bit definition of the Control register is shown in Table 5. This register stores various configuration inputs and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Status register is shown in Table 6. This register contains device capabilities and output status information and its bit definition complies with the IEEE 802.3 specification.

The structure and bit definition of the PHY ID #1 and PHY ID #2 registers are shown in Tables 7 and 8, respectively. These registers contain an identification code unique to the 80C240 and their bit definition complies with the IEEE 802.3 specification.

The structure and bit definition of the AutoNegotiation Advertisement and AutoNegotiation Remote End Capability registers are shown in Tables 9 and 10, respectively. These registers are used by the AutoNegotiation algorithm and their bit definition complies with the IEEE 802.3 specification.

The structure and bit definition of Configuration 1 and 2 registers is shown in Table 11 and 12. These registers store various configuration inputs.

The structure and bit definition of the Status Output register is shown in Table 13. This register contains output status information.

The structure and bit definition of the Mask register is shown in Table 14. this register allows each R/LT bit in the Status Output register to be masked out or removed as a bit that will set interrupt.

Register 20 is reserved for factory use. All bit values must be set to defaults for normal operation.

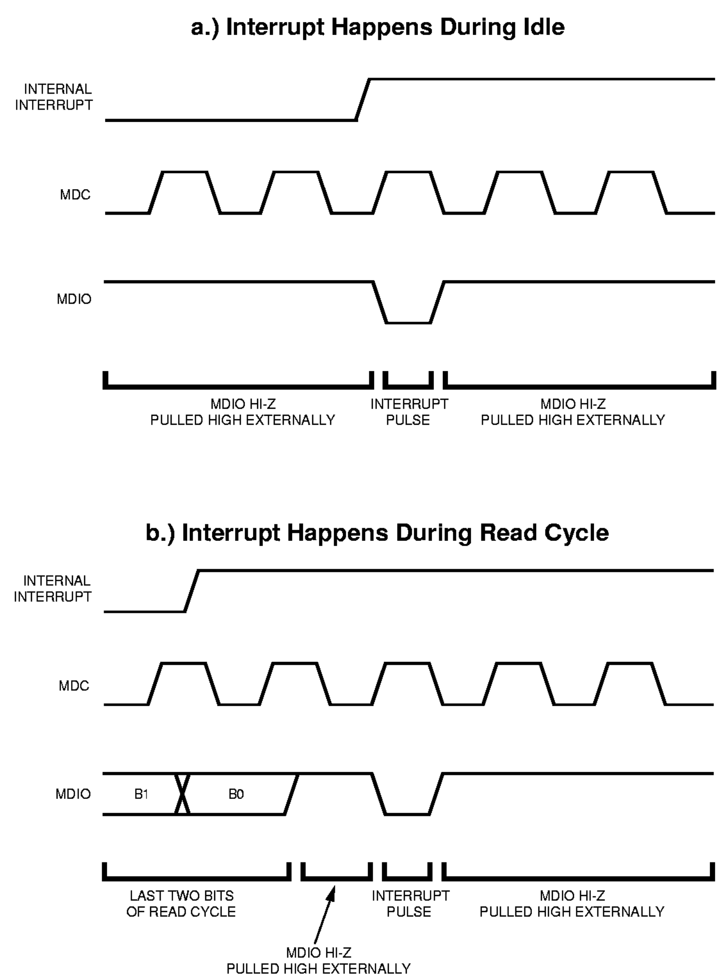


Figure 13. MDIO Interrupt Pulse

4.0 Register Description

Table 3. MI Serial Port Frame Structure

<Idle>	<Start>	<Read>	<Write>	<PHY Addr.>	<Reg. Addr.>	<Turnaround>	<Data> ....
IDLE	ST[1:0]	READ	WRITE	PHYAD[4:0]	REGAD[4:0]	TA[1:0]	D[15:0] ....

Register 0	Control
Register 1	Status
Register 2	PHY ID #1
Register 3	PHY ID #2
Register 4	AutoNegotiation Advertisement
Register 5	AutoNegotiation Remote End Capability
Register 16	Configuration 1
Register 17	Configuration 2
Register 18	Status Output
Register 19	Mask
Register 20	Reserved

Symbol	Name	Definition	R/W
IDLE	Idle Pattern	These Bits Are an Idle Pattern. Device Will Not Initiate An MI Cycle until it Detects at Least 32 1's.	W
ST1 ST0	Start Bits	When ST[1:0] = 01, A MI Serial Port Access Cycle Starts.	W
READ	Read Select	1 = Read Cycle	W
WRITE	Write Select	1 = Write Cycle	W
PHYAD[4:0]	Physical Device Address	When PHYAD[4:0] = $\overline{\text{MDA[4:0]}}$ Pins Inverted, The MI Serial Port Is Selected For Operation.	W
REGAD[4:0]	Register Address	If REGAD = 00000 - 11110, These Bits Determine The Register From Which D[15:0] Is Read/Written. If REGAD = 11111 and multiple register access is enabled, All Registers Are Read/Written.	W
TA1 TA0	Turnaround Time	These Bits Provide Some Turnaround Time For MDIO When READ = 1, TA[1:0] = Z0 When WRITE = 1, TA[1:0] = ZZ	R/W
D[15:0]	Data	These 16 Bits Contain Data To/From One Of The Eleven Registers Selected By Register Address Bits REGAD[4:0].	Any

IDLE is shifted in first

Table 4. MI Serial Port Register Map

Register	x.15	x.14	x.13	x.12	x.11	x.10	x.9	x.8	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
0 Control	RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX	COLTST	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0
	R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	1	1	0	1/0	0	0	0	0	0	0	0	0	0	0
1 Status	CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
	R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R/LL	R/LH	R
	1	0	0	1	1	0	0	0	0	0	0	0	1	1	0	1
2 PHY ID #1	OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10	OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
3 PHY ID #2	OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
4 AutoNegot. Advertisement	NP	ACK	RF	RESERVED = 0	RESERVED = 0	RESERVED = 0	T4	TX_FDX	TX_HDX	10_FDX	10_HDX	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	CSMA
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1
5 AutoNeg. Remote End Capability	NP	ACK	RF	RESERVED = 0	RESERVED = 0	RESERVED = 0	T4	TX_FDX	TX_HDX	10_FDX	10_HDX	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	CSMA
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16 Configuration 1	LNK_DIS	APOL_DIS	XMT_DIS	RESERVED = 1	CIS	EQLZR	RLVL0	RESERVED = 1	RESERVED = 0	RESERVED = 0	RESERVED = 0	VREF_EXT	RESERVED = 1	P34_CFG	P11_CFG	CRS_AST
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0
17 Configuration 2	PLED3_1	PLED3_0	PLED2_1	PLED2_0	PLED1_1	PLED1_0	PLED0_1	PLED0_0	LED_DEF	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	MREG	INT_MDIO
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						R/W	R/W
	1	1	1	1	1	1	1	1	0						0	0
18 Status Output	INT	LNK_FAIL	INACT_D3	INACT_D4	RPOL	PSWAP	EOP	CWRD	DCBAL	PRMBL	ASKEW	SPD_DET	DPLX_DET	ANEG_ST1	ANEG_ST0	JAB
	R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19 Mask	RESERVED = 0	MASK_ LNK_FAIL	MASK_ INACT_D3	MASK_ INACT_D4	MASK_ RPOL	MASK_ PSWAP	MASK_ EOP	MASK_ CWRD	MASK_ DCBAL	MASK_ PRMBL	MASK_ ASKEW	MASK_ SPD_DET	MASK_ DPLX_DET	MASK_ ANEG_ST1	MASK_ ANEG_ST0	MASK_ JAB
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20 Reserved	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0	RESERVED = 0
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
		0	0	0	0	0	0	0	0	0	0	0	0	0		

Note: All Reserved Bit Values Must Be Programmed As Specified.

Table 5. Register 0 (Control) Structure And Bit Definition

0.15	0.14	0.13	0.12	0.11	0.10	0.9	0.8
RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX
R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W

0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
COLTST	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
0.15	RST	Reset	1 = Reset 0 = Normal	R/W SC	0
0.14	LPBK	Loopback Enable	1 = Loopback Mode Enabled 0 = Normal	R/W	0
0.13	SPEED	Speed Select	1 = 100 Mbps Selected (100BaseT4) 0 = 10 Mbps Selected (10BaseT)	R/W	1
0.12	ANEG_EN	AutoNegotiation Enable	1 = AutoNegotiation Enabled 0 = Normal	R/W	1
0.11	PDN	Powerdown Enable	1 = Powerdown 0 = Normal	R/W	0
0.10	MII_DIS	MII Interface Disable	1 = MII Interface Disabled 0 = Normal	R/W	1[1]
0.9	ANEG_RST	AutoNegotiation Reset	1 = Restart AutoNegotiation Process 0 = Normal	R/W SC	0
0.8	DPLX	Duplex Mode Select	1 = Full Duplex 0 = Half Duplex	R/W	0
0.7	COLTST	Collision Test Enable	1 = Collision Test Enabled 0 = Normal	R/W	0
0.6 thru 0.0			Reserved, must be 0	R/W	0

x.15 Bit Is Shifted First

Note: 1. If $\overline{\text{MDA}}$[4:0] ≠ 11111, then the MII_DIS default value is changed to 0.

Table 6. Register 1 (Status) Structure And Bit Definition

1.15	1.14	1.13	1.12	1.11	1.10	1.9	1.8
CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	0	0	0
R	R	R	R	R	R	R	R

1.7	1.6	1.5	1.4	1.3	1.2	1.1	1.0
0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
R	R	R	R/LH	R	R/LL	R/LH	R

Bit	Symbol	Name	Definition	R/W	Def.
1.15	CAP_T4	100BaseT4 Capable	1 = Capable of 100BaseT4 Operation	R	1
1.14	CAP_TXF	100BaseTX Full Duplex Capable	0 = Not Capable Of 100BaseTX Full Duplex	R	0
1.13	CAP_TXH	100BaseTX Half Duplex Capable	0 = Not Capable Of 100BaseTX Half Duplex	R	0
1.12	CAP_TF	10BaseT Full Duplex Capable	1 = Capable Of 10BaseT Full Duplex	R	1
1.11	CAP_TH	10BaseT Half Duplex Capable	1 = Capable Of 10BaseT Half Duplex	R	1
1.10 thru 1.7			Reserved	R	0
1.6	CAP_SUPR	MI Preamble Suppression Capable	0 = Not Capable of Accepting Frames with MI Preamble Suppression	R	0
1.5	ANEG_ACK	AutoNegotiation Acknowledgement	1 = AutoNegotiation Acknowledgement Process Complete 0 = Normal	R	0
1.4	REM_FLT	Remote Fault Detect	1 = Remote Fault Detected. This bit is set when Either Interrupt Detect Bit 18.15 or AutoNegotiation Remote Fault Bit 5.13 is set. 0 = No Remote Fault	R/LH	0
1.3	CAP_ANEG	AutoNegotiation Capable	1 = Capable of AutoNegotiation Operation	R	1
1.2	LINK	Link Status	1 = Link Pulse Detected (Same As Bit 18.14) 0 = Link Pulse Not Detected	R/LL	1
1.1	JAB	Jabber Detect	1 = Jabber Detected (Same As Bit 18.0) 0 = Normal	R/LH	0
1.0	EXREG	Extended Register Capable	1 = Extended Registers Exist	R	1

x.15 Bit Is Shifted First

Table 7. MI Register 2 (PHY ID #1) Structure And Bit Definition

2.15	2.14	2.13	2.12	2.11	2.10	2.9	2.8
OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10
R	R	R	R	R	R	R	R

2.7	2.6	2.5	2.4	2.3	2.2	2.1	2.0
OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
2.15	OUI3	Company ID,	SEEQ OUI = 00 – A0 – 7D	R	0
2.14	OUI4	Bits 3-18			0
2.13	OUI5				0
2.12	OUI6				0
2.11	OUI7				0
2.10	OUI8				0
2.9	OUI9				0
2.8	OUI10				0
2.7	OUI11				0
2.6	OUI12				0
2.5	OUI13				0
2.4	OUI14				1
2.3	OUI15				0
2.2	OUI16				1
2.1	OUI17				1
2.0	OUI18				0

x.15 Bit Is Shifted First

Table 8. Register 3 (PHY ID #2) Structure And Bit Definition

3.15	3.14	3.13	3.12	3.11	3.10	3.9	3.8
OUI19	OUI20	OU21	OU22	OU23	OU24	PART5	PART4
R	R	R	R	R	R	R	R

3.7	3.6	3.5	3.4	3.3	3.2	3.1	3.0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
3.15 3.14 3.13 3.12 3.11 3.10	OUI19 OUI20 OUI21 OUI22 OUI23 OUI24	Company ID, Bits 19-24	SEEQ OUI = 00 – A0 – 7D	R	1 1 1 1 1 0
3.9 3.8 3.7 3.6 3.5 3.4	PART5 PART4 PART3 PART2 PART1 PART0	Manufacturer's Part Number	00_{16}	R	0 0 0 0 0 0
3.3 3.2 3.1 3.0	REV3 REV2 REV1 REV0	Manufacturer's Revision Number	0_{16}	R	0 0 0 0

x.15 Bit Is Shifted First

Table 9. Register 4 (AutoNegotiation Advertisement) Structure

4.15	4.14	4.13	4.12	4.11	4.10	4.9	4.8
NP	ACK	RF	0	0	0	T4	TX_FDX
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

4.7	4.6	4.5	4.4	4.3	4.2	4.1	4.0
TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
4.15	NP	Next Page Enable	1 = Next Page Exists 0 = No Next Page	R/W	0
4.14	ACK	Acknowledge	1 = Received Word Recognized 0 = Not Recognized	R	0
4.13	RF	Remote Fault Enable	1 = Remote Fault Detected 0 = No Remote Fault	R/W	0
4.12 4.11 4.10			Reserved, must be 0	R/W	0 0 0
4.9	T4	100BaseT4 Capable	1 = Capable Of 100BaseT4 0 = Not Capable	R/W	1
4.8	TX_FDX	100BaseTX Full Duplex Capable	1 = Capable of 100BaseTX Full Duplex 0 = Not Capable	R/W	0
4.7	TX_HDX	100BaseTX Half Duplex Capable	1 = Capable Of 100BaseTX Half Duplex 0 = Not Capable	R/W	0
4.6	10_FDX	10BaseT Full Duplex Capable	1 = Capable Of 10BaseT Full Duplex 0 = Not Capable	R/W	1
4.5	10_HDX	10BaseT Half Duplex Capable	1 = Capable Of 10BaseT Half Duplex 0 = Not Capable	R/W	1
4.4 thru 4.1			Reserved, must be 0	R/W	0
4.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R/W	1

x.15 Bit Is Shifted First

Table 10. Register 5 (AutoNegotiation Remote End Capability) Structure And Bit Definition

5.15	5.14	5.13	5.12	5.11	5.10	5.9	5.8
NP	ACK	RF	0	0	0	T4	TX_FDX
R	R	R	R	R	R	R	R

5.7	5.6	5.5	5.4	5.3	5.2	5.1	5.0
TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
5.15	NP	Next Page Enable	1 = Next Page Exists 0 = No Next Page	R	0
5.14	ACK	Acknowledge	1 = Received Word Recognized 0 = Not Recognized	R	0
5.13	RF	Remote Fault Enable	1 = Remote Fault Detected 0 = No Remote Fault	R	0
5.12 5.11 5.10			Reserved	R	0 0 0
5.9	T4	100BaseT4 Capable	1 = Capable Of 100BaseT4 0 = Not Capable	R	0
5.8	TX_FDX	100BaseTX Full Duplex Capable	1 = Capable of 100BaseTX Full Duplex 0 = Not Capable	R	0
5.7	TX_HDX	100BaseTX Half Duplex Capable	1 = Capable Of 100BaseTX Half Duplex 0 = Not Capable	R	0
5.6	10_FDX	10BaseT Full Duplex Capable	1 = Capable Of 10BaseT Full Duplex 0 = Not Capable	R	0
5.5	10_HDX	10BaseT Half Duplex Capable	1 = Capable Of 10BaseT Half Duplex 0 = Not Capable	R	0
5.4 thru 5.1			Reserved	R	0
5.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R	0

x.15 Bit Is Shifted First

Table 11. Register 16 (Configuration 1) Structure and Bit Definition

16.15	16.14	16.13	16.12	16.11	16.10	16.9	16.8
LNK_DIS	APOL_DIS	XMT_DIS	XMT_PDN	CIS	EQLZR	RLVL0	TLVL3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.7	16.6	16.5	16.4	16.3	16.2	16.1	16.0
TLVL2	TLVL1	TLVL0	VREF_EXT	1	P34_CFG	P11_CFG	CRS_AST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
16.15	LNK_DIS	Link Disable	1 = Receive Link Pulse Detect Function Disabled 0 = Normal	R/W	0
16.14	APOL_DIS	Auto Polarity Disable	1 = Auto Polarity Correction Function Disabled 0 = Normal	R/W	0
16.13	XMT_DIS	TP Transmit Disable	1 = TP Transmitter Disabled 0 = Normal	R/W	0
16.12			1 = Reserved Must be Written to 1		See Defin.
16.11	CIS	Controller Interface Select	1 = BII Interface Selected 0 = MII Interface Selected	R/W	0
16.10	EQLZR	Receive Equalizer Select	If 100Mb Mode Selected: 1 = Receive Equalizer Disabled, Set To 0 Length 0 = Receive Equalizer On If 10Mb Mode Selected: 1 = Receive Equalizer On 0 = Receive Equalizer Disabled, Set To 0 Length	R/W	0
16.9	RLVL0	Receive Input Level Adjust	1 = Receive Squelch Levels Reduced By 4.5 dB 0 = Normal	R/W	0
16.8			1 = Reserved	R/W	1
16.7 16.6 16.5			0 = Reserved	R/W	0 0 0
16.4	VREF_EXT	External VREF Enable	1 = 2.5v VREF Required On $\overline{\text{MDINT}}$ Pin 0 = Normal	R/W	0
16.3			Reserved for factory use, must be 1	R/W	1
16.2	P34_CFG	Pin 34 Configuration Select	1 = Pin 34 is TX_CLK50 0 = Pin 34 is $\overline{\text{RX\_EN}}$	R/W	1
16.1	P11_CFG	Pin 11 Configuration Select	1 = Pin 11 is $\overline{\text{JAM}}$ 0 = Pin 11 is $\overline{\text{MDINT}}$/LPBK	R/W	0
16.0	CRS_AST	CRS Assert Time Select	1 = t_{31} is 0 – 155 ns, TX_EN to CRS Loopback Disabled (Repeater) 0 = t_{31} is 215 – 275 ns (DTE)	R/W	0

x.15 Bit Is Shifted First

Table 12. Register 17 (Configuration 2) Structure And Bit Definition

17.15	17.14	17.13	17.12	17.11	17.10	17.9	17.8
PLED3_1	PLED3_0	PLED2_1	PLED2_0	PLED1_1	PLED1_0	PLED0_1	PLED0_0
R/W	R/W	R/W or R/WSC	R/W or R/WSC	R/W	R/W	R/W	R/W

17.7	17.6	17.5	17.4	17.3	17.2	17.1	17.0
LED_DEF	0	0	0	0	0	MREG	INT_MDIO
R/W						R/W	R/W

Bit	Symbol	Name	Definition		R/W	Def.
17.15 17.14	PLED3_1 PLED3_0	Programmable LED Output Select, Pin PLED3	11 = Link 10 = LED Blink 01 = LED On 00 = LED Off	(PLED3 Is Low When Link Pulse Detected) (PLED3 Is Toggling 100 mS Low, 100 mS High) (PLED3 Is Low) (PLED3 Is High)	R/W	11
17.13 17.12	PLED2_1 PLED2_0	Programmable LED Output Select, Pin PLED2	11 = Activity 10 = LED Blink 01 = LED On 00 = LED Off	(PLED2 Is Low For 100 mS When Activity Occurs,Then Pin Returns High and Bit Clears Itself) (PLED2 Is Toggling 100 mS Low, 100 mS High) (PLED2 Is Low) (PLED2 Is High)	R/W or R/W SC	11
17.11 17.10	PLED1_1 PLED1_0	Programmable LED Output Select, Pin PLED1	11 = Full Duplex 10 = LED Blink 01 = LED On 00 = LED Off	(PLED1 Is Low When Device In Full Duplex Mode) (PLED1 Is Toggling 100 mS Low, 100 mS High) (PLED1 Is Low) (PLED1 Is High)	R/W	11
17.9 17.8	PLED0_1 PLED0_0	Programmable LED Output Select, Pin PLED0	11 = 100Mb Detect 10 = LED Blink 01 = LED On 00 = LED Off	(PLED0 Is Low When Device In 100 Mbps Mode) (PLED0 Is Toggling 100 mS Low, 100 mS High) (PLED0 Is Low) (PLED0 Is High)	R/W	11
17.7	LED_DEF	LED Default Function Select	1 = PLED[3:0] is Link 100, Activity, Full Duplex, and Link 10 Detect 0 = PLED[3:0] is Link, Activity, Full Duplex, and 100 Mbps Detect		R/W	0
17.6 thru 17.2			Reserved for factory use, must be 0			0
17.1	MREG	Multiple Register Access Enable	1 = Multiple Register Access Feature Enabled 0 = No Multiple Register Access		R/W	0
17.0	INT_ MDIO	MDIO Interrupt Pulse Select	1 = Interrupt Signaled with MDIO Pulse 0 = Interrupt not Signaled with MDIO Pulse		R/W	0

x.15 Bit Is Shifted First

Table 13. Register 18 (Status Output) Structure And Bit Definition

18.15	18.14	18.13	18.12	18.11	18.10	18.9	18.8
INT	LNK_FAIL	INACT_D3	INACT_D4	RPOL	PSWAP	EOP	CWRD
R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT

18.7	18.6	18.5	18.4	18.3	18.2	18.1	18.0
DCBAL	PRMBL	ASKEW	SPD_DET	DPLX_DET	ANEG_ST1	ANEG_ST0	JAB
R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT

Bit	Symbol	Name	Definition	R/W	Def.
18.15	INT	Interrupt Detect	0 = Interrupt Bit(s) Have Changed Since Last Read Operation. 0 = No Change	R	0
18.14	LNK_FAIL	Link Fail Detect	1 = Link Pulse Not Detected On RX_D2 0 = Normal	R/LT	0
18.13	INACT_D3	D3 Inactive	1 = BI_D3 Inactive When RX_D2 Active 0 = Normal	R/LT	0
18.12	INACT_D4	D4 Inactive	1 = BI_D4 Inactive When RX_D2 Active 0 = Normal	R/LT	0
18.11	RPOL	Reverse Polarity Detect	1 = Reverse Polarity Detected 0 = Normal	R/LT	0
18.10	PSWAP	Pair Swap Error	1 = Pair Swap Error Detected On BI_D3, BI_D4 0 = Normal	R/LT	0
18.9	EOP	EOP Error	1 = EOP Error Detected On Receive Data 0 = Normal	R/LT	0
18.8	CWRD	Codeword Error	1 = Codeword Error Detected On Receive Data 0 = Normal	R/LT	0
18.7	DCBAL	DC Balance Error	1 = DC Balance Error Detected On Receive Data 0 = Normal	R/LT	0
18.6	PRMBL	Preamble Error	1 = Preamble Error Detected On Receive Data 0 = Normal	R/LT	0
18.5	ASKEW	Align Skew Error	1 = Align Skew Error Detected On Receive Data 0 = Normal	R/LT	0
18.4	SPD_DET	100/10 Detect	1 = Device in 100BaseT4 Mode (100 Mbps) 0 = Device in 10BaseT Mode (10 Mbps)	R/LT	0
18.3	DPLX_DET	Duplex Detect	1 = Device In Full Duplex 0 = Device In Half Duplex	R/LT	0
18.2 18.1	ANEG_ST1 ANEG_ST0	AutoNegotiation Status	11 = AutoNegotiation Detected, Negotiation Started 10 = AutoNegotiation Detected, Negotiation Stuck 01 = AutoNegotiation Detected, Negotiation Done 00 = AutoNegotiation Not Detected	R/LT	00
18.0	JAB	Jabber Detect	1 = Jabber Detected 0 = Normal	R/LT	0

Table 14. Register 19 (Mask) Structure And Bit Definition

19.15	19.14	19.13	19.12	19.11	19.10	19.9	19.8
0	MASK_ LNK_FAIL	MASK_ INACT_D3	MASK_ INACT_D4	MASK_ RPOL	MASK_ PSWAP	MASK_ EOP	MASK_ CWRD
			R/W	R/W	R/W	R/W	R/W

19.7	19.6	19.5	19.4	19.3	19.2	19.1	19.0
MASK_ DCBAL	MASK_ PRMBL	MASK_ ASKEW	MASK_ SPD_DET	MASK_ DPLX_DET	MASK_ ANEG_ST1	MASK_ ANEG_ST0	MASK_ JAB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
19.15			Reserved, must be 0		0
19.14	MASK_ LNK_FAIL	Interrupt Mask - Link Fail Detect	1 = Mask Interrupt For LNK_FAIL In Register 18 0 = No Mask	R/W	1
19.13	MASK_ INACT_D3	Interrupt Mask - D3 Inactive	1 = Mask Interrupt For INACT_D3 In Register 18 0 = No Mask	R/W	1
19.12	MASK_ INACT_D4	Interrupt Mask - D4 Inactive	1 = Mask Interrupt For INACT_D4 In Register 18 0 = No Mask	R/W	1
19.11	MASK_ RPOL	Interrupt Mask - Reverse Polarity	1 = Mask Interrupt For RPOL In Register 18 0 = No Mask	R/W	1
19.10	MASK_ PSWAP	Interrupt Mask - Pair Swap Error	1 = Mask Interrupt For PSWAP In Register 18 0 = No Mask	R/W	1
19.9	MASK_ EOP	Interrupt Mask - EOP Error	1 = Mask Interrupt For EOP In Register 18 0 = No Mask	R/W	1
19.8	MASK_ CWRD	Interrupt Mask - Codeword Error	1 = Mask Interrupt For CWRD In Register 18 0 = No Mask	R/W	1
19.7	MASK_ DCBAL	Interrupt Mask - DC Balance Error	1 = Mask Interrupt For DCBAL In Register 18 0 = No Mask	R/W	1
19.6	MASK_ PRMBL	Interrupt Mask - Preamble Error	1 = Mask Interrupt For PRMBL In Register 18 0 = No Mask	R/W	1
19.5	MASK_ ASKEW	Interrupt Mask - Align Skew Error	1 = Mask Interrupt For ASKEW In Register 18 0 = No Mask	R/W	1
19.4	MASK_ SPD_DET	Interrupt Mask - 100/10 Detect	1 = Mask Interrupt For SPD_DET In Register 18 0 = No Mask	R/W	1
19.3	MASK_ DPLX_DET	Interrupt Mask - Duplex Detect	1 = Mask Interrupt For DPLX_DET In Register 18 0 = No Mask	R/W	1
19.2	MASK_ ANEG_ST1	Interrupt Mask - AutoNeg. Detect	1 = Mask Interrupt For ANEG_ST1 In Register 18 0 = No Mask	R/W	1
19.1	MASK_ ANEG_ST0	Interrupt Mask - AutoNeg. Detect	1 = Mask Interrupt For ANEG_ST0 In Register 18 0 = No Mask	R/W	1
19.0	MASK_ JAB	Interrupt Mask - Jabber Detect	1 = Mask Interrupt For JAB In Register 18 0 = No Mask	R/W	1

x.15 Bit Is Shifted First

5.0 Application Information

5.1 EXAMPLE SCHEMATICS

A typical example of the 80C240 used in an adapter card application is shown in Figure 14, a switching hub application is shown in Figure 15, and an external PHY application is shown in Figure 16.

5.2 TP TRANSMIT AND RECEIVE INTERFACE

The interface between the TP inputs/outputs on TX_D1±, RX_D2±, BI_D3±, and BI_D4± and the twisted pair cable is typically transformer coupled and terminated with a transformer and two resistors as shown in Figures 14-16.

The transformer specifications are shown in Table 15. Sources for the transformer are listed in Table 16.

Table 15. Transformer Specification

Parameter	Spec
Turns Ratio	2:1 CT
Inductance (µH Min)	350
Leakage Inductance (µH Max)	0.4
Capacitance (pF Max)	10
DC Resistance (Ohm Max)	0.4

Two external 200 ohm 1% resistors are needed from V_{CC} to the TX_D1±, RX_D2±, BI_D3±, and BI_D4± inputs/outputs to provide a 100 ohm termination impedance when looking back through the transformer from the twisted pair cable, as shown in Figures 14-16.

The 80C240 has special circuitry to reduce common mode noise on the twisted pair outputs. Common mode chokes may not be needed to meet emissions requirements in most applications and have been eliminated from the application schematics in Figure 14-16.

To minimize noise pickup, the loading on TX_D1±, RX_D2±, BI_D3±, and BI_D4± should be minimized and the positive and negative inputs/outputs should always be loaded equally.

Table 16. Transformer Sources

Vendor	Part Number
Valor	ST6111
NanoPulse	NP6127-30
PCA	EPE6129S
Belfuse	S553-1084-03
Pulse Engr	PE69001

5.3 TP TRANSMIT OUTPUT CURRENT SET

The TP output current level is set by an external resistor tied between REXT and GND. The output current is determined by the following equation where R is the value of REXT:

$$I_{out} = (R/10K) * I_{REF}$$

Where I_{REF} = 70 mA for 100 Mbps
= 50 mA for 10 Mbps

REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels.

Keep REXT close to the REXT and GND pins as possible in order to reduce noise pickup into the transmitter.

Since the TP output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it is necessary to minimize PC board loading effect in order to meet transmit amplitude and pulse shape as specified in IEEE 802.3 documents.

5.4 TRANSMITTER DROOP

The IEEE 802.3 Section 23 specification has a droop specification at the transmit output. Since the 80C240 TP output is a current source, it has no perceptible droop by itself. However, the open circuit inductance of the transformer added to the device transmitter output as shown in Figures 14-16 will cause droop to appear at the transmit interface to the TP wire. If the transformer connected to the 80C240 outputs meets the requirements in Table 15, the transmit interface to the TP cable will meet the IEEE 802.3 Section 23 droop requirements.

5.5 CONTROLLER INTERFACE

5.5.1 General

The controller interface will connect to any MII Ethernet controller without any glue logic provided that the external Ethernet controller has a MII interface that complies with IEEE 802.3 as shown in Figures 14 and 15.

5.5.2 Clocks

A 50 Mhz clock output is provided on the TX_CLK50 pin. This clock may be useful as a master clock to an external Ethernet controller. Due to its high frequency, TX_CLK50 can only drive a 25 pF load. Thus, the TX_CLK50 output

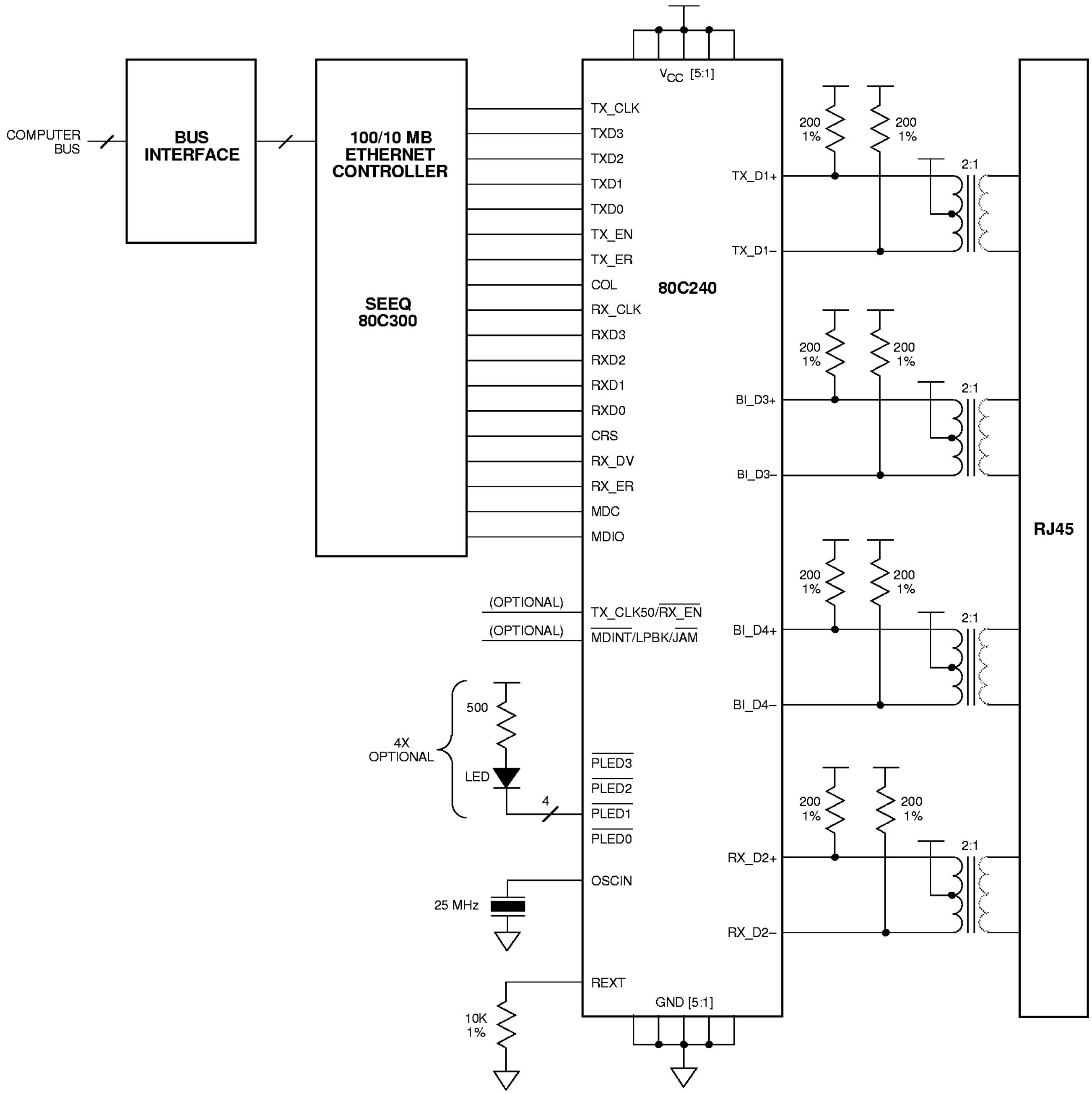


Figure 14. Typical Adapter Card schematic Using 80C240

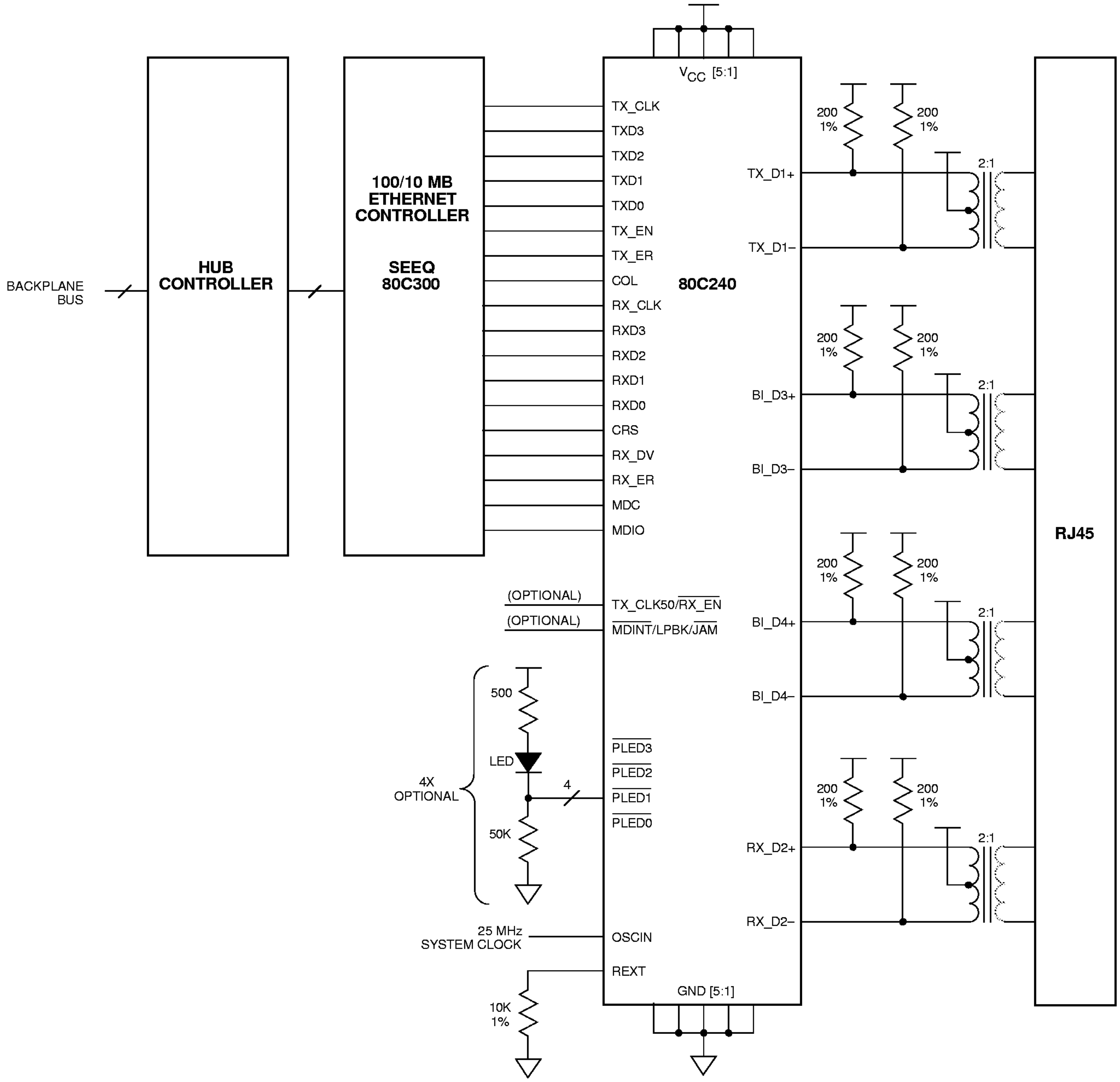


Figure 15. Typical Switching Hub Schematic Using 80C240

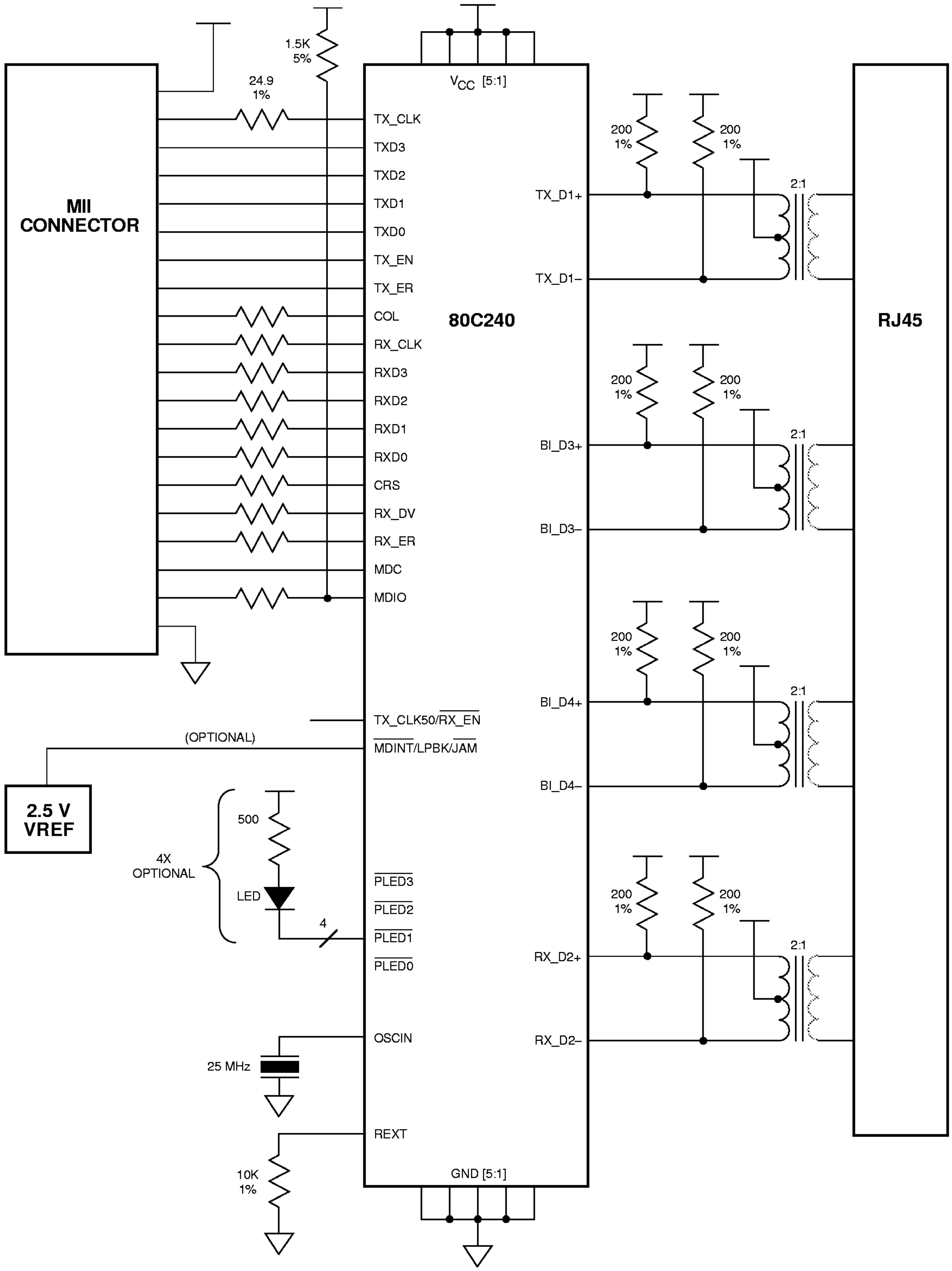


Figure 16. Typical External PHY Schematic Using 80C240

can only directly drive a single input and any stray capacitance on TX_CLK50 must be minimized. The output can be externally buffered if greater drive requirements are needed.

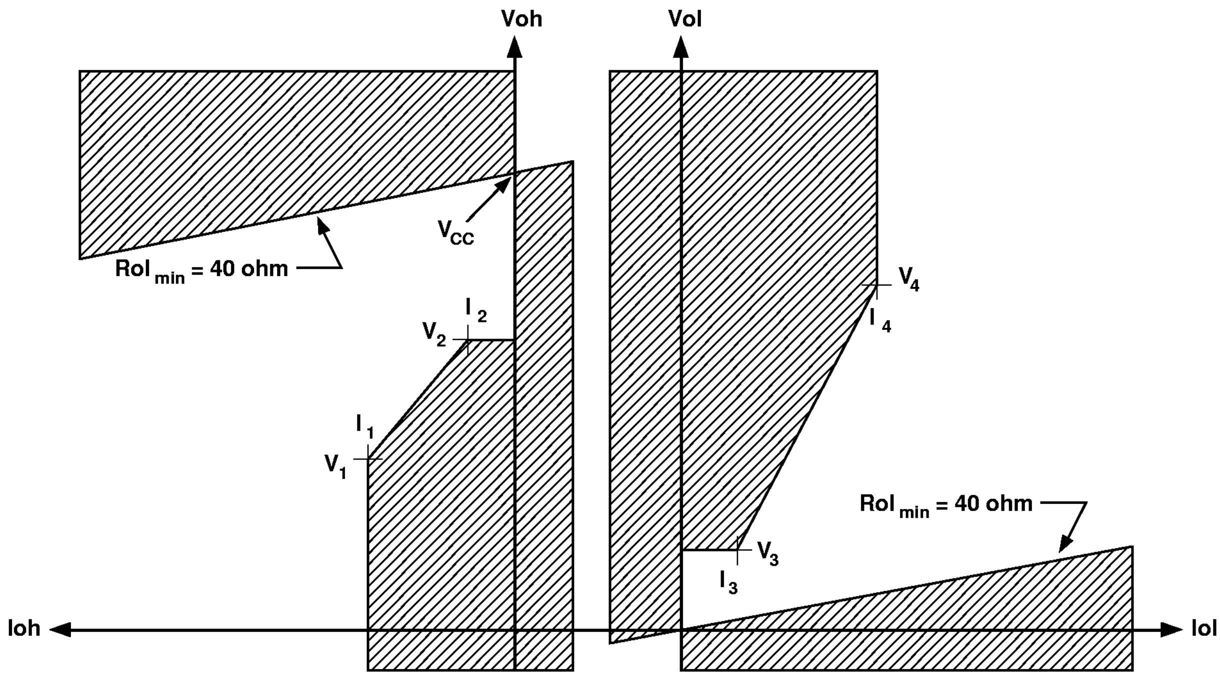
Standard Ethernet controllers with a MII use the output clock TX_CLK to clock data on TXD[3:0]. If a nonstandard controller or ASIC controller is used, there might be a need to clock TXD[3:0] into the 80C240 on the edges of an external master clock which would be an input to the 80C240. This can be done by using OSCIN as the master clock input. OSCIN generates TX_CLK inside the 80C240; thus, TXD[3:0] data can be clocked into the 80C240 on edges of output clock TX_CLK or input clock OSCIN. In the case where OSCIN is used as the input clock, a crystal is no longer needed on OSCIN, and TX_CLK can be left open or used for some other purpose.

5.5.3 Output Drive

The digital outputs on the 80C240 controller signals can meet the MI driver characteristics specified in IEEE 802.3 Section 22 specification and shown in Figure 17 if external 24.9 ohm 1% termination resistors are added. These termination resistors are only needed if the outputs have to drive a MII cable or other transmission line type load, such as in the external PHY application shown in Figure 16. If the 80C240 is used in internal applications such as adapter cards and switching hubs, as shown in Figure 14 and 15, then these terminations resistors may not be needed.

5.5.4 MII Disable

The MII outputs can be placed in the high impedance state and inputs disabled by setting the MII disable bit in the MI



I - V	I (mA)	V (Volts)
I_1, V_1	–20	1.10
I_2, V_2	–4	2.4
I_3, V_3	4	0.40
I_4, V_4	43	3.05

Roh_{min} Rol_{min} equals 40 ohms

Figure 17. MII Output Driver Characteristics

serial port Control register. When this bit is set to disable state, the TP outputs are also disabled. The default value of this bit when the device powers up or is reset is dependent on the device address. If the device address latched into MDA[4:0] at reset is 11111, it is assumed that the device is being used in applications where many devices could be sharing the MII bus, like adapter card or external PHY's, and the device powers up with the MII interface disabled. If the device address latched into MDA[4:0] at reset is not 11111, it is assumed that the device is being used in application where it is the only device on the MII bus, like hubs, and the device powers up with the MII interface enabled.

5.5.5 Receive Enable Output

The 80C240 has a receive output enable input pin, RX_EN, which when asserted forces the MII outputs (RX_CLK, RXD[3;0], RX_DV, RX_ER, and (COL) into the high impedance state.

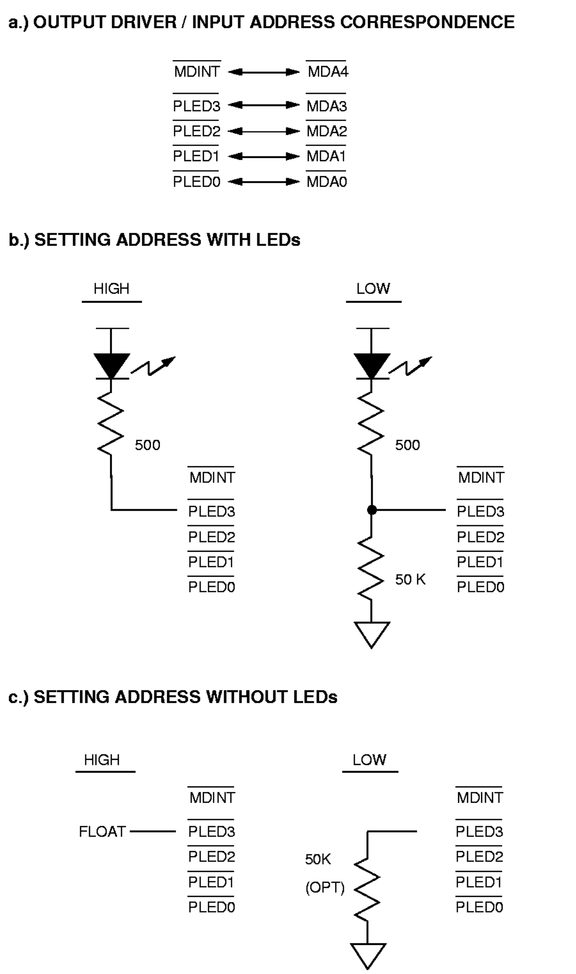


Figure 18. Serial Port Device Address Selection

RX_EN can be used to "wire Or" the outputs of many 80C240 devices in a multiport application like a repeater. By monitoring CRS from each individual port, the repeater controller can assert only the RX_EN line to that 80C240 device which is receiving data. This method will reduce, by 8 per device, the number of pins and PCB traces required on a repeater core IC.

The RX_EN function can be enabled by setting the Pin 34 Configuration bit in the MI serial port Configuration 1 register. When this bit is set, the TX_CLK50/RX_EN pin (Pin 34) becomes the RX_EN input and no longer outputs a 50 MHz clock and the MDA4 MI address is permanently forced high.

5.5.6 CRS Assert Delay

The IEEE 802.3 Section 23 specification defines that the CRS assert time be artificially delayed from its minimum value in order to meet the fairness timing parameter. There are some applications, like repeaters, where this artificial CRS assert delay is not needed or desired. The 80C240 has the ability to program the CRS assert delay time (t_{31}) to either the IEEE 802.3 mandated time with the artifical delay (215-275 nS) or to the device minimum without the artifical delay (0-155 nS). The CRS assert delay time is programmable with the CRS assert delay bit in the MI serial port Configuration 1 register. Programming the CRS assert delay bit high also disables the internal TX_EN to CRS loopback path.

5.6 MI SERIAL PORT

5.6.1 General

The 80C240 has a MI serial port to set all of the device's configuration inputs and read out the status outputs. Any external device that has a IEEE 802.3 compliant MI interface can connect directly to the 80C240 without any glue logic, as shown in Figures 14 and 15.

As described earlier, the MI serial port consists of 8 lines: MDC, MDIO, MDINT, and MDA[4:0]. However, only 2 lines, MDC and MDIO are needed to shift data in and out. MDINT and MDA[4:0] are provided for convenience only.

The MDA[4:0] addressed are inverted inside the 80C240 before going to the MI Serial port block. For example, the MDA[4:0] pins would have to be pin strapped to 11111 externally in order to successfully match PHYAD[4:0] = 00000 internally.

5.6.2 Polling vs. Interrupt

The status output bits can be monitored by either polling the serial port or with interrupt.

If polling is used, the registers can be read at regular intervals and the status bits can be checked against their previous values to determine any changes. To make polling simpler, all the registers can be accessed on a single read cycle by setting the register address bits REGAD[4:0] to 11111 and adding enough clocks to read out all the bits, provided the multiple register access feature has been enabled.

The interrupt features offers the ability to detect changes in the status output bits without constant register polling. Assertion of interrupt indicates that one or more of the status output bits has changed since the last read cycle. There are three interrupt output indicators: (1) MDINT/LPBK/JAM pin when programmed for interrupt output, (2) INT bit in MI serial port Status Output register, and (3) interrupt pulse on MDIO when programmed for interrupt pulse. These interrupt signals can be used by an external device to initiate a read cycle. Then when an interrupt is detected, the individual registers (or multiple registers) can be read out and the status bits compared against their previous values to determine any changes. After the interrupt bits have been read out, the interrupt signals are automatically deasserted. A mask register bit for every status output bit exists in the Mask register so that the interrupt bits can be individually programmed for each application.

5.6.3 Serial Port Addressing

The device address for the MI serial port is selected by tying the MDA[4:0] pins to the desired value. MDA[4:0] share the same pins as the TX_CLK50 and PLED[3:0] outputs, respectively, as shown in Figure 18a. At powerup or reset, the output drivers are tristated for an interval called the poweron reset time. During the poweron reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port address. The LED outputs are open drain with internal resistor pullup to V_{CC}.

If an LED is desired on the LED outputs, then an LED and resistor are tied to V_{CC} as shown in Figures 18b. If a high address is desired, the LED to V_{CC} automatically makes the latched address value a high. If a low value for the address is desired, a 50K resistor to GND must be added as shown in Figure 18b.

If no LED's are needed on the LED outputs, the selection of addresses can be done without any external components as shown in Figure 18c. If a high address is desired, the pin should be left floating and the internal pullup will pull the pin high during poweron reset and latch in a high address value. If a low address is desired, the output pin should be tied to GND (except TX_CLK50 which should be tied to GND through a 50K resistor).

5.7 LONG CABLE

IEEE 802.3 specifies that 10BaseT and 100BaseT4 operate over twisted pair cable lengths of between 0-100 meters. If the receive level adjust bit is set in the MI serial port Configuration 1 register, the squelch levels are reduced by 4.5 dB which will allow the 80C240 to operate with up to 150 meters of twisted pair cable. The equalizer and aligner are already designed to accommodate between 0-150 meters of cable.

5.8 AUTOMATIC JAM

The 80C240 has an automatic JAM generation feature which automatically transmits a JAM packet when receive activity is detected. This feature is primarily designed to give the user a means to easily implement flow control. In a typical application, a watermark signal from a system FIFO can be tied directly to the JAM pin. Thus, when the system FIFO is full, and more data is incoming, the device will automatically transmit a JAM packet and thus create a collision which will cause the far end device to backoff until the system FIFO can empty itself.

The JAM feature can be made available by appropriately setting the pin 11 configuration select bit in the MI Serial Port Configuration 1 register. When the bit is set, the MDINT/LPBK/JAM pin (Pin 11) becomes a JAM input and the interrupt output and loopback input hardware function are disabled (both still active through Serial Port).

5.9 OSCILLATOR

The 80C240 requires a 25 Mhz reference frequency for internal signal generation. This 25 Mhz reference frequency can be generated by either connecting an external 25 MHz crystal between OSCIN and GND, or by applying an external 25 MHz clock to OSCIN.

If the crystal oscillator is used, it needs only an external crystal, and no other external capacitors or other components are required. The crystal must have the characteristics shown in Table 17. The crystal must be placed as close as possible to OSCIN and GND so that parasitics on OSCIN are kept to a minimum.

Table 17. Crystal Specifications

Parameter	Spec
Type	Parallel Resonant
Frequency	25 Mhz +/- 0.01%
Equivelent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Power Dissipation	1mW max

5.10 LED DRIVERS

The PLED[3:0] outputs can all drive LED's tied to V_{cc} as shown in Figures 14-16. The PLED[3:0] outputs can be programmed through the MI serial port to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink. PLED[3:0] can be programmed to one of these functions by appropriately setting the LED output select bits in the MI serial port Configuration 2 register. When PLED[3:0] is programmed for its Normal function, these outputs indicate the specific functions described in the MI serial port Configuration 2 register shown on Table 12 (Link Detect, Activity, Full Duplex Detect, and 100Mbps Detect). When PLED[3:0] is programmed to be On, the LED output driver go low, thus turning on the LED under user control. When PLED[3:0] is programmed to be Off, the LED output driver will turn off, thus turning off the LED under user control. When PLED[3:0] is programmed to Blink, the LED output driver will continuously blink at a rate of 100 mS on, 100 mS off.

The normal functions for PLED[3:0] can be changed from Link Detect, Activity, Full Duplex Detect, 100 Mbps Detect to Link Detect 100 Mbps, Activity, Full Duplex Detect, Link detect 10 Mbps by appropriately setting the LED default Select bit in the MI serial Port Configuration 2 Register.

The On and Off functions allow the LED driver to be controlled directly through the MI serial port to indicate any function that is desired under external control. The Blink function allows the same external control of the LED driver and also offers the provision to blink the LED without the need for any external timers.

The PLED[3:0] outputs can also drive other digital inputs. Thus, PLED[3:0] can also be used as digital outputs whose function can be user defined and controlled through the MI serial port.

5.11 EXTERNAL PHY APPLICATION

The 80C240 can be used in external PHY applications as shown in the schematic in Figure 16. The TP and MII interface external components were discussed in previous sections. One additional requirement might be the additional of an external reference, as shown in Figure 16.

The 80C240 uses an internal reference derived from V_{cc} to set the output level. The 80C240 requires V_{cc} to be 5V ± 5% in order to meet the IEEE 802.3 specified output levels. If an MII cable is used to connect an external PHY using the 80C240 to a MII connector, V_{cc} is supplied through the MII cable and might have a tolerance of ±10%. If the supply tolerance is greater than ± 5% to the 80C240, it will not meet the IEEE 802.3 specified output level. In order to meet the IEEE 802.3 output level requirements if the supply tolerance is ± 10%, an external reference is required for the 80C240. This external reference is supplied to the device through the MDINT pin when the external reference bit is set in the MI serial port Configuration 1 register. The external reference to the 80C240 must be 2.5V ±5% in order to meet the IEEE 802.3 specified output level.

5.12 POWER SUPPLY DECOUPLING

There are five V_{cc}'s on the 80C240 (V_{cc}[5:1]) and five GND's (GND[5:1]).

All five V_{cc}'s should be connected together as close as possible to the device with a large V_{cc} plane. If the V_{cc}'s vary in potential by even a small amount, noise and latchup can result. The V_{cc}'s should be kept to within 25 mV of each other.

All five GND's should also be connected together as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result. The GND's should be kept to within 25 mV of each other.

A 0.01-0 µF decoupling capacitor should be connected between each V_{cc}/GND set as close as possible to the device pins, preferably within 0.5" . The value should be chosen on whether the noise between V_{cc} and GND is high or low frequency. A conservative approach would be to *use two decoupling capacitors on each V_{CC}/GND set (except V_{CC2}/GND 2), one 0.1 µF for low frequency and one 0.001µF for high frequency noise on the power supply.*

The V_{CC} connection to the transmit transformer center tap shown in Figures 14-16 has to be well decoupled in order to minimized common mode noise injection from the supply into the twisted pair cable. It is recommended that a 0.01 µF decoupling capacitor be placed between the center tap V_{CC} to the 80C240 GND plane. This decoupling capacitor should be physically placed as close as possible to the transformer center tap, preferably within 0.5".

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device: (1) The resultant AC noise voltage measured across each V_{CC}/GND set should be less than 100 mVpp, (2) All V_{CC}'s should be within 50 mVpp of each other, and (3) All GND's should be within 50 mVpp of each other.

6.0 Specifications

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

VCC Supply Voltage ....-.3V to 6.0V

All Inputs and Outputs
with Respect to GND ....-.3V to VCC+.3V

Input Latchup Current ....+/-100 mA
Package Power Dissipation .... 2.2 Watt @ 70 °C
Storage Temperature ....-65 to +150°C
Temperature Under Bias............................ -10 to +80°C
Lead Temperature (Soldering, 10 Sec) .... 260°C
Body Temperature (Soldering, 30 Sec) ....220°C

DC Electrical Characteristics

Unless otherwise noted, all test conditions are as follows:

1. T = 0 to +70°C
2. V_{CC} = 5V +/–5%
3. 25 Mhz +/– 0.01%
4. REXT = 10K +/– 1%, no load

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
V_{IL}	Input Low Voltage			0.8	Volt	All except OSCIN, $\overline{\text{MDA[4:0]}}$
				V_{CC} – 1.0	Volt	$\overline{\text{MDA[4:0]}}$
				1.5	Volt	OSCIN
V_{IH}	Input High Voltage	2			Volt	All except OSCIN, $\overline{\text{MDA[4:0]}}$
		V_{CC} –0.5			Volt	$\overline{\text{MDA[4:0]}}$
		3.5			Volt	OSCIN
I_{IL}	Input Low Current			–1	µA	V_{IN} = GND All Except OSCIN PLED[3:0], TX_CLK50/$\overline{\text{RX\_EN}}$ MDINT/LPBK/JAM
		–3	–8	–25	µA	V_{IN} = GND $\overline{\text{PLED[3:0]}}$,$\overline{\text{TX\_CLK50}}$/$\overline{\text{RX\_EN}}$ MDINT/LPBK/JAM
		–20		–100	µA	V_{IN} = GND OSCIN
I_{IH}	Input High Current			1	µA	V_{IN} = V_{CC} All Except OSCIN
		30		150	µA	V_{IN} = V_{CC} OSCIN
V_{OL}	Output Low Voltage			0.4	Volt	I_{OL} = –4mA All Except $\overline{\text{PLED[3:0]}}$
				1	Volt	I_{OL} = –20mA $\overline{\text{PLED[3:0]}}$
V_{OH}	Output High Voltage	4			Volt	I_{OH} = 4mA All Except $\overline{\text{PLED[3:0]}}$, $\overline{\text{MDINT}}$
		2.4			Volt	I_{OH} = 3 µA $\overline{\text{PLED[3:0]}}$, $\overline{\text{MDINT}}$
C_{IN}	Input Capacitance		5		pF	
I_{CC}	V_{CC} Supply Current			520	mA	Transmitting
				0.1	mA	Powerdown Mode

Twisted Pair Characteristics, Transmit

Unless otherwise noted, all test conditions are as follows:

1. T = 0 to +70°C
2. V_{CC} = 5V +/–5%
3. 25 Mhz +/– 0.01%
4. REXT = 10K +/– 1%, no load
5. TPO± Loading shown in Figure 13 or equivalent.

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
T_{OV}	TP Differential Output	3.15	3.5	3.85	V pk	V_{CC} = 5V + 5%, 100Base-T4
	Voltage	2.2	2.5	2.8	V pk	V_{CC} = 5V + 5%, 10Base-T
T_{OVT}	TP Differential Output	See Figure 5				100 Mbps
	Voltage Template	See Figure 7				10 Mbps
T_{ISI}	TP Differential Output ISI Template	See Figure 6				100 Mbps
T_{SOI}	TP Differential Output SOI Voltage Template	See Figure 9				10 Mbps
T_{LPT}	TP Differential Output Link Pulse Voltage Template	See Figure 11				T4LP
		See Figure 10				NLP and FLP
T_{OIV}	TP Differential Output Idle Voltage			+/- 50	mV	Measured on Secondary Side of Xfmr on Figure 14
T_{OIA}	TP Output Current	63	70	77	mA pk	100 Mbps
		44	50	56	mA pk	10 Mbps
T_{CMA}	TP Common Mode AC Output Voltage			20	mV pk	
T_{HD}	TP Harmonic Distortion			-27	dB	All 1's output
T_{OR}	TP Output Resistance		10K		Ohm	
T_{OC}	TP Output Capacitance		15		pF	

Twisted Pair Characteristics, Receive

Unless otherwise noted, all test conditions are as follows:

1. T = 0 to +70°C
2. V_{CC} = 5V +/-5%
3. 25 Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. 12.5/10 Mhz sinewave on TP inputs in 100/10 Mbps

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
R_{STP}	TP Input Squelch	325		467	mV pk	
	Threshold, Positive	195		280	mV pk	RLVL0 = 1
R_{STN}	TP Input Squelch	–125		–225	mV pk	
	Threshold, Negative	–75		–135	mV pk	RLVL0 = 1
R_{UTP}	TP Input Unsquelch	325		467	mV pk	10 Mbps
	Threshold, Positive	195		280	mV pk	10 Mbps, RLVL = 1
R_{UTN}	TP Input Unsquelch	–95		–175	mV pk	10 Mbps
	Threshold, Negative	–55		–105	mV pk	10 Mbps, RLVL = 1
R_{OCV}	TP Input Open Circuit Voltage	V_{CC}–0.95	V_{CC}	V_{CC}+0.65	Volt	
R_{CMR}	TP Input Common Mode Voltage Range	V_{CC}–2.55		V_{CC}+2.55	Volt	
R_{DR}	TP Input Differential Voltage Range	GND		V_{CC}+2.55	Volt	
R_{CRR}	TP Input Common Mode Rejection Ratio			–20	dB	0 – 10Mhz
R_{IR}	TP Input Resistance	5K			ohm	
R_{IC}	TP Input Capacitance		10		pF	

AC Test Timing Conditions

Unless otherwise noted, all test conditions are as follows:

1. T = 0 to +70°C
2. V_{CC} = 5V +/-5%
3. 25 Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. Input conditions:
   All Inputs: tr,tf <= 10nS, 20-80%
6. Output Loading
   D1±, D2±, D3±, D4±: See Figure 14 or equivalent
   TX_CLK50: 25pF
   Open Drain Outputs: 1K Pullup, 50pF
   All Other Digital Outputs: 50pF
7. Measurement Points:
   D1±, D2±, D3±, D4±: 0v During Data, ±0.3V at start/end of packet
   All other inputs and outputs: 1.5 Volts

25 MHz Input/50 MHz Output Clock Timing Characteristics

Refer To Figure 19 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	OSCIN Cycle Time	39.996	40	40.004	nS	
t_2	OSCIN High Time	16			nS	
t_3	OSCIN Low Time	16			nS	
t_4	TX_CLK50 Cycle Time	19.998	20	20.002	nS	
t_5	TX_CLK50 High Time	6		14	nS	
t_6	TX_CLK50 Low Time	6		14	nS	
t_7	TX_CLK50 Rise/Fall Time			10	nS	
t_8	OSCIN to TX_CLK50 Delay			10	nS	
t_9	OSCIN to TX_CLK Delay			10	nS	

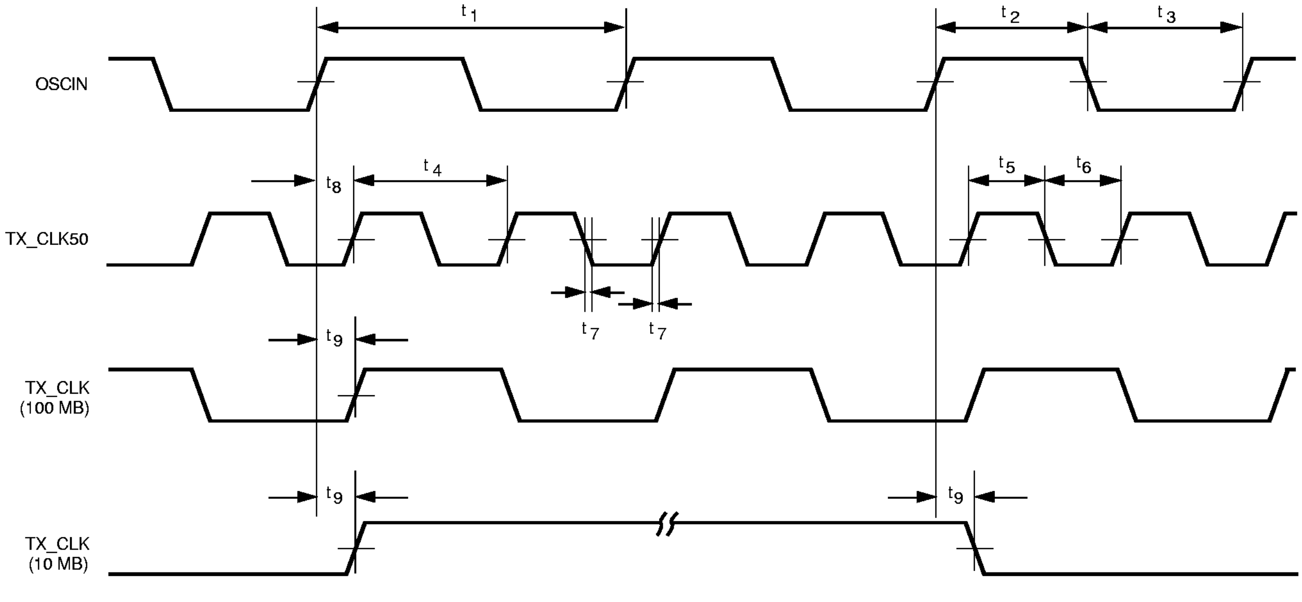


Figure 19. 25 Mhz Input / 50 Mhz Output TIming

Transmit Timing Characteristics

Refer To Figures 20 and 21 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{11}	TX_CLK Cycle Time	39.996	40	40.004	nS	100 Mbps, MII
		399.96	400	400.04	nS	10 Mbps, MII
		99.99	100	100.01	nS	10 Mbps, BII
t_{12}	TX_CLK Low Time	16	20	24	nS	100 Mbps, MII
		160	200	240	nS	10 Mbps, MII
		40	50	60	nS	10 Mbps, BII
t_{13}	TX_CLK High Time	16	20	24	nS	100 Mbps, MII
		160	200	240	nS	10 Mbps, MII
		40	50	60	nS	10 Mbps, BII
t_{14}	TX_CLK Rise/Fall Time			10	nS	
t_{15}	TX_EN Setup Time	10			nS	
t_{16}	TX_EN Hold Time	0			nS	
t_{17}	CRS During Transmit Assert Time			40	nS	
t_{18}	CRS During Transmit Deassert Time			360	nS	
t_{19}	TXD Setup Time	10			nS	
t_{20}	TXD Hold Time	0			nS	
t_{21}	TX_ER Setup Time	10			nS	
t_{22}	TX_ER Hold Time	0			nS	
t_{23}	Transmit Propagation Delay			175	nS	100 Mbps, MII
				600	nS	10 Mbps, MII
				300	nS	10 Mbps, BII
t_{24}	Transmit Output Jitter			± 4.0	nS	100 Mbps
				± 5.5	nS	10 Mbps
t_{24a}	Transmit Output Skew			± 0.50	nS	100 Mbps
t_{25}	Transmit SOI Pulse Width To 0.3V	250			nS	10 Mbps
t_{26}	Transmit SOI Pulse Width to 40 mV			4500	nS	10 Mbps
t_{27}	$\overline{\text{PLED2}}$ Delay Time			200	nS	$\overline{\text{PLED2}}$ Programmed for Activity
t_{28}	$\overline{\text{PLED2}}$ Pulse Width	80		105	mS	$\overline{\text{PLED2}}$ Programmed for Activity

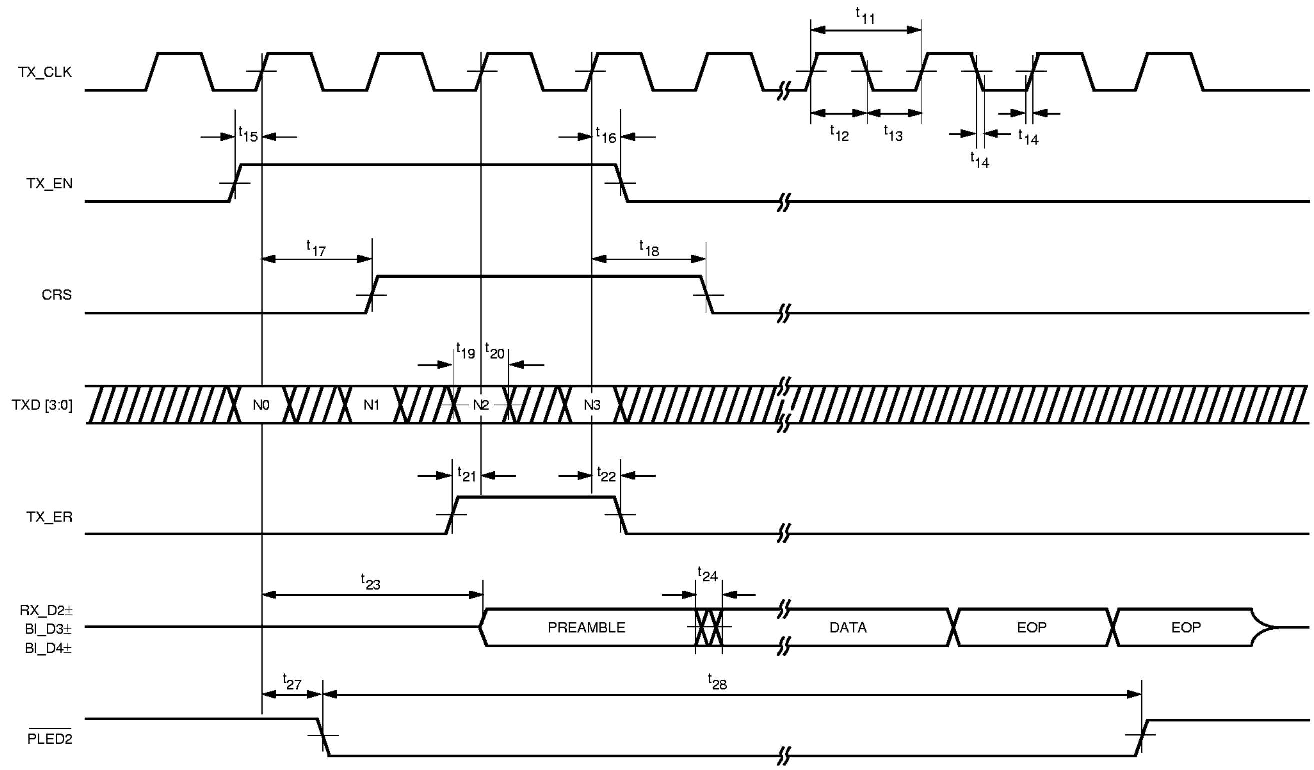
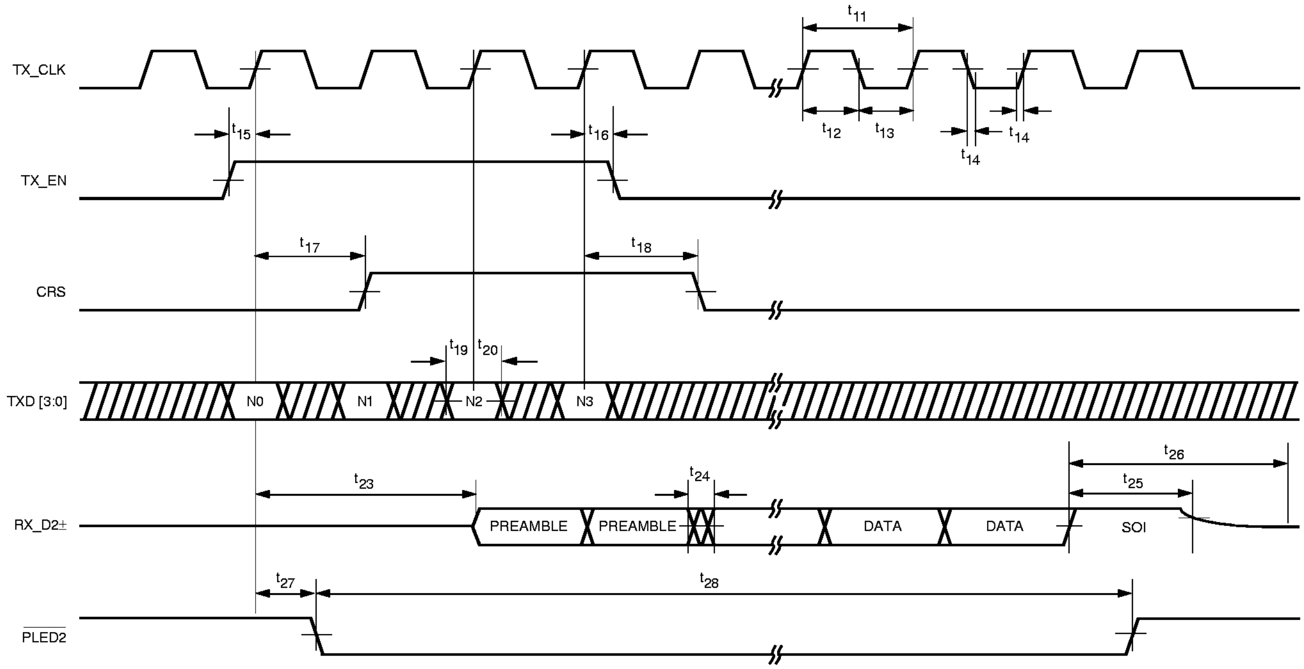


Figure 20. Transmit Timing - 100 Mbps

MII 10 MB



BII 10 MB

Same as MII 10 MB Except:

a) TX_CLK = 10 MHz.
b) Data in on TXD0 Only.

Figure 21. Transmit Timing - 10 Mbps

Receive Timing Characteristics

Refer To Figures 22, 23, 24, 25 and 26 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{31}	Start Of Packet To CRS Assert Delay	215		275	nS	100 Mbps
				155	nS	100 Mbs, Bit CRS_AST = 1
				700	nS	10 Mbps
t_{32}	End Of Packet To CRS Deassert Delay			495	nS	100 Mbps
				600	nS	10 Mbps Relative To Start Of SOI Pulse
t_{33}	Start Of Packet To RX_DV Assert Delay	810		1145	nS	100 Mbps
				3600	nS	10 Mbps
t_{34}	End Of Packet To RX_DV Deassert Delay			495	nS	100 Mbps
				700	nS	10 Mbps Relative To Start Of SOI Pulse
t_{36}	Start of Packet to First Data Nibble Delay	670		1145	nS	100 Mbps
				7200	nS	10 Mbps
t_{37}	RX_CLK To RX_DV, RXD, RX_ER Delay	-8		8	nS	
t_{38}	RX_CLK High Time	18	20	22	nS	100 Mbps, MII
		180	200	220	nS	10 Mbps, MII
		45	50	55	nS	10 Mbps, BII
t_{39}	RX_CLK Low Time	18	20	60	nS	100 Mbps, MII
		180	200	600	nS	10 Mbps, MII
		45	50	150	nS	10 Mbps, BII
t_{40}	SOI Pulse Width Required For Idle Detection	125			nS	10 Mbps Measure RX_D2± from last zero cross to 0.3V point.
t_{41}	Receive Input Jitter			±9.5	nS	100 Mbps
				±13.5	nS	10 Mbps
t_{42}	Receive Align Skew	90		120	nS	100 Mbps
t_{43}	$\overline{\text{PLED2}}$ Delay Time			200	nS	$\overline{\text{PLED2}}$ Programmed For Activity
t_{44}	$\overline{\text{PLED2}}$ Pulse Width	80		105	mS	$\overline{\text{PLED2}}$ Programmed For Activity
t_{45}	RX_CLK, RXD, CRS, RX_DV, RX_ER Output Rise And Fall Times			10	nS	
t_{46}	$\overline{\text{RX\_EN}}$ to Hi-Z Delay			40	nS	

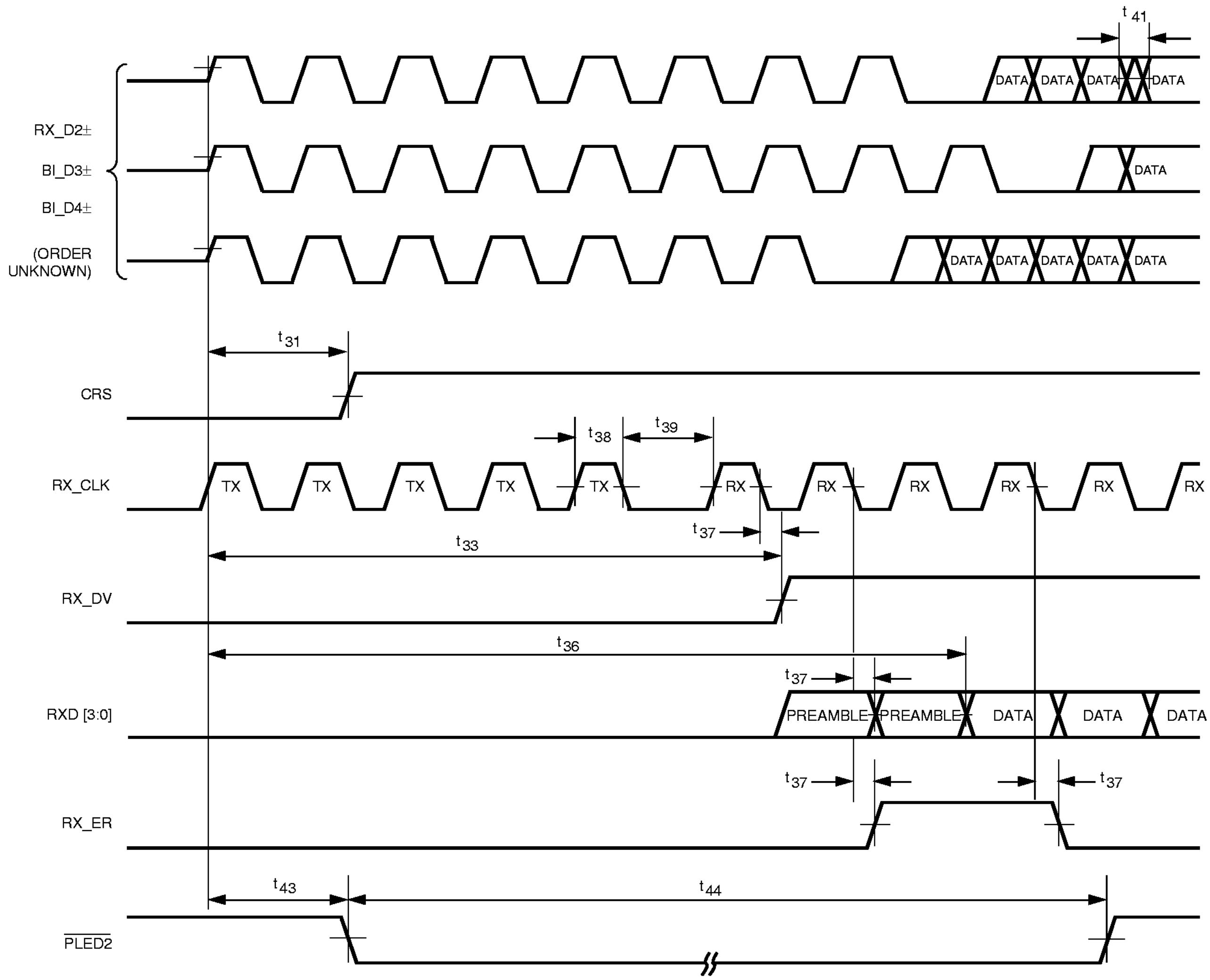


Figure 22. Receive Timing, Start of Packet - 100 Mbps

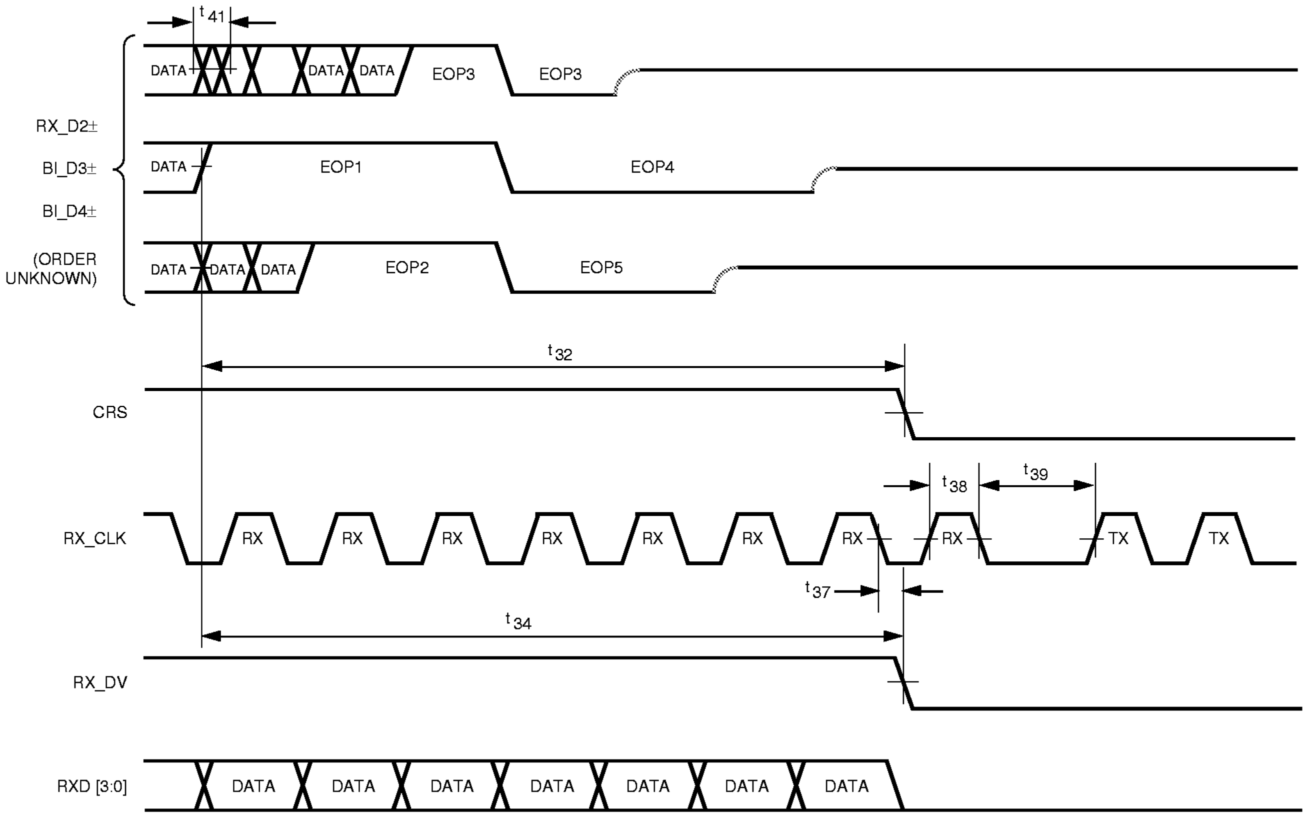
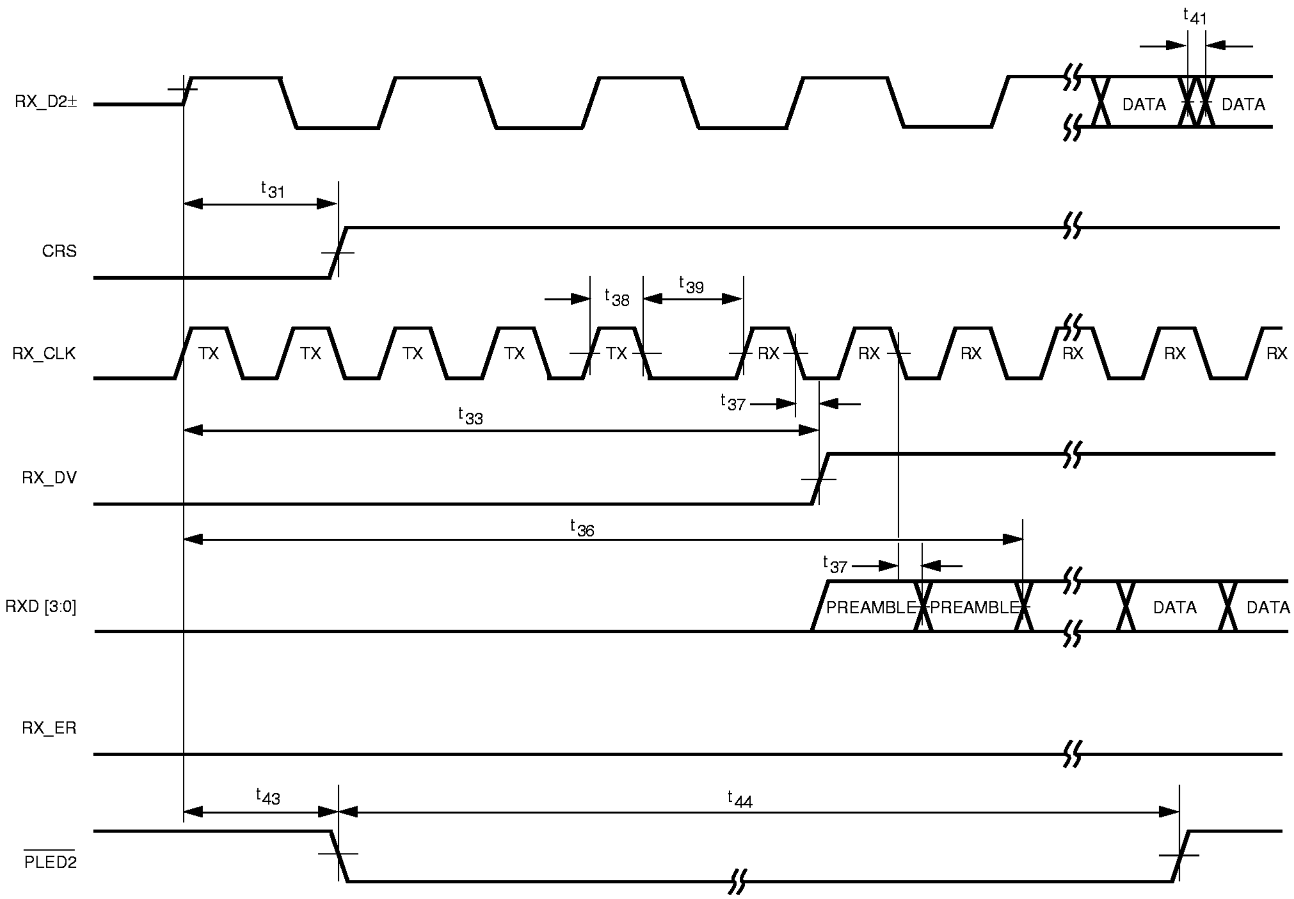


Figure 23. Receive Timing, End of Packet - 100 Mbps

MII 10 MB



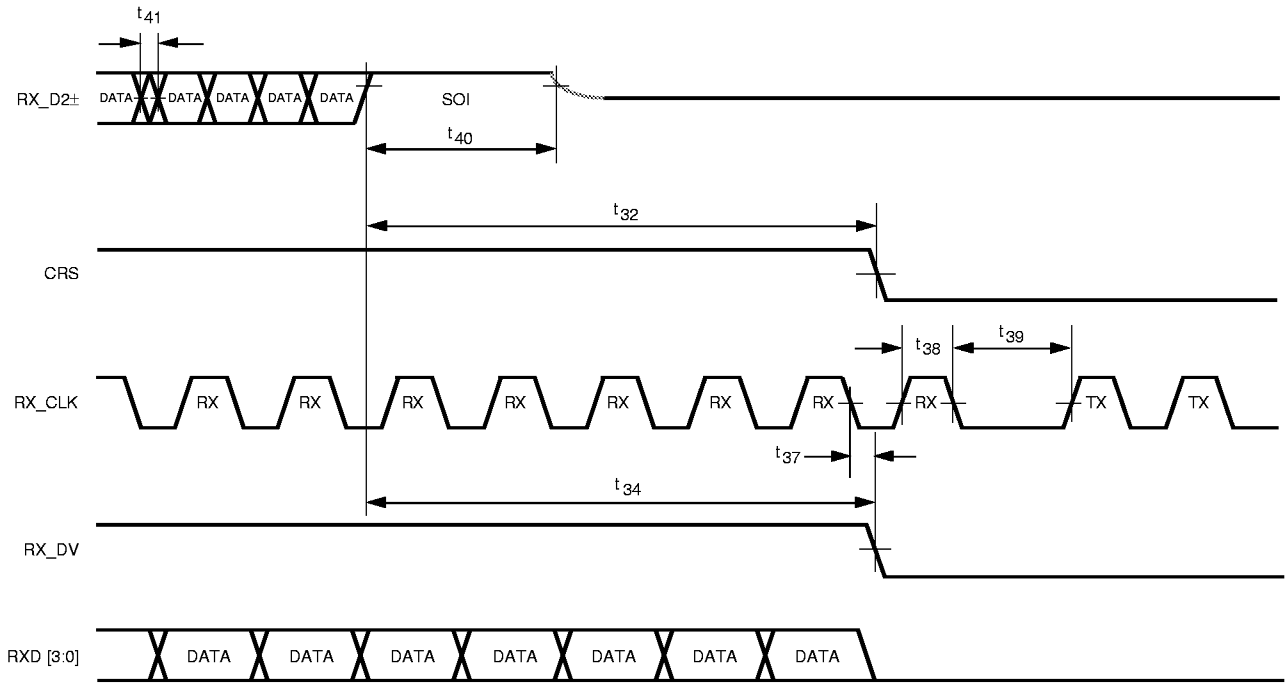
BII 10 MB

Same as MI 10 MB Except:

a) RX_CLK = 10 MHz.
b) Data Out on RXD0 only.

Figure 24. Receive Timing, Start of Packet - 10 Mbps

MII 10 MB



BII 10 MB

Same as MI 10 MB Except:

a) RX_CLK = 10 MHz.
b) Data Out on RXD0 only.

Figure 25. Receive Timing, End of Packet - 10 Mbps

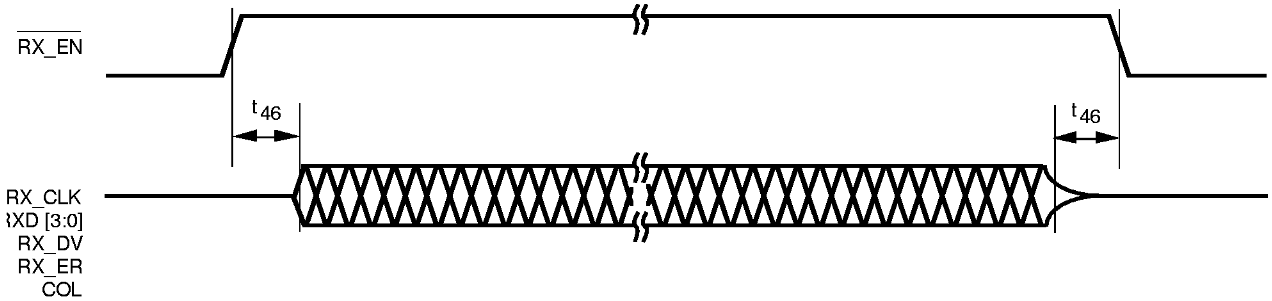


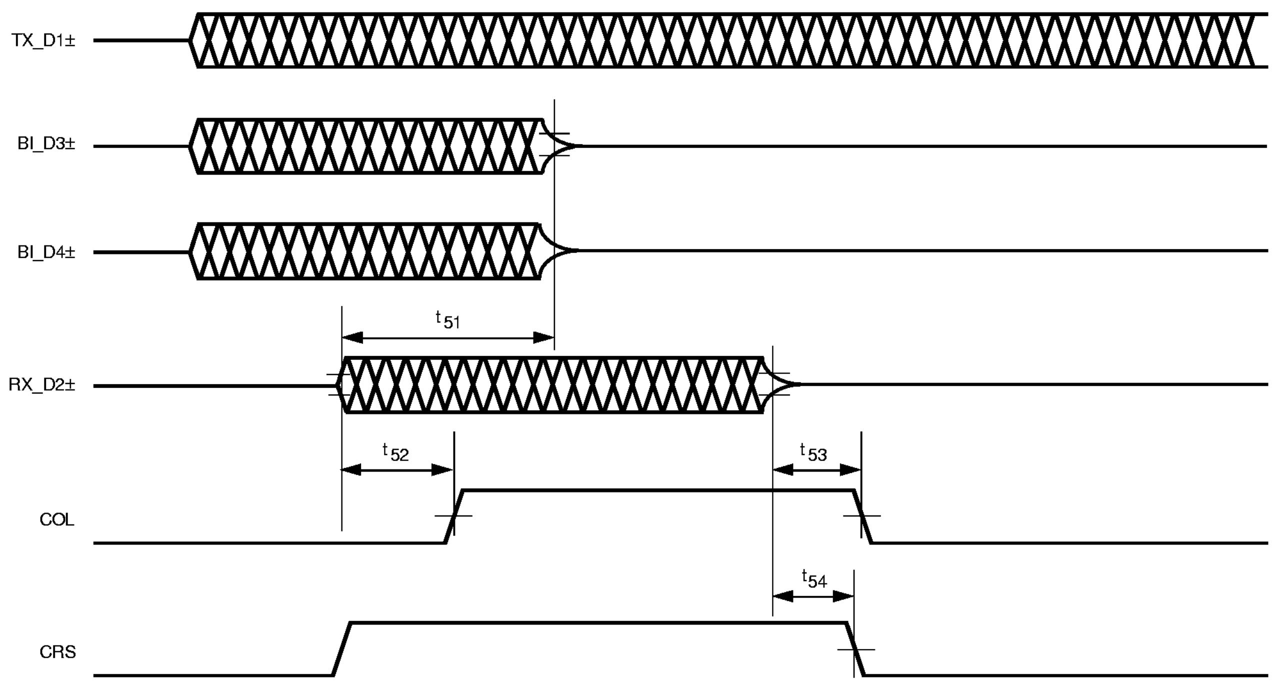
Figure 26. RX_EN Timing

Collision and Jam Timing Characteristics

Refer To Figures 27, 28, 29 and 30 for Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	Rcv Packet Start to Xmt Packet Stop Time			155	nS	100 Mbps
t_{52}	Rcv Packet Start to			275	nS	100 Mbps
	COL Assert Time			700	nS	10 Mbps
t_{53}	Rcv Packet Stop to			515	nS	100 Mbps
	COL Deassert Time			300	nS	10 Mbps
t_{54}	Rcv Packet Stop to	30		505	nS	100 Mbps
	CRS Deassert Time			300	nS	10 Mbps
t_{55}	TXEN Assert to COL Assert Time			40	nS	
t_{56}	TXEN Deassert to COL Deassert Delay Time			360	nS	
t_{57}	TXEN Deassert to CRS Deassert Delay Time			360	nS	
t_{57a}	COL Rise and Fall Time			10	nS	
t_{58}	Collision Test Assert Time			5120	nS	
t_{59}	Collision Test Deassert Time			40	nS	
t_{60a}	CRS Assert to Xmt JAM Packet Start During JAM			100	nS	
t_{60b}	CRS Assert to COL Assert During JAM			100	nS	
t_{60c}	Rcv Packet Stop to COL Deassert During JAM			440	nS	

MII 100 MB



MII 10 MB

Same as MII 100 MB Except:

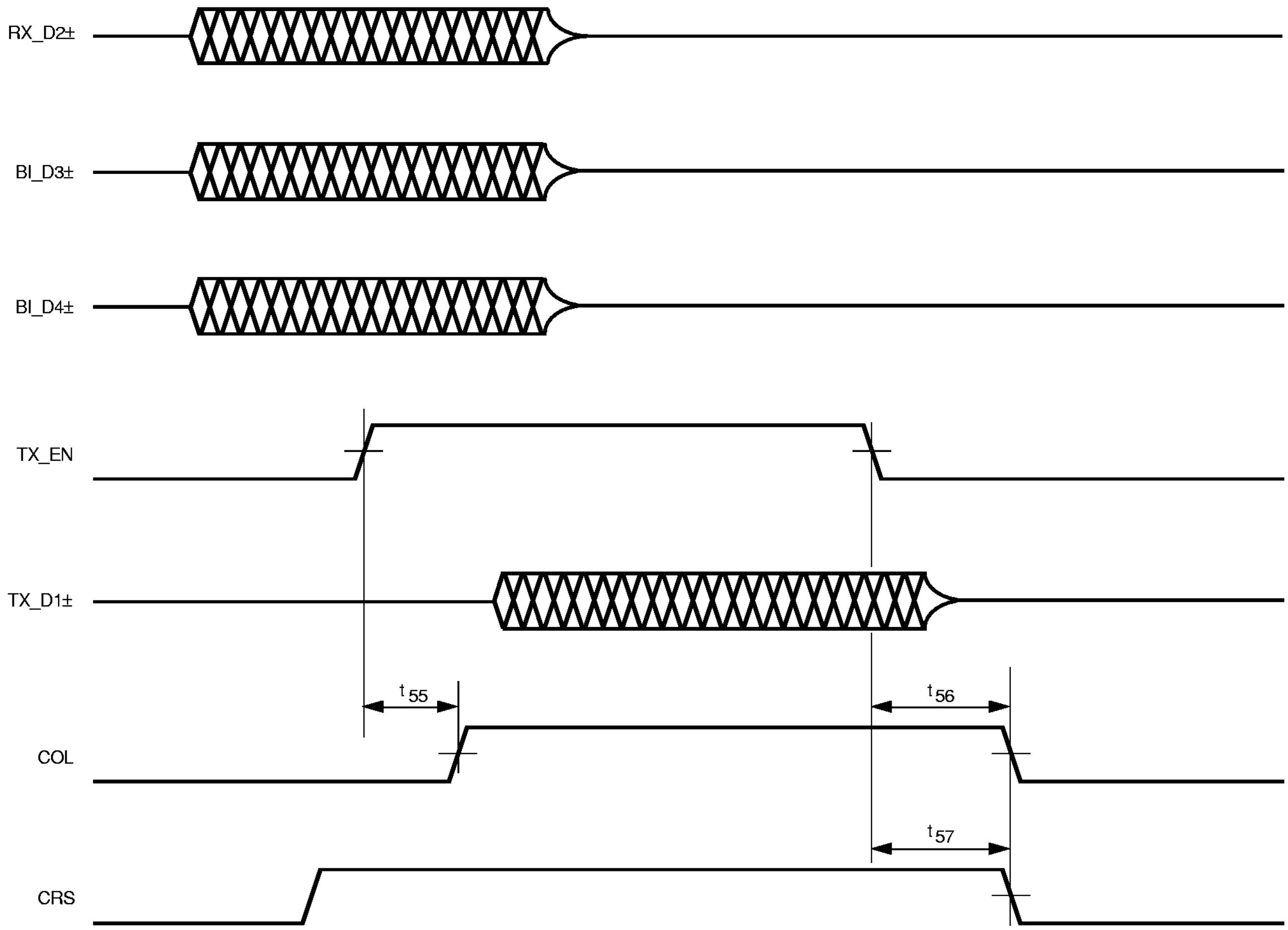
a) TP Output on TX_D1 only.

BII 10 MB

Same as MII 10 MB

Figure 27. Collision Timing, Receive

MII 100 MB



MII 10 MB

Same as MII 100 MB Except:
a) TP Input on RX_D2 Only.

BII 10 MB

Same as MII 10 MB

Figure 28. Collision Timing, Transmit

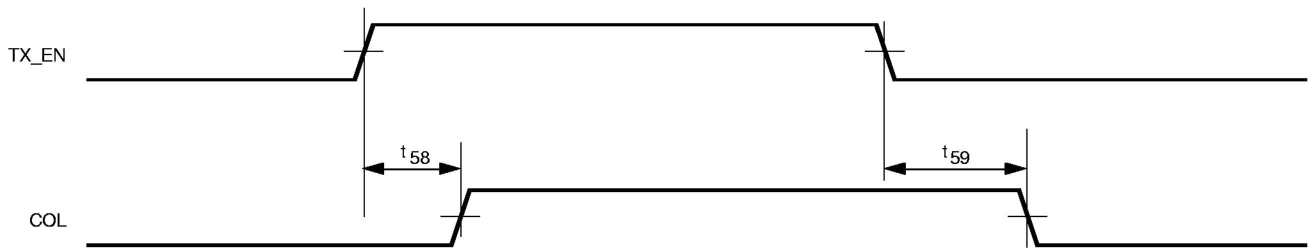
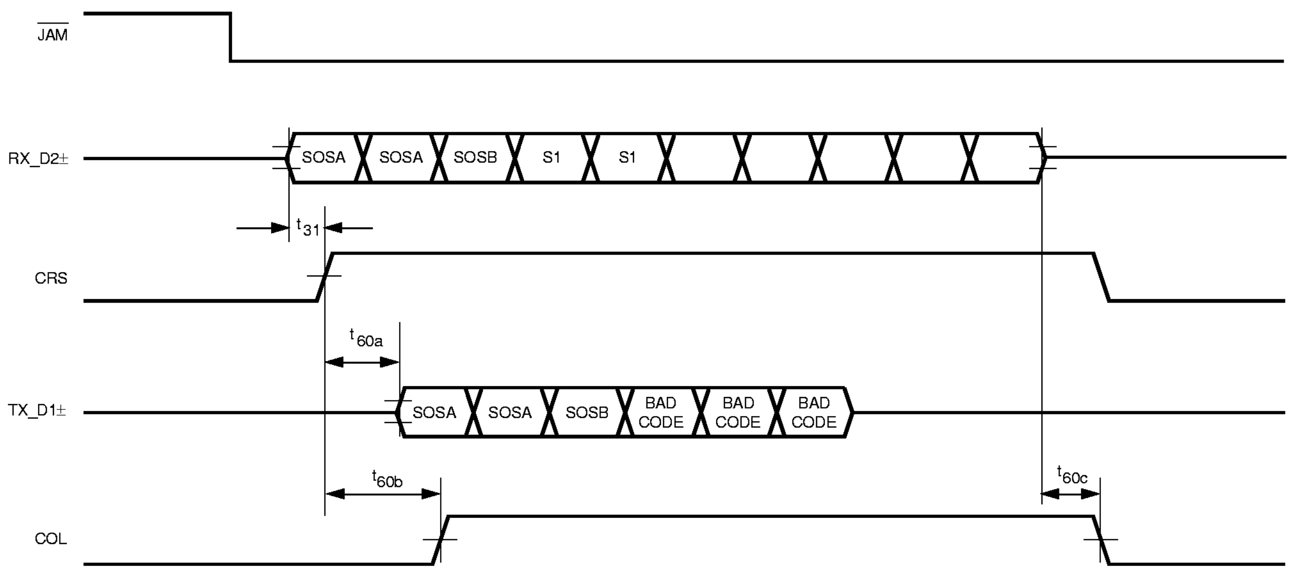


Figure 29. Collision Test Timing

MII 100 MB



MII 10 MB

Not Applicable

BII 10 MB

Not Applicable

Figure 30. JAM Timing

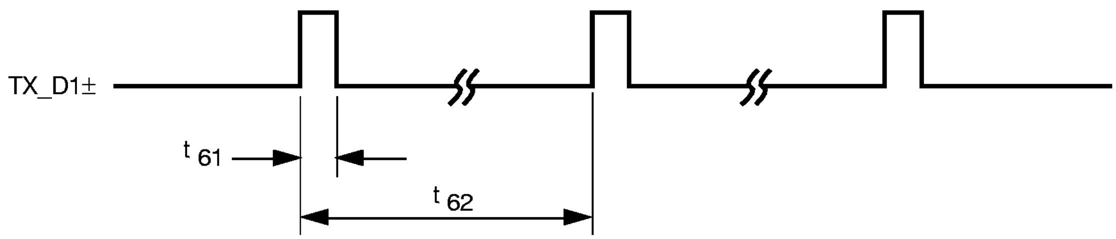
Link Pulse Timing Characteristics

Refer To Figures 31, 32 and 33 For Timing Diagram

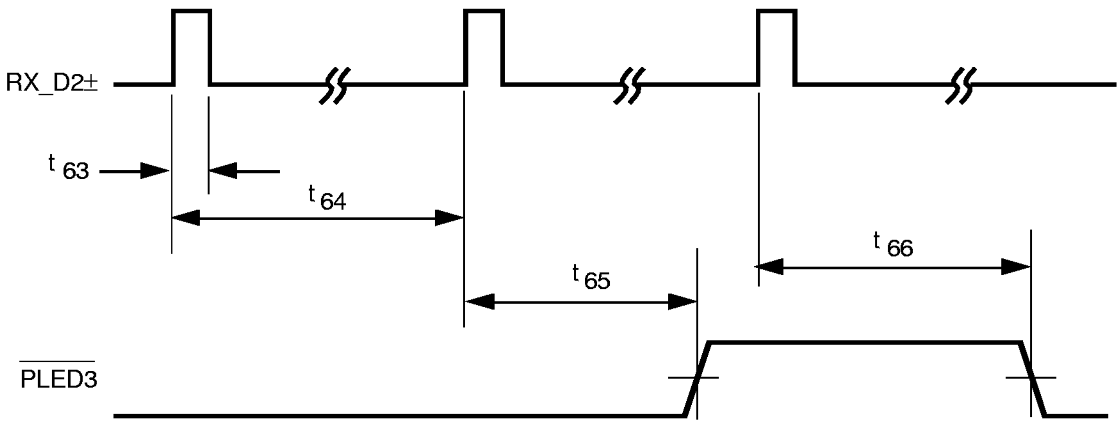
SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{61}	NLP Transmit Link Pulse Width	See Figure 11			ns	
t_{62}	NLP Transmit Link Pulse Period	8		24	mS	
t_{63}	NLP Receive Link Pulse Width Required For Detection	50			nS	
t_{64}	NLP Receive Link Pulse Minimum Period Required For Detection	6		7	mS	link_test_min
t_{65}	NLP Receive Link Pulse Maximum Period Required For Detection	50		150	mS	link_test_max link_loss
t_{66}	NLP Receive Link Pulses Required To Exit Link Fail State	3	3	3	Link Pulses	lc_max
t_{61a}	T4LP Transmit Link Pulse Width	See Figure 10			ns	
t_{62a}	T4LP Transmit Link Pulse Period	0.6		1.8	mS	
t_{63a}	T4LP Receive Link Pulse Width Required For Detection	40			nS	
t_{64a}	T4LP Receive Link Pulse Minimum Period Required For Detection	0.15		0.45	mS	
t_{65a}	T4LP Receive Link Pulse Maximum Period Required For Detection	5		6	mS	
t_{66a}	T4LP Receive Link Pulses Required To Exit Link Fail State	15		Link Pulses		31 Link Pulses Followed By a Packet or 96 More Link Pulses Are To Required Exit Link Fail
t_{67}	FLP Transmit Link Pulse Width	100		150	nS	
t_{68}	FLP Transmit Clock Pulse To Data Pulse Period	55.5	62.5	69.5	µS	
t_{69}	FLP Transmit Clock Pulse To Clock Pulse Period	111	125	139	µS	

Link Pulse Timing Characteristics (continued)

SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{70}	FLP Transmit Link Pulse Burst Period	8		22	mS	
t_{71}	FLP Receive Link Pulse Width Required For Detection	50			nS	
t_{72}	FLP Receive Link Pulse Minimum Period Required For Clock Pulse Detection	5		25	µS	
t_{73}	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	µS	
t_{74}	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	µS	
t_{75}	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	µS	
t_{76}	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t_{77}	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	mS	
t_{78}	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	mS	
t_{79}	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulse Bursts	
t_{80}	FLP Receive Acknowledge Fail Period	1200		1500	mS	
t_{81}	FLP Transmit Renegotiate Link Fail Period	1200		1500	mS	BREAK_LINK_TIMER
t_{82}	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotation Has Completed	750		1000	mS	LINK_FAIL_INHIBIT_TIMER

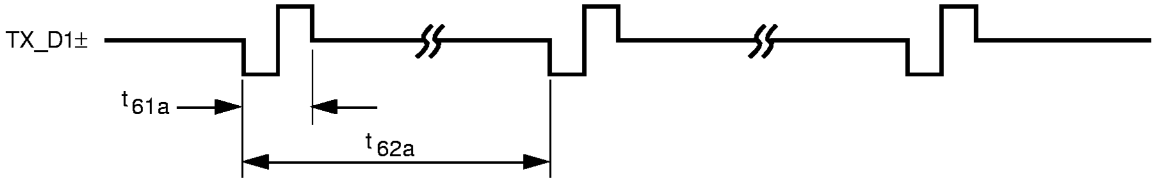


a.) Transmit NLP

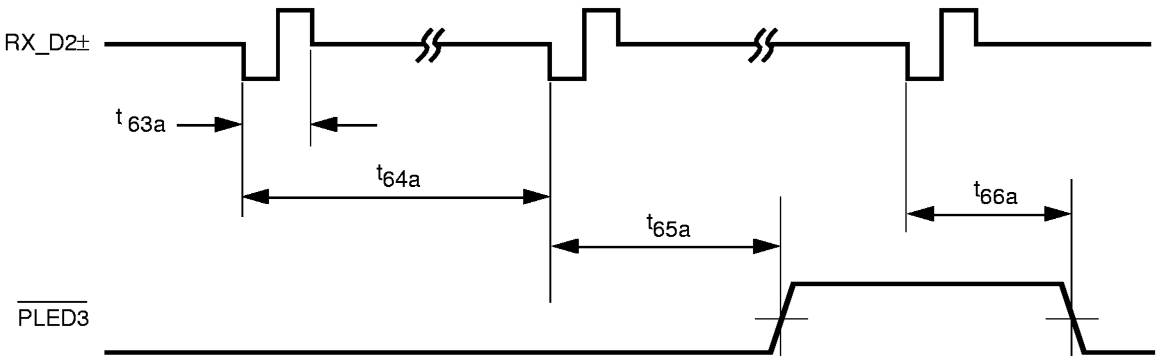


b.) Receive NLP

Figure 31. NLP Link Pulse Timing

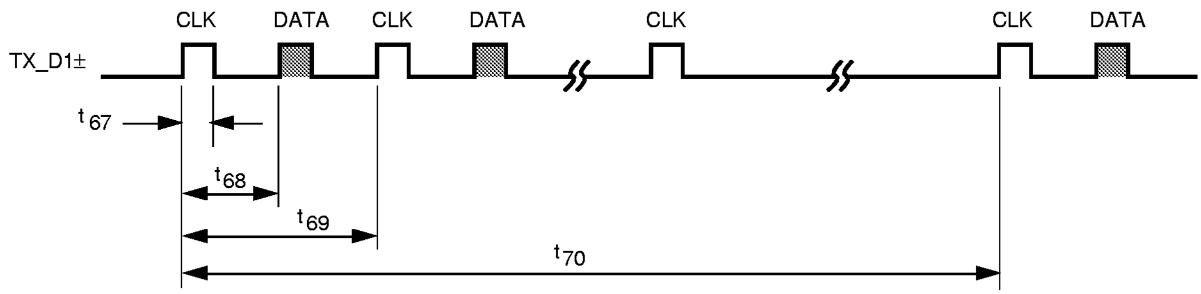


a.) Transmit T4LP

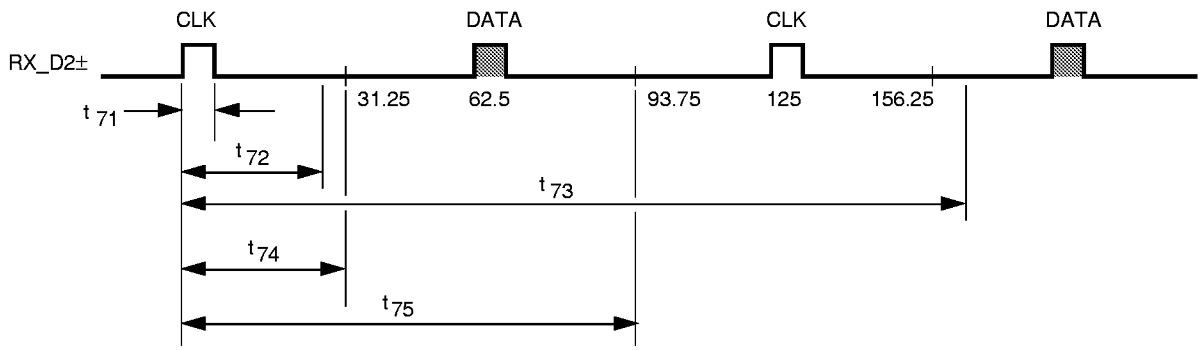


b.) Receive T4LP

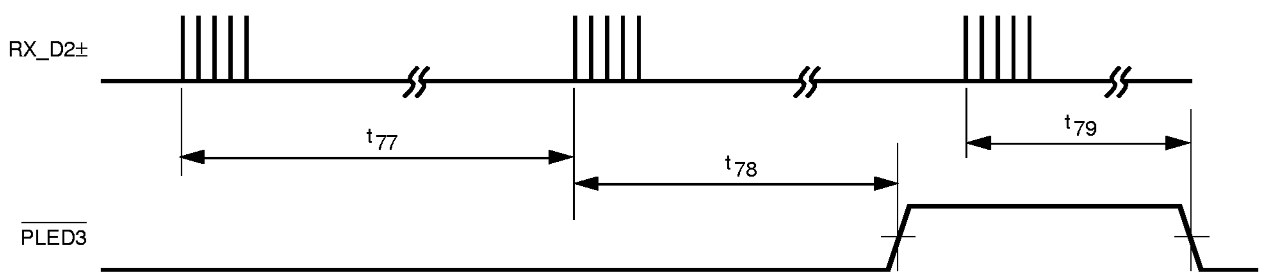
Figure 32. T4LP Link Pulse Timing



a.) Transmit FLP and FLP Burst



b.) Receive FLP



c.) Receive FLP Burst

Figure 33. FLP Link Pulse Timing

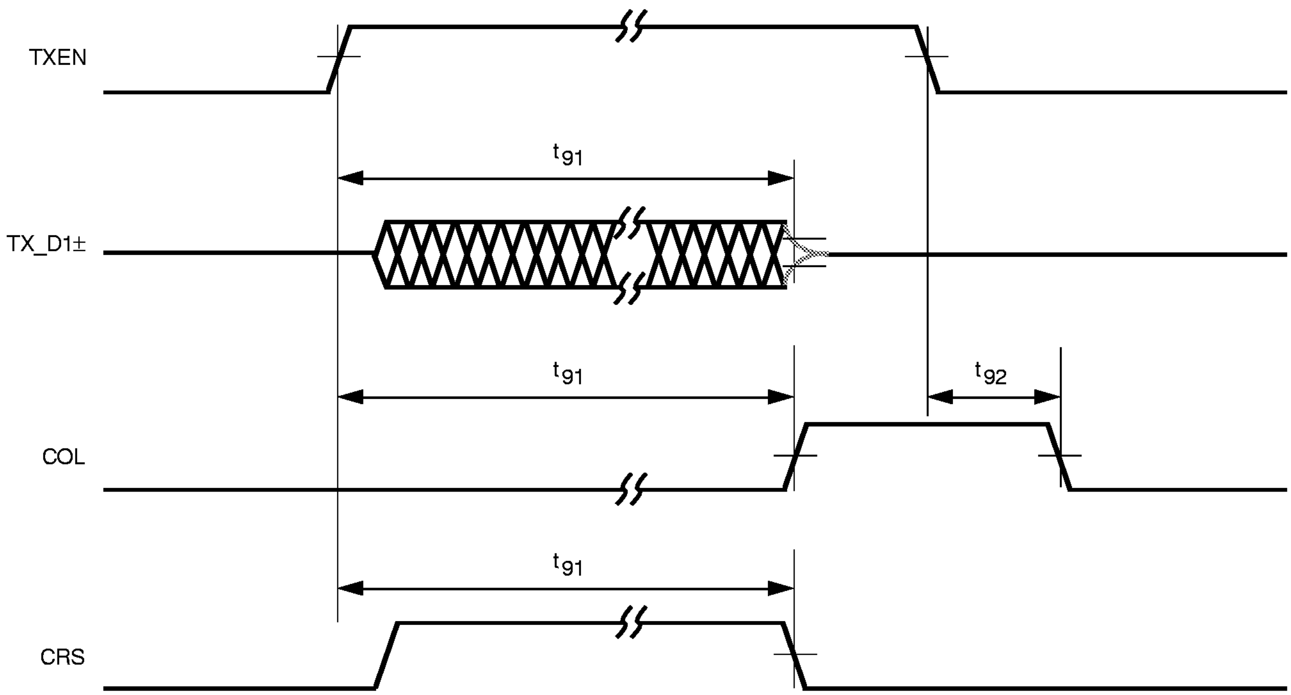
Jabber Timing Characteristics

Refer To Figure 34 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	TYP	MAX	UNIT	CONDITIONS
t_{91}	Jabber Activation Delay Time	20		50	mS	10 Mbps
t_{92}	Jabber Deactivation Delay Time	250		750	mS	10 Mbps

MI 100 Mb — Not Applicable

MI 10 MB



BII 10 MB

Same as MI 10

Figure 34. Jabber Timing

LED Driver TIming Characteristics

Refer To Figure 35 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	TYP	MAX	UNIT	CONDITIONS
t_{96}	$\overline{\text{PLED[3:0]}}$ On Time	80		105	mS	
t_{97}	$\overline{\text{PLED[3:0]}}$ Off Time	80		105	mS	

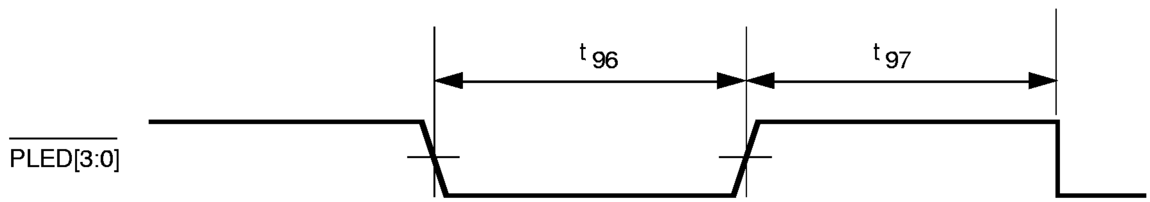


Figure 35. LED Driver Timing

MI Serial Port Timing Characteristics

Refer To Figure 36 and 37 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	TYP	MAX	UNIT	CONDITIONS
t_{101}	MDC High Time	20			nS	
t_{102}	MDC Low Time	20			nS	
t_{103}	MDIO Setup Time	10			nS	Write Bits
t_{104}	MDIO Hold Time	10			nS	Write Bits
t_{105}	MDC To MDIO Delay			20	nS	Read Bits
t_{106}	MDIO Hi-Z To Active Delay			20	nS	Write-Read Bit Transition
t_{107}	MDIO Active To HI-Z Delay			20	nS	Read-Write Bit Transition
t_{108}	Frame Delimiter (Idle)	32			Clocks	MDC Clocks with MDIO = 1's
t_{109}	End of Frame to MDINT Transition			100	nS	
t_{110}	MDC to MDIO Interrupt Pulse Assert Delay			100	nS	
t_{111}	MDC to MDIO Interrupt Pulse Deassert Delay			100	nS	

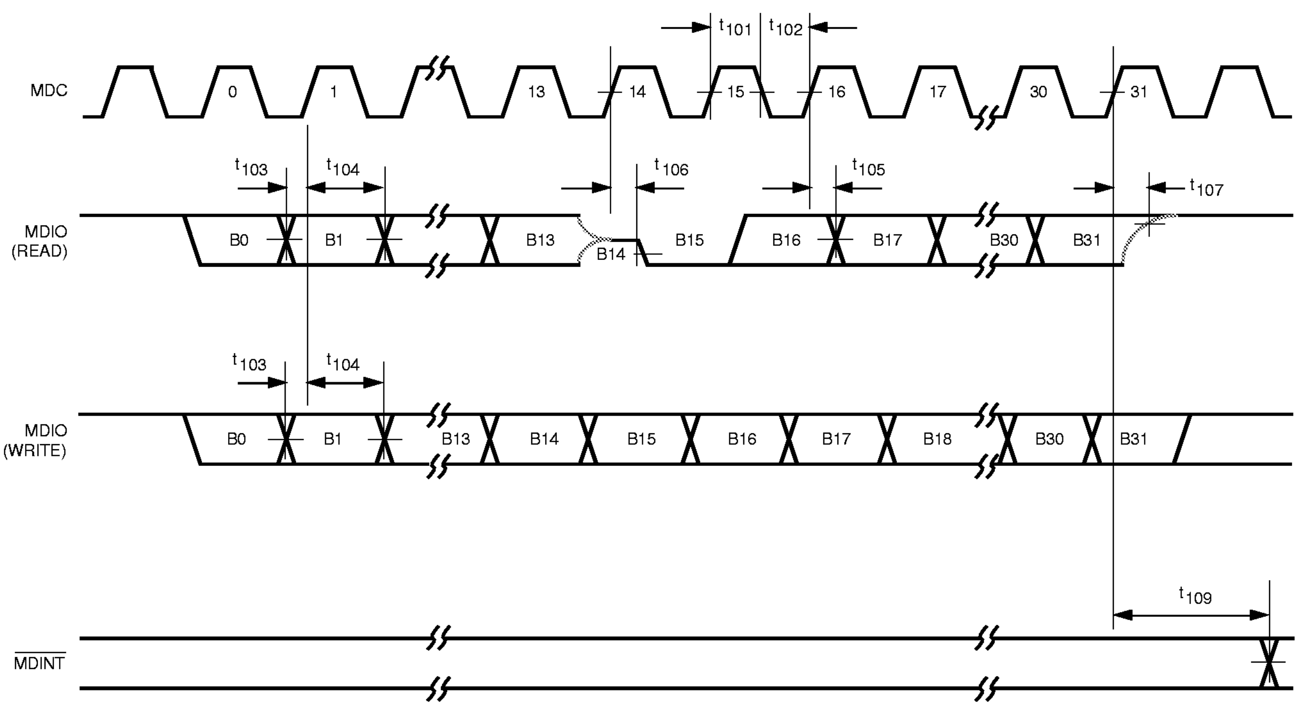


Figure 36. MI Serial Port Timing

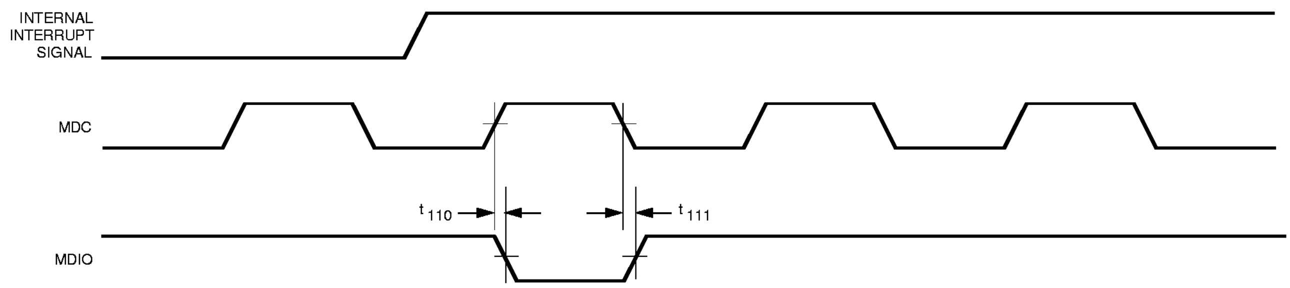
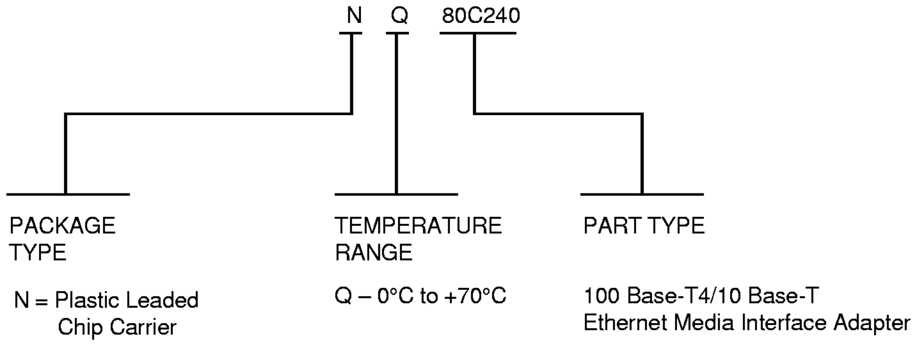


Figure 37. MDIO Interrupt Pulse Timing

Ordering Information



Revision History

9/5/96

Page 77; The 44 Pin PLCC EDQUAD dimension diagram has been added to this data sheet.

2/6/97

Page 1; Features, Many User Features and Options, Transmit Level Adjust has been deleted.

Page 2; Table of Contents
- 3.8.3 Transmit Level Adjust, has been changed to Optional Reference Voltage Input.
- 3.8.6 Transmit Powerdown has been deleted.

Page 4; Pin Description, Pin 8-24, Description, Positive Supply, +5 +/– 10% Volts has been changed to Positive Supply, +5 +/– 5% Volts.

Page 15;
- 3.8.3 Transmit Level Adjust and Table 1 have been deleted.
- 3.8.3 Optional Reference Voltage Input, is the new 3.8.3 section.
- 3.8.6 Transmit Powerdown has been deleted.

Page 16; Figure 7. TP Output Voltage Template - 10 Mbps,alphabetic references have been added to illustration.
- Voltage Template Values for Figure 7 has been added.

Page 28; Table 4. MI Serial Port Register Map
- All 0 Reserve Bit Values have been changed to Reserves = 0.
- All 1 Reserve Bit Values have been changed to Reserves = 1.
- Configuration 1
  - XMT_PDN has been changed to Reserves = 1.
  - TLVL3 has been changed to Reserves = 1.
  - TLVL2 has been changed to Reserves = 0.
  - TLVL1 has been changed to Reserves = 0.
  - TLVL0 has been changed to Reserves = 0.
- Note: All Reserves Bit Values must be programmed as specified, has been added.

Revision History

2/6/97

Page 35; Table 11 Register (Configuration 1) Structure and Bit Definition.
- Bit 16.12,
  - Symbol is now blank.
  - Name is now blank.
  - Definition has been changed from 1 = TP Transmitter Powered Down, 0 = Normal to 1 = Reserved, Must be Written to 1.
  - Def. has been changed from 0 to See Definition.
- Bit 16.8,
  - Symbol is now blank.
  - Name is now blank.
  - Definition, See Table 1, has been changed Reserved = 1
- Bit 16.5-16.7,
  - Symbol is now blank.
  - Name is now blank.
  - Definition, See Table 1, has been changed Reserved = 0

Page 39; Section 5.3 TP Transmit Output Current Set, Paragraph 4, Since the TP... has been changed to, Since the TP output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it is necessary to minimize PC board loading effect in order to meet transmit amplitude and pulse shape as specified in IEEE 802.3 documents.

Page 43; Figure 17. MII Output Driver Characteristics, Rol_{MIN} has been changed to Rol_{MIN} = 40 ohm.

Page 47; The Absolute Maximum Ratings have changed.

Page 48; DC Electrical Charateristics,
- 2. V_{CC} = 5V +/– 10% has been changed to 2. V_{CC} = 5V +/– 5%.
- I_{IL} Conditions V_{IN} = GND $\overline{PLED[3:0]}$, TX_CLK50/RX_EN $\overline{MDINT}$/LPBK/$\overline{JAM}$
  - I_{IL} Limit (min) has been changed from 12 to -3.
  - I_{IL} Limit (typ) has been changed from 25 to -8.
  - I_{IL} Limit (Max) has been changed from 50 to -25.
- I_{IL} Conditions V_{IN} = GND OSCIN
  - I_{IL} Limit (min) is now -20.
  - I_{IL} Limit (Max) has been changed from -150 to -100.
- I_{IH} Input High Current
  - Conditions V_{IN} = V_{CC} row has been removed.
  - Conditions V_{IN} = V_{CC} OSCIN, Limit (min) is now 30.
- V_{OH} Output High Current, Conditions I_{OH} = 50µA $\overline{PLED[3:0]}$. $\overline{MDINT}$ has been changed to I_{OH} 3µA $\overline{PLED[3:0]}$, $\overline{MDINT}$
- I_{CC}, Limit (max) has been changed from 350 to 520.

Page 49; Twisted Pair Characteristics, Transmit
- 2. V_{CC} = 5V +/– 10% has been changed to 2. V_{CC} = 5V +/– 5%.
- T_{OIR}, TP Output current Adjustment Range and T_{ORA}, TP Output Current TLVL Step Accuracy , have been deleted.

Revision History

2/6/97

Page 50; Twisted Pair Characteristics Receive

- 2. V_{CC} = 5V +/– 10% has been changed to 2. V_{CC} = 5V +/– 5%.
- R_{UTP} , Conditions 10 Mbps Limit (min) has been changed from 230 to 325.
- R_{UTP} , Conditions 10 Mbps Limit (max) has been changed from 360 to 467.
- R_{UTP} , Conditions 10 Mbps RLVL = 1, Limit (min) has been changed from 135 to 195.
- R_{UTP} , Conditions 10 Mbps RLVL = 1, Limit (max) has been changed from 215 to 280.

Page 51; AC Test Timing Conditions

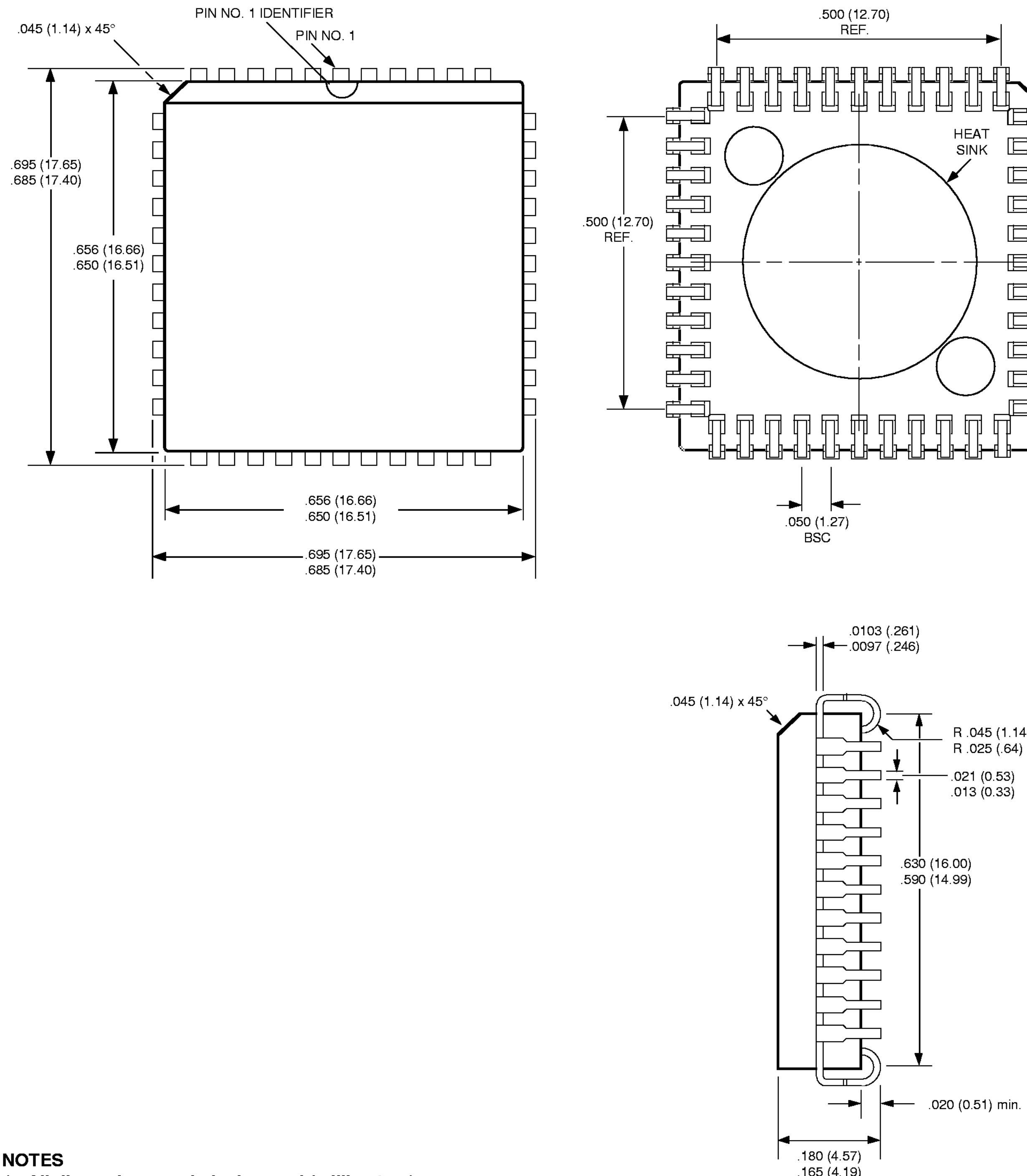
- 2. V_{CC} = 5V +/– 10% has been changed to 2. V_{CC} = 5V +/– 5%.

Page 62; Collision and JAM Timing Characteristics I_{60C} Limit (max) has been changed from 360 to 440.

Page 77; A pagination change has occurred beginning on page 77.

Surface Mount Packages

44 PIN PLCC EDQUAD



NOTES

1. **All dimensions are in inches and (millimeters).**
2. **Dimensions do not include mold flash. Maximum allowable flash is .008 (0.20).**
3. **Formed leads shall be planar with respect to one another within 0.004 inches.**