54AC/74AC161 • 54ACT/74ACT161
54AC/74AC163 • 54ACT/74ACT163

Synchronous Presettable Binary Counter

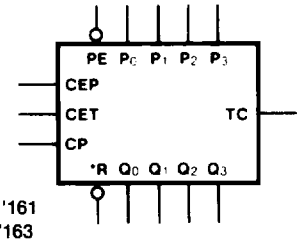
Description

The 'AC/'ACT161 and 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'AC/'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- **Synchronous Counting and Loading**
- **High-Speed Synchronous Expansion**
- **Typical Count Rate of 125 MHz**
- **Outputs Source/Sink 24 mA**
- **'ACT161 and 'ACT163 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol

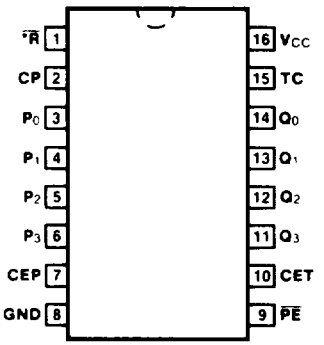


* $\overline{MR}$ for '161
* $\overline{SR}$ for '163

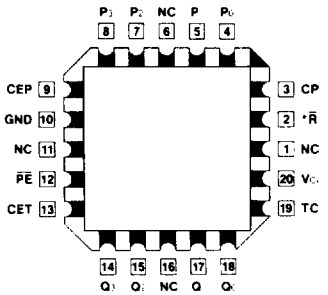
Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ ('161)	Asynchronous Master Reset Input
$\overline{SR}$ ('163)	Synchronous Reset Input
P_0 - P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0 - Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

* $\overline{MR}$ for '161
* $\overline{SR}$ for '163

Functional Description

The 'AC/'ACT161 and 'AC/'ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('161), synchronous reset ('163), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, '161), Synchronous Reset ($\overline{SR}$, '163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('161) or $\overline{SR}$ ('163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT161 and 'AC/'ACT163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP•CET•$\overline{PE}$

$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

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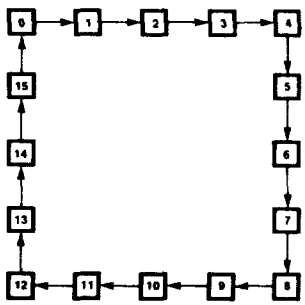
Mode Select Table

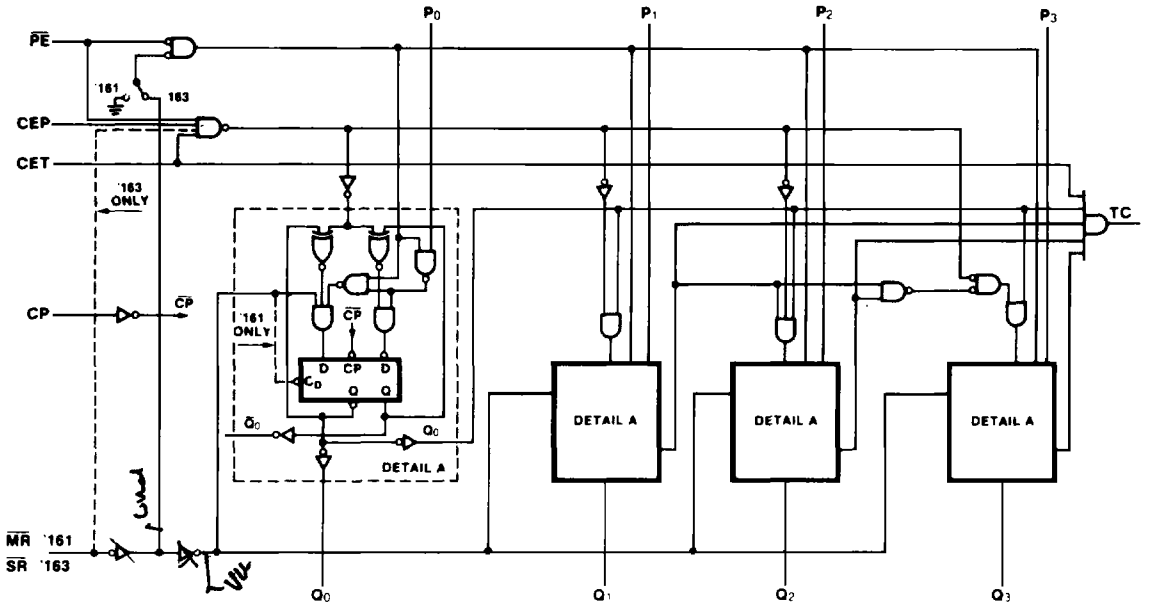
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (∫)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT161/163)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC161 $T_A = +25°C$, $C_L = 50$ pF			54AC161 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC161 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		87 118						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0		7.5 5.5						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		11.0 8.0						ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0		7.5 5.5						ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0		8.5 6.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0		11.0 8.0						ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC161 $T_A = +25°C$ $C_L = 50$ pF	54AC161 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC161 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.5			ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5			ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0			ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.5 3.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT161 $T_A = +25°C$, $C_L = 50$ pF			54ACT161 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT161 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	115	125				100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	9.5			1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	10.5			1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.0			1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	12.5			1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	8.5			1.0	10.0	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	9.5			1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.0	10.0			1.0	11.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	1.0	8.0	13.5			1.0	14.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT161		54ACT161	74ACT161	Units	Fig. No.
			$T_A = +25°C$, $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	9.5		11.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0		0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{MR}$ to CP	5.0	4.0	8.5		9.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{MR}$ to CP	5.0	−5.5	−0.5		−0.5	ns	3-9
t_s	Setup Time HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		9.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5		−0.5	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0		0	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0		3.5	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0		3.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0		7.5	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0		0.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC163 $T_A = +25°C$, $C_L = 50$ pF			54AC163 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC163 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	87 118				60 95		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0			1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	12.0 9.5			1.0 1.0	13.0 10.0	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	9.5 7.0	15.0 10.5			1.0 1.0	16.5 11.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	11.0 8.0	14.0 11.0			1.0 1.0	15.5 11.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	7.5 5.5	9.5 6.5			1.0 1.0	11.0 7.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	8.5 6.0	11.0 8.5			1.0 1.0	12.5 9.5	ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC163 $T_A = +25°C$ $C_L = 50$ pF		54AC163 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC163 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0	13.5 8.5		16.0 10.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0	−1.0 0		−0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14.0 9.5		16.5 11.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5		−0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5		14.0 8.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5		−0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5		7.0 5.0	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0		0 0.5	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5		4.0 3.0	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0		4.5 3.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT163 $T_A = +25°C$, $C_L = 50$ pF			54ACT163 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT163 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120	128				105		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	10.0			1.0	11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	11.0			1.0	12.0	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.5			1.0	13.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	13.5			1.0	15.0	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	9.0			1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	10.0			1.0	11.0	ns	3-6

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT163		54ACT163	74ACT163	Units	Fig. No.
			$T_A = +25°C$, $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	10.0		12.0	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0.5		0.5	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0		11.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5		−0.5	ns	3-9
t_s	Setup Time HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		10.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5		0	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0		0.5	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5		3.5	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5		3.5	ns	3-6

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V